

Aluminum-silicon interdiffusion in silicon heterojunction solar cells with a-Si:H(i)/a-Si:H(n/p)/Al rear contacts

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Abstract — We characterize a-Si:H(i)/a-Si:H(n)/Al and a-Si:H(i)/a-Si:H(p)/Al contacts implemented on the rear side of silicon heterojunction solar cells. Electrical test structures and full-area solar cells employing these contacts demonstrate promising performance. For example, a-Si:H(i)/a-Si:H(p)/Al test structures with a 40-nm-thick a-Si:H(p) layer that were annealed at 180 °C had contact resistivities of 48 m Ω ·cm² and implied open-circuit voltage losses after metallization of only 9 mV. Similarly, solar cells with full-area rear a-Si:H(i)/a-Si:H(n)/Al contacts that were annealed at 150 °C had open-circuit voltages of 717 mV and contact resistivities of 9.4 m Ω ·cm². For thinner doped a-Si:H layers and higher annealing temperatures, the contacts become less stable and performance degrades. Complementary transmission electron microscopy and energy-dispersive x-ray spectroscopy analysis show the Al-Si interactions at these interfaces that explain the range of exhibited performance. This analysis leads to a better understanding of the materials properties limiting the contact stability.

Index Terms — silicon heterojunction solar cells, amorphous silicon, crystalline silicon, photovoltaic metallization.

I. INTRODUCTION

To prevent degradation of the hydrogenated amorphous silicon (a-Si:H) layers in silicon heterojunction (SHJ) solar cells, the cells are typically metallized by screen-printing low-temperature Ag paste or sputtering Ag on indium-oxide-based transparent conductive oxides (TCOs) [1]. Techno-economic modeling by Louwen *et al.* in 2016 showed that Ag and In-containing films are the costliest components of a SHJ cell after the high-purity n-type c-Si wafer. Specifically, the rear ITO/Ag layers in screen-printed bifacial and full-area- sputtered configurations account for approximately 18% and 9% of cell production cost, respectively [2]. The low-temperature pastes used are more resistive than high-temperature Al-BSF/PERC pastes and, consequently, more costly due to the higher Ag consumption required to achieve sufficiently low lateral resistivity [1]. The PV industry already accounts for approximately 11% of the global Ag market supply, and because of continued demand, the bulk cost of Ag is expected to remain high [3].

As a result, metallization techniques to SHJ cells that reduce or eliminate Ag consumption are an active area of research. Alternative metallization approaches include Smart Wire Connection Technology, drop-on-demand printing of low-temperature Ag inks, screen-printing of Cu-based pastes,

electroplating of Cu, and application of metals other than Ag with no TCO [4-9]. According to the aforementioned 2016 techno-economic modeling, embracing the latter approach and replacing physical-vapor-deposited (PVD) ITO/Ag with a single Al layer would reduce the cost contribution of the rear metallization from 2.6 ¢/Watt to 0.7 ¢/Watt [2]. For PVD metallization, an even more insidious cost effect than the material cost is the large capital investment requirements, which limits the manufacturing growth rate and makes competition difficult with incumbent screen-printing [10]. A single rear Al layer would reduce the number of tools—and thus the capital barrier—needed to enter into or expand cell manufacturing.

It is because of low cost and adequate electrical conductivity that the solar industry already employs Al metallization extensively; Al-BSF and Passivated Emitter and Rear Contact (PERC/PERL) technologies with Al metallization comprised over 95% of the worldwide silicon module market share in 2019 [11]. However, the direct contact of the Al paste to the c-Si absorber in these cell structures causes large recombination losses and severely limits the upper limit of device efficiency. Passivating contacts, such as SHJ contacts, avoid these recombination losses by electronically separating the absorber from the metal electrode and, consequently, are expected to capture increasing market share [11]. Existing Al pastes are not viable for SHJ cells, however, as the processing temperatures are incompatible: degradation of the surface passivation due to hydrogen effusion occurs well-below the paste firing temperature [12]. Further, no low-temperature Al paste analog currently exists for SHJ technology. Consequently, PV researchers exploring Al metallization for use in SHJ devices employ PVD processes such as thermal evaporation and sputtering.

Prior to use in SHJ solar cells, stacks of a-Si:H and Al were studied in depth due to the dramatic amount of atomic movement at surprisingly low annealing temperatures and for their potential to form low-cost poly-crystalline Si [13-16]. The degree of Si-Al interdiffusion upon low-temperature annealing is remarkable and can result in complete layer exchange of the Si and Al across the interface [17]. When applied as a contact for c-Si solar cells, a-Si:H/Al stacks exhibit low contact resistance. For instance, Labie *et al.* demonstrated contact resistivities of 10 m Ω ·cm² for a-Si:H(i)/a-Si:H(n)/Al contacts [18]. Such low values make these contacts appealing for

implementation in SHJ cells; however, simultaneously maintaining the excellent passivation afforded by the a-Si:H has proven to be a challenge due to the Si-Al interdiffusion at low temperatures.

For a-Si:H/Al stacks in SHJ devices, the Al atomic reservoir is significantly larger than the adjacent Si because the a-Si:H films are so thin. Further, a-Si:H contains relatively high free energy from its high degree of disorder and large amount of hydrogen, each of which promote atomic rearrangement within the a-Si:H film during thermal processing [19]. The atomic concentration gradient, coupled with the high free energy, creates a driving force for Al to be incorporated in the a-Si:H film. When Al is integrated into full SHJ cells, this interdiffusion is exhibited as a tradeoff between transport and passivation. Stang *et al.* fabricated SHJ cells with Al metallization and reported an increase in fill factor (FF) from 72.9 to 78.7% and a decrease in open-circuit voltage (V_{oc}) from 684 to 649 mV after 10 additional minutes of annealing at 150 °C (following an original 5-minute anneal) [8]. Konishi *et al.* reported the same FF - V_{oc} interchange and found that devices with thicker a-Si:H layers maintained their passivation at higher temperatures [9]. Each of these studies attributed this tradeoff to Si/Al interdiffusion, where Al entering the a-Si:H film increases conductivity, and thereby FF , but also increases recombination, degrading V_{oc} . This general sensitivity of the solar cell figures of merit to a-Si:H thickness and annealing temperature has been observed consistently, but a detailed analysis of the interface interactions has not yet been reported.

Here, we investigate the properties of a-Si:H(i)/a-Si:H(n/p)/Al contacts with varying a-Si:H doped layer thickness and annealing temperatures. Specifically, we characterize the contact resistivity and passivation quality of test structures utilizing the transfer length method (TLM) and photoconductance measurements, respectively. Based on the test structure results, we fabricate and measure full SHJ devices with these contacts. We then link the electrical behavior of the devices to the morphology and composition of the contact interfaces observed in scanning transmission electron microscopy (STEM). By spanning a wide parameter space in a step-wise fashion, this work identifies promising processing conditions for high-performance SHJ cells utilizing Al metallization and provides finer insight into the materials interactions in the contacts.

II. EXPERIMENTAL DETAILS

A. Electrical Contact Properties

The metrics selected to quantify resistance and passivation quality were, respectively, contact resistivity, ρ_c , and the difference between the implied open-circuit voltage (iV_{oc}) of the initially passivated wafer and the final V_{oc} after all sputtering and annealing steps, $iV_{oc}-V_{oc}$. The latter metric for passivation loss is unusual for contact characterization but functional in this instance. Typically, recombination attributable to diffused and metal contacted regions is quantified with the recombination current prefactor, J_0 , which has been measured and reported for

numerous solar cell technologies [20-22]. J_0 is most often calculated with the Kane and Swanson technique utilizing photoconductance data from a Sinton WCT-120 lifetime tester [23]. Since Al-Si atomic interdiffusion has a strong impact on contact recombination and majority carrier conductivity, it is essential to test processing conditions that are fully representative of the final devices, but fully metallized cells are not measurable with photoconductance. We tested 10-nm-thick Al layers, which are thin enough to be compatible with a Sinton WCT-120, but found from cross-sectional electron microscopy that, at least for thick a-Si:H layers (up to 40 nm), such thin Al layers are not representative of full device metallization. Nast *et al.* similarly observed that the film thickness ratio of Al to a-Si:H is a key driver in the interdiffusion process [17]. Therefore, to measure passivation quality, $iV_{oc}-V_{oc}$ was used instead of the drop in iV_{oc} .

For contact resistance samples, n- and p-type Czochralski (Cz) silicon solar wafers were used for a-Si:H(i)/a-Si:H(n)/Al and a-Si:H(i)/a-Si:H(p)/Al contacts, respectively. For passivation test structures, only n-type Cz wafers were used. The wafers were 180 μm thick with a resistivity of approximately 4 $\Omega\cdot\text{cm}$. Prior to a-Si:H deposition, all wafers went through texturing in KOH solution, cleaning in Piranha and RCA-B solutions, and final oxide stripping in BOE solution. Next, 6-nm-thick symmetric a-Si:H(i) layers were deposited on all samples using plasma-enhanced chemical vapor deposition (PECVD). For the contact resistance samples, symmetric doped a-Si:H layers with thicknesses of 5, 10, 20, or 40 nm were deposited. For the passivation samples, the rear doped a-Si:H layer was again 5, 10, 20, or 40 nm thick, while the front side had an 8-nm-thick doped a-Si:H layer of the opposite polarity.

For the contact resistivity samples, Al was sputtered using a DC source power of 1 kW and a chamber pressure of 7.1 mTorr through a shadow mask to create a TLM pattern, as shown in Figure 1a. The spacings between adjacent pads were 0.25, 0.5, 1, 2, 4, and 8 mm respectively. For each a-Si:H thickness, the contact resistance of eight samples was measured after sputtering, and then remeasured after hot-plate annealing at 150, 180, 210, or 240 °C for 20 minutes in ambient atmosphere (two samples per temperature). Additionally, reference samples with ITO/Ag metallization in place of Al were fabricated and measured for comparison. ITO and Ag were sputtered sequentially through a single shadow mask without breaking vacuum. The ITO was deposited using a DC source power of 1 kW, a chamber pressure of 7.1 mTorr, and an oxygen partial pressure of 0.36 mTorr, which is the recipe used at the rear of the final solar cells. For the ITO/Ag references, a single doped a-Si:H thickness (8 nm) was used, but the same annealing temperatures were tested.

The structure of the passivation samples is shown in Figure 1b. iV_{oc} was measured on 16 locations of each wafer, immediately following the a-Si:H PECVD depositions, with a Sinton WCT-120 tool in transient mode. Next, sixteen 2 cm by 2 cm pads of front ITO and rear metal—either Al or ITO/Ag references—were sputtered onto the passivated wafers at the same locations where the iV_{oc} measurements were performed.

The front ITO was deposited using a DC source power of 1 kW, a chamber pressure of 5.5 mTorr, and an oxygen partial pressure of 0.17 mTorr. The rear Al or ITO/Ag were deposited using the same conditions as for the contact resistivity samples. The V_{oc} was then measured in the as-deposited state using a Sinton Suns-Voc tool. Finally, the V_{oc} was remeasured after hot-plate annealing at 150, 180, 210, or 240 °C for 20 minutes in ambient atmosphere (four pads per temperature).

B. Solar Cells with Full-Area Rear Metallization

The cells followed the same fabrication sequence as the passivation samples but included a final screen-printing step of Namics low-temperature Ag paste before the hot-plate anneal. However, rather than sweeping a range of thicknesses, a single rear doped a-Si:H thickness was chosen for both n-type (40 nm) and p-type (60 nm) contacts based on the performance of the contact resistivity and passivation samples. The a-Si:H(p) was thicker than targeted but nonetheless demonstrated the anticipated results. Additionally, the wafers used for solar cells were front-side textured and rear-side planar, as shown in Figure 1c, to facilitate subsequent electron microscopy of the rear contact. The post-screen-printing annealing temperature was varied to generate cells demonstrating a wide range of contact performance: The a-Si:H(i)/a-Si:H(n)/Al cells were annealed at 150, 180, and 210 °C, whereas the a-Si:H(i)/a-Si:H(p)/Al cells were annealed at 180, 210, and 240 °C. All cells were annealed for 20 minutes in ambient atmosphere,

except the p-type cell that was annealed at 240 °C, which was annealed for 40 minutes to magnify the effects of Si-Al interdiffusion. Complementary reference cells with rear ITO/Ag in place of Al were also fabricated for performance comparison. The ITO/Ag cells were annealed after screen-printing at 220 °C for 20 minutes. Current-voltage measurements were performed on each cell using a Sinton FCT-450 I-V tester to extract the solar cell figures of merit. The Sinton FCT-450 I-V tester calculates series resistance by comparing Suns- V_{oc} and I-V sweeps at the maximum power point [24]. The a-Si:H(i)/a-Si:H(n)/Al cells also had TLM structures on the same wafer as the cells, which was not possible with the a-Si:H(i)/a-Si:H(p)/Al cells since n-type wafers were used for all cells.

C. Electron microscopy and elemental mapping

Changes to the contact interfaces following the annealing step were probed using scanning transmission electron microscopy (STEM). After electrical characterization of the complete solar cells, lamella were lifted out from their rear contacts by focused ion beam and thinned, with final thinning at 5 kV. Bright-field images were taken using a JEOL ARM microscope operated at 200 keV. Elemental maps of samples were obtained using energy-dispersive X-ray spectroscopy (EDXS) to show local concentrations of Al and Si. The n-type sample annealed at 150 °C was mapped using electron energy-loss spectroscopy (EELS).

III. RESULTS AND DISCUSSION

A. a-Si:H(i)/a-Si:H(p)/Al Contacts

Figure 2a shows the contact resistivity of all a-Si:H(i)/a-Si:H(p)/Al test structures. After annealing, all Al-metallized TLM samples showed a significant decrease in contact resistivity to approximately $50 \text{ m}\Omega \cdot \text{cm}^2$. This initial decrease in contact resistivity can be attributed to breaking of the native silicon oxide overgrowth and improved interfacial adhesion [19]. The contact resistivities of the annealed Al samples were significantly lower than the ITO/Ag controls—which were about $200 \text{ m}\Omega \cdot \text{cm}^2$, consistent with our previous findings [25]—showing potential for advanced cell architectures utilizing optimized contact fractions and rear reflectors. For an idealized solar cell simulated in Quokka 2 with $J_0 = 10 \text{ fA}$, reducing ρ_c from 200 to $50 \text{ m}\Omega \cdot \text{cm}^2$ results in 0.7% absolute efficiency boost, and the optimized metalized area reduces from over 50% to approximately 25% [26, 27]. All Al samples annealed at low temperatures (150 and 180 °C) exhibited virtually identical contact resistivity. Higher thermal loads (210 and 240 °C) caused a drop of several orders of magnitude in the contact resistivity of the samples with thinner a-Si:H(p) layers (5 and 10 nm). As will be confirmed in Section IIID, such a drop in contact resistivity indicates that Al has entered the a-Si:H film at high concentrations and formed a highly conductive alloy, as observed in prior studies [8, 28, 29]. Additionally, the Al could be reaching the wafer, forming local c-Si/Al contacts with very low resistivity [30].

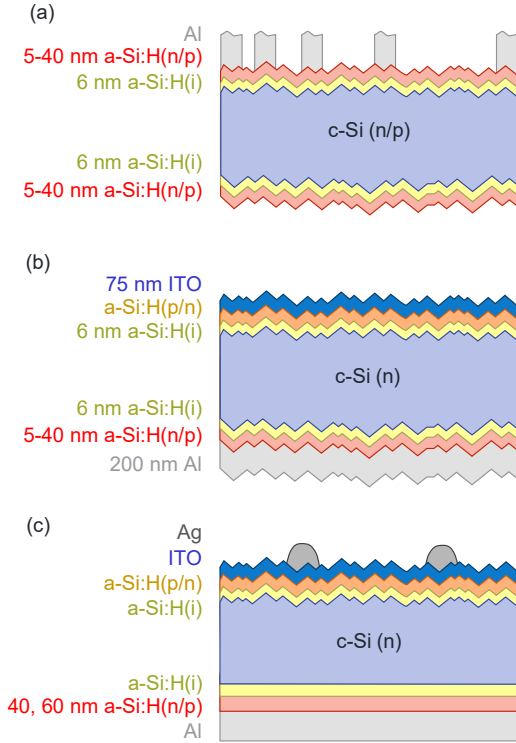


Fig. 1. Schematics (not to scale) of the (a) test structures used to measure contact resistivity, (b) test structures used to measure passivation quality, and (c) fully fabricated solar cells.

Further evidence of Al interdiffusion was observed in the passivation samples, in Figure 2b. With sufficient thermal load, the passivation of every Al-metallized structure deteriorated (increase in $iV_{oc}-V_{oc}$), while the ITO/Ag references saw minimal losses. We found no conditions for which the 5-nm-thick samples can maintain high-quality passivation, and only a narrow, low-temperature range in which 10-nm-thick samples can. This result necessitates thicker a-Si:H(p) layers for implementation of direct Al metallization in solar cells. For 20- and 40-nm-thick samples, there is a wider range of acceptable annealing conditions that maintain surface passivation, as similarly observed by Konishi *et al.* [9]. For the 20- and 40-nm-thick samples annealed at 180 °C, the average $iV_{oc}-V_{oc}$ was 11 and 9 mV, respectively. These processing conditions simultaneously resulted in low contact resistivity (40–50 mΩ·cm²) and are promising for use at the rear side of full devices.

Another noteworthy result from the $iV_{oc}-V_{oc}$ data is the large variance observed for the intermediate values of a-Si:H(p) thickness and annealing temperature, highlighting the sensitive nature of these contacts to process variation. Conversely, at the extreme temperatures and thicknesses tested, there is greater

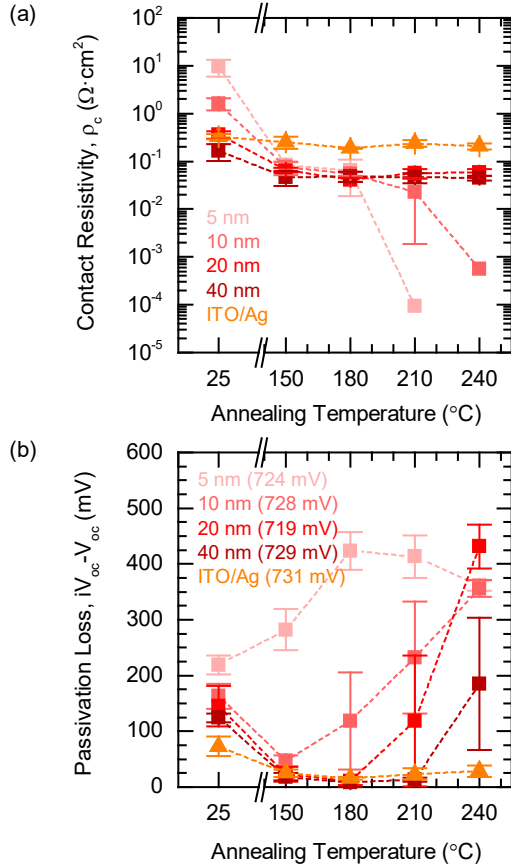


Fig. 2. (a) Contact resistivity and (b) passivation quality of test structures with a-Si:H(i)/a-Si:H(p)/Al contacts in the as-deposited condition (indicated by 25 °C) and after annealing. The average iV_{oc} values of the initial passivated wafers are shown in parentheses in (b).

consistency: A 10-nm-thick a-Si:H layer will almost certainly not maintain passivation when annealed at 180 °C or above,

whereas a 40-nm-thick sample will almost surely perform well at most temperatures. Additionally, the lowest and highest annealing temperatures will almost surely result in high-quality and deteriorated passivation, respectively, for most a-Si:H(p) film thicknesses.

B. a-Si:H(i)/a-Si:H(n)/Al Contacts

Figure 3a shows the contact resistivity of all a-Si:H(i)/a-Si:H(n)/Al contact structures. Contact resistivity decreased for all samples by 2–3 orders of magnitude, relative to the as-deposited values, after annealing at 150 °C. This is evidence that annealing treatments are imperative for direct Al metallization to both n- and p-type a-Si:H. The average contact resistivity of the 20-nm-thick a-Si:H(n) sample annealed at 150 °C was 3.5 mΩ·cm², considerably lower than the ITO/Ag references, which were generally around 500 mΩ·cm². (This value is on the high end for our reference SHJ process, but it is sensitive to the oxygen partial pressure when sputtering ITO, and that pressure is purposefully high for rear ITO layers because they do not need low sheet resistance and they should be as transparent as possible for IR wavelengths.) For the idealized solar cell simulated in Quokka with $J_0 = 10$ fA,

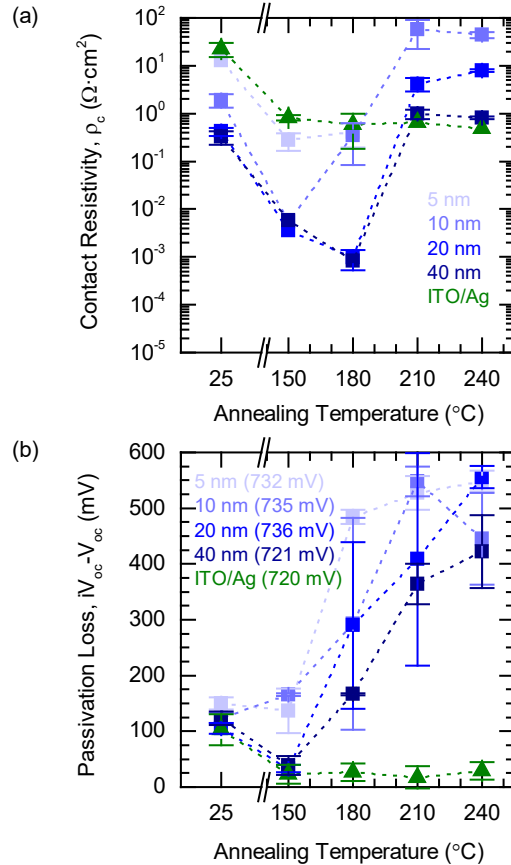


Fig. 3. (a) Contact resistivity and (b) passivation quality of structures containing with a-Si:H(i)/a-Si:H(n)/Al contacts in the as-deposited condition (indicated by 25 °C) and after annealing. The average iV_{oc} values of the initial passivated wafers are shown in parentheses in (b).

reducing ρ_c from 500 to 3.5 mΩ·cm² results in an absolute efficiency gain of 1.8% and reduces the optimal contact fraction

from nearly 100% to approximately 8% [26]. Further, $3.5 \text{ m}\Omega\cdot\text{cm}^2$ is considerably lower than the lowest reported resistivity value for an a-Si:H(i)/a-Si:H(n)/ITO/Ag contact of $55 \text{ m}\Omega\cdot\text{cm}^2$ [31]. An anneal at 180°C further reduced the contact resistivity for the 20- and 40-nm-thick samples, while the thinner samples increased relative to the 150°C anneal. At higher annealing temperatures (210 and 240°C), the thicker samples exhibited this same drastic increase in contact resistivity of several orders of magnitude. For the 5-nm-thick samples, the resistance values became immeasurable after annealing at 210 and 240°C . These trends are in stark contrast to the resistivity decrease with annealing temperature observed for Al in contact with a-Si:H(p), indicating that a drastic event—such as counter-doping—has occurred.

This hypothesis is supported by the passivation experiment, in Figure 3b, in which $iV_{oc}-V_{oc}$ approached 600 mV (i.e., V_{oc} approached zero) for many samples annealed at the higher temperatures. 240°C is not hot enough to drive Al into c-Si to induce extra bulk recombination, and surface recombination alone from Al reaching the c-Si surface cannot make the V_{oc} so low. Such a drastic reduction can occur only if both contacts are the same polarity, indicating that the n-type a-Si:H layers must have been counter-doped to p-type. This is in agreement with the TLM data and with prior results from Haque *et al.*, who showed a-Si:H(n) can be fully converted to p-type at 200°C when in contact with Al [14].

The interaction of Al and a-Si:H(n) is sufficiently strong that, even at 150°C , the 5- and 10-nm-thick samples were unable to maintain passivation: they had $iV_{oc}-V_{oc} \geq 137 \text{ mV}$ for every tested annealing temperature. On the other hand, the 20- and 40-nm-thick samples annealed at 150°C had average $iV_{oc}-V_{oc}$ of 33 and 39 mV, respectively. These losses are nearly acceptable but still higher than desirable, though the ITO/Ag references also had 23 mV loss after annealing at 150°C , indicating abnormally high systematic voltage losses for this particular batch of samples. All Al samples annealed at 180°C or higher had $iV_{oc}-V_{oc} \geq 167 \text{ mV}$. Thus, only the thickest samples (20 and 40 nm) annealed at the lowest tested temperature of 150°C demonstrated the potential for maintaining quality surface passivation. These conditions simultaneously resulted in $\rho_c = 1\text{--}10 \text{ m}\Omega\cdot\text{cm}^2$ and thus exhibit promise for implementation in full devices with low contact fraction.

C. Solar Cells with Full-Area Rear Metallization

Figure 4a shows the V_{oc} of the fabricated cells. As expected, the Al-metallized hole and electron contacts exhibited a wide range of performance based on annealing temperature, with the electron contact varying more dramatically. The origins of this variation will be discussed in greater detail in the subsequent section. The devices with rear a-Si:H(i)/a-Si:H(n)/Al and a-Si:H(i)/a-Si:H(p)/Al contacts annealed at the lowest tested temperatures had V_{oc} s of 717 and 696 mV, respectively. Each of these values was higher than the respective ITO/Ag reference cells, indicating good potential for device performance when passivation is maintained.

The J_{sc} of the cells are shown in Figure 4b. Though the ITO/Ag stack is known to have superior reflectance than Al alone, we observed $<1 \text{ mA/cm}^2$ difference in J_{sc} between the best performing Al cells and the ITO/Ag references. We attribute this to the use of planar-rear wafers and front ITO thickness variation. In a separately prepared batch with symmetric random pyramid texture, we measured Al and ITO/Ag to yield integrated J_{sc} s of 37.5 and 40.3 mA/cm^2 , respectively, with nearly all losses occurring at longer wavelengths. Minimizing these parasitic absorption losses at

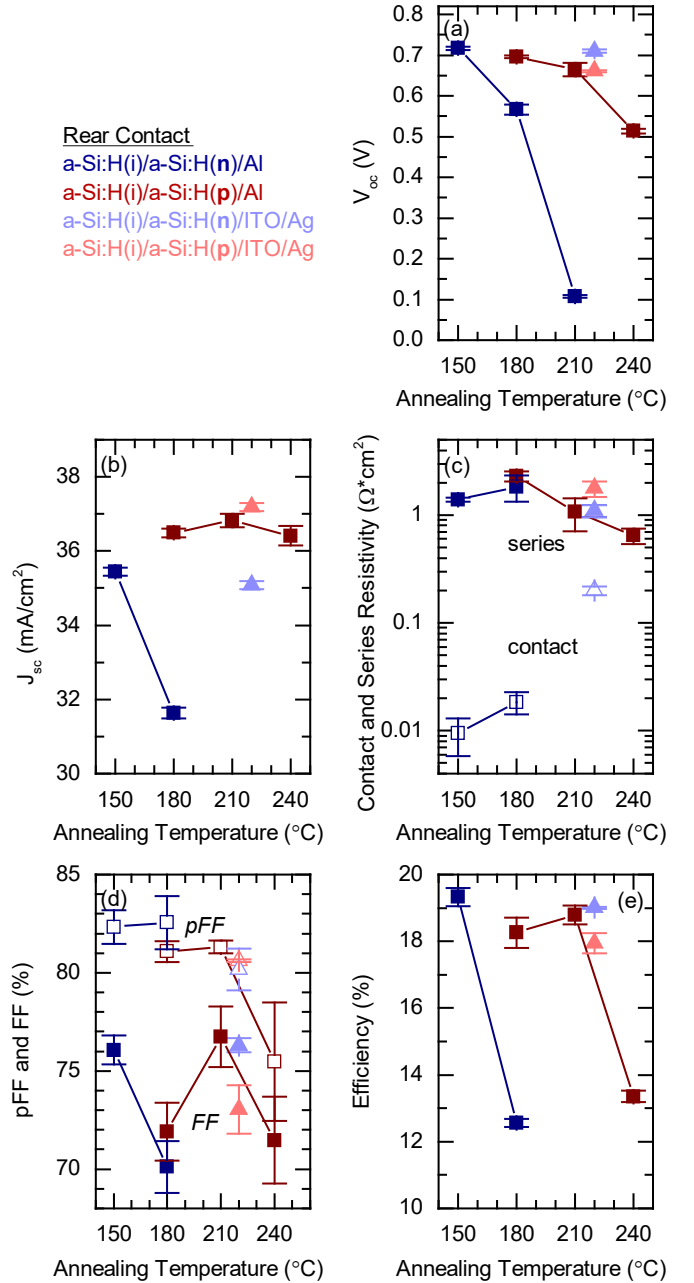


Fig. 4. (a) V_{oc} , (b) J_{sc} , (c) contact and series resistivity, (d) pFF and FF , and (e) efficiency of SHJ solar cells with either Al or ITO/Ag metallization to rear n- or p-type a-Si:H layers.

the rear Al layer will be essential for the best cell performance; fortunately, inserting a low-refractive-index dielectric film between the a-Si:H layers and rear metal has been shown to effectively reflect infrared light and has been demonstrated in SHJ cells [32, 33].

Figure 4c and 4d shows the resistivities and FF of the cells, respectively. In the TLM structures (which were possible only for the cells with electron contacts at the rear), the contact resistivity was more than an order of magnitude lower for the Al-metallized samples, as predicted in Figure 3a. However, the Al-metallized cell did not exhibit superior series resistivity or FF . A significant contributing factor is the line resistance of the front Ag paste, which has a manufacturer's recommended curing temperature of 200 °C. The line resistivity for these cells annealed at 150, 180, and 210 °C were 3.0, 0.85, and 0.6 Ω/cm , respectively. For a 2 cm $\times$ 2 cm cell with 8 fingers, each separated by 2/7 cm, increasing line resistivity from 0.6 to 3.0 Ω/cm results in an increase in series resistivity from 0.12 to 0.61 $\Omega\cdot\text{cm}^2$, according to the analysis by Meier [34]. Thus, the low annealing temperatures to optimize the Al-metallized contacts must be considered with subsequent processing, and plating, for example, may be more compatible than screen-printed front fingers. The efficiency of the devices is shown in Figure 4e. Overall, the devices exhibited the expected behavior based on the electrical test structures, and demonstrated performance on par with the ITO/Ag reference devices. The best performing cell with a-Si:H(i)/a-Si:H(n)/Al rear contact had $V_{oc} = 722$ mV while simultaneously achieving $\rho_c = 9.4$ $\text{m}\Omega\cdot\text{cm}^2$.

D. STEM and EDXS

Since these test structures and full devices exhibited an extremely wide range of performance, we examined the contacts using STEM and EDXS or EELS. We begin with the a-Si:H(i)/a-Si:H(n)/Al electron contacts. Figure 5a shows the contact annealed at 150 °C; it exhibits a smooth a-Si:H(n)/Al interface with seemingly no interdiffusion. This sample was extracted from the best Al-metallized cell, which had high V_{oc} and low ρ_c .

Figure 5b shows significant diffusion of Al into the underlying a-Si:H(i)/a-Si:H(n) stack at 180 °C. The interdiffusion process in Al-induced crystallization and layer exchange initiates at the a-Si:H/Al interface due to mobile free electrons in Al screening Si-Si covalent bonds, creating approximately two monolayers of highly mobile, or free, Si atoms [35]. Similarly, bond screening from Al is believed to weaken Si-H bonds in a-Si:H(i)/Al stacks, causing hydrogen effusion at temperatures below 150 °C [36]. Thus, sufficiently thick Al adjacent to Si-Si and Si-H bonds increases the density of free Si atoms and Si dangling bonds, which, combined, facilitate extensive atomic rearrangement. The mobile Si atoms at or near the a-Si:H/Al interface typically find an energetically favorable position by wetting the grain boundaries of the polycrystalline Al film [35]. However, as Al enters the a-Si:H film at rapid rates and high concentrations, the free Si atoms deeper in the a-Si:H film likely lose access to these grain boundaries and a meta-stable Al-Si mixed phase forms. This composition is unable to provide the same degree of c-Si

surface passivation due to hydrogen loss, recombination losses in the Al-rich contact, and, likely, Al reaching the c-Si wafer in some areas. Together, these mechanisms are responsible for the low V_{oc} (563 mV) of this cell. This semi-metallic structure is, however, highly conductive, as observed in the TLM test structures and in comparable contact structures from prior work [29, 37]. During annealing, as Al enters the a-Si:H film in high concentrations and disrupts the a-Si:H bonding, we expect there to be a significant amount of free Si atoms. When these atoms

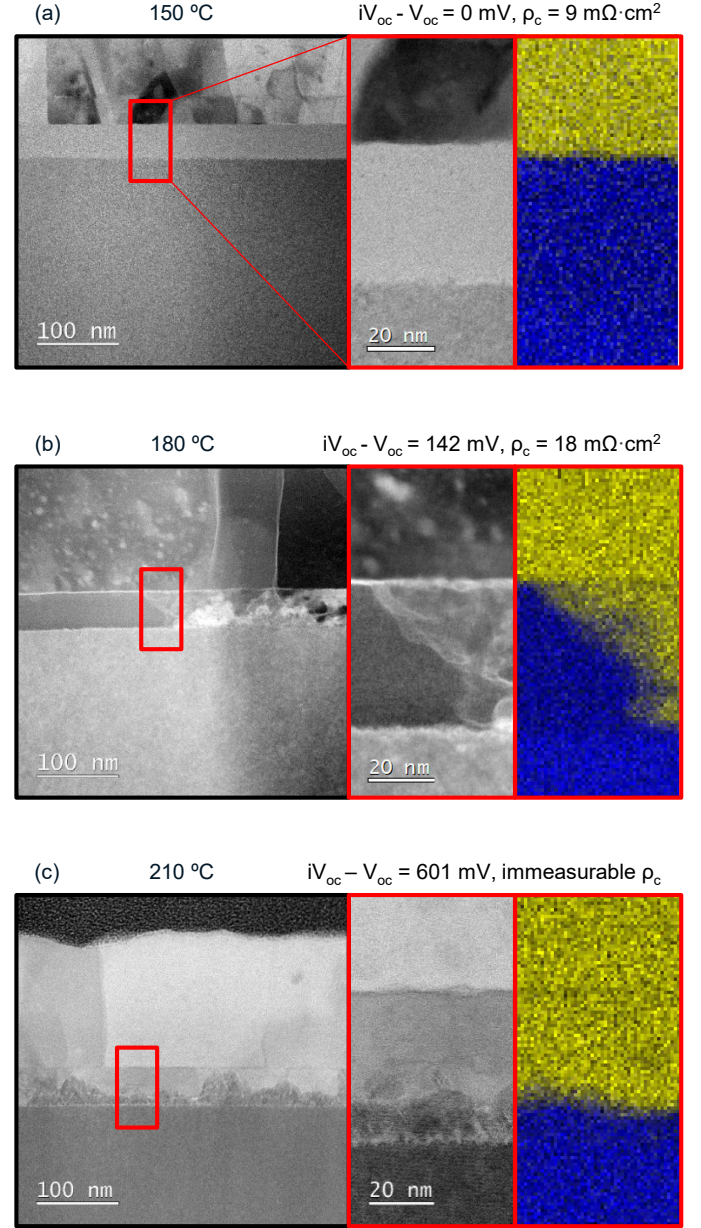


Fig. 5. Low-magnification STEM cross-section, high-magnification STEM cross-section, and complementary EDXS or EELS map for a-Si:H(i)/a-Si:H(n)/Al contacts annealed at (a) 150 °C, (b) 180 °C, and (c) 210 °C. Also shown are the difference between the cell V_{oc} and the iV_{oc} of the initially passivated wafer, and the contact resistance from TLM.

exceed a critical thickness, based on the surrounding interfaces, crystallization becomes an energetically favorable process [35].

Figure 5c, of the cell annealed at 210 °C, shows Si crystallization commencing at the c-Si wafer surface below a predominantly Al-rich layer. The directionality of the crystallized lattice within the former a-Si:H layer matches that of the substrate, indicating that the c-Si substrate has provided an energetically favorable site for epitaxial nucleation. This cell had a V_{oc} of 108 mV and the corresponding TLM structures had immeasurable contact resistance, which is evidence that, during the crystallization process, Al was incorporated into the Si lattice as a p-type dopant, as similarly observed by Haque *et al.* [19]. Given the high concentration of Al diffusion into the a-Si:H(i)/a-Si:H(n) stack and the Si crystallization far below the amorphous crystallization temperature, we hypothesize that covalent bond screening and the resultant hydrogen effusion and Si dissociation are major factors induced by Al in these electron contacts. Given the relatively low concentration of weakly bound higher hydrides in a-Si:H(i)/a-Si:H(n) stacks, thermally induced hydrogen effusion in the absence of Al bond screening is not expected to be a significant factor, as marginal hydrogen effusion occurs below 210 °C [38, 39].

We turn now to the a-Si:H(i)/a-Si:H(p)/Al hole contacts. In contrast to the a-Si:H(n)/Al interface, the a-Si:H(p)/Al interface annealed at 180 °C appears sharp, with seemingly minimal to no interdiffusion, as shown in Figure 6a. This translated to a 12 mV loss relative to the iV_{oc} of the pre-metallized passivated wafers, and to higher V_{oc} than all ITO/Ag reference cells. We hypothesize that, rather than rapidly dissociating the Si and entering the a-Si:H, as for the a-Si:H(n) layer, Al diffuses at low temperatures in accordance with its ability to enter the a-Si:H(p) film as an active acceptor dopant. Near-UV photoelectron spectroscopy performed by Stang *et al.* indicated a 50 meV downward shift in the Fermi level of an a-Si:H(i)/a-Si:H(p)/Al contact when annealed at 150 °C, which was attributed to Al occupying acceptor positions [8]. Konishi *et al.* performed secondary ion mass spectrometry (SIMS) on c-Si/a-Si:H(i)/a-Si:H(p)/Al structures annealed at 150 and 200 °C for 30 minutes. The results showed no Al in the a-Si:H(i) layer after the 150 °C anneal and a concentration of $5.9 \cdot 10^{18}/\text{cm}^3$ at the c-Si wafer surface after the 200 °C anneal [9]. In the 180 °C sample here, we do not directly observe Al interaction in STEM or EDXS, which has a detection limit of about 1%, corresponding to a concentration of approximately $4.9 \cdot 10^{20} \text{ cm}^{-3}$ in a-Si:H [40]. Though, dopant-level concentrations of Al are not detectable, we do expect a modest level of p-type dopant incorporation, resulting in the cell maintaining good performance.

Figure 6b shows the a-Si:H(i)/a-Si:H(p)/Al contact annealed at 210 °C. We observe Al signal from EDXS only at the very top of the a-Si:H(p) film. In the high-magnification STEM image, we observe visible roughening at the c-Si/a-Si:H(i) interface, though it is not apparent what is causing this. One possibility is that dopant-level concentrations of Al have already been introduced throughout the a-Si:H(p) film (as active dopants) and the Al continues to diffuse through the a-Si:H(i) layer. As we have seen, Al diffuses more rapidly through intrinsic and n-type a-Si:H compared to p-type. Al could be diffusing through the a-Si:H(i) and reaching the wafer

in smaller concentrations, causing some perturbation to the passivation ($iV_{oc} - V_{oc} = 43 \text{ mV}$).

Heavy Al diffusion into a-Si:H(p) does not occur until 240 °C, as shown in Figure 6c. Given the high concentration of higher hydrides in a-Si:H(i)/a-Si:H(p) stacks, some hydrogen effusion is expected at 210 °C [38, 39], but the effusion rates measured by De Wolf *et al.* show a significant increase between 210 and 240 °C. This is likely a major driver for the higher Al diffusion into the a-Si:H(p) layer at this higher temperature:

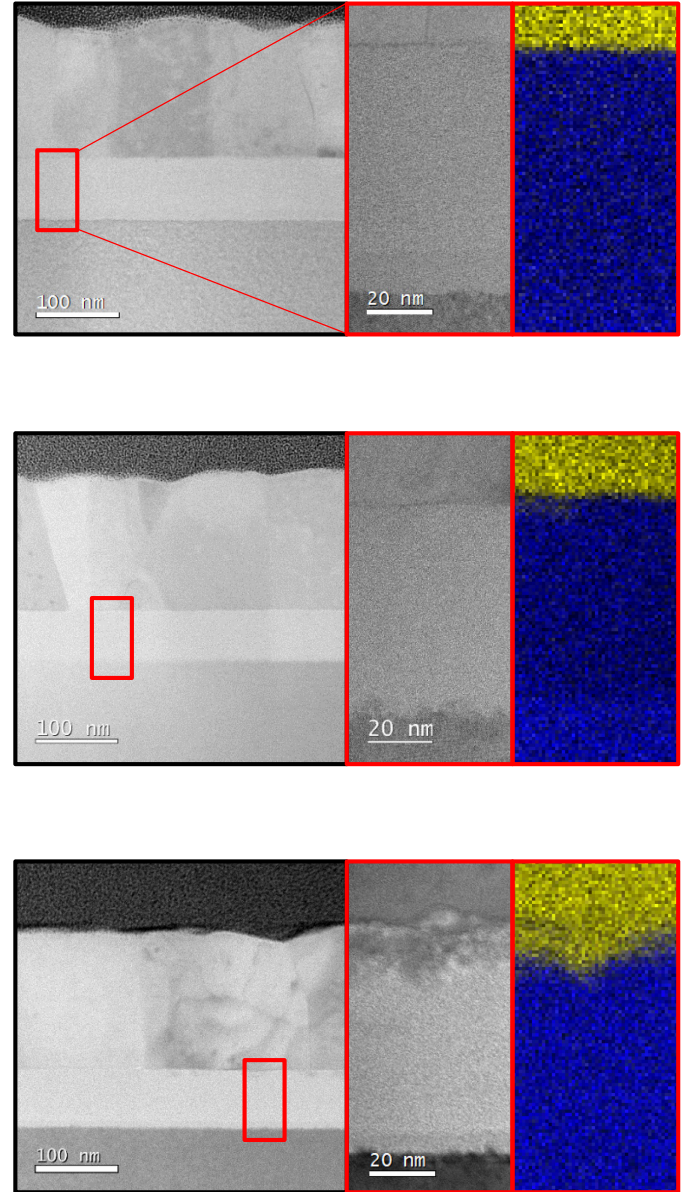


Fig. 6. Low-magnification STEM cross-section, high-magnification STEM cross-section, and complementary EDXS map for a-Si:H(i)/a-Si:H(p)/Al contacts annealed at (a) 180 °C, (b) 210 °C, and (c) 240 °C. Also shown are the difference between the cell V_{oc} and the iV_{oc} of the initially passivated wafer, and the cell's series resistance.

Hydrogen effusion from the thermal treatment significantly increases the density of dangling bonds, thereby providing

more energetically favorable pathways for Al diffusion. Further accelerating this process is the incorporation of Al as an active dopant within the a-Si:H(p) layer, which will drive the Fermi level closer toward the valence band, further increasing the hydrogen effusion rate by reducing the energetic barrier to bond rupture [38]. Thus, once this critical temperature is reached, multiple mechanisms self-propagate and facilitate alloy-level concentrations of Al diffusion into the a-Si:H(p) layer.

Finally, we note that growth-dependent structural properties and long-range disorder may also influence diffusion pathways. Diffusion through microstructural grain boundaries and microvoids has been linked to Al diffusion in prior work [41]. In the a-Si:H(i)/a-Si:H(n) stacks, the Al preferentially diffuses down to the c-Si wafer before moving laterally. On the other hand, Al seems to sweep more uniformly into a-Si:H(p).

IV. CONCLUSIONS

We have explored the properties of SHJ electron and hole contacts with direct Al metallization to a-Si:H(n/p) for a wide range of a-Si:H(n/p) thicknesses and annealing temperatures. Thicker (20–40 nm) a-Si:H layers metallized with Al and annealed at 150 °C (for n-type) and 180 °C (for p-type) preserve the wafer surface passivation and provide lower contact resistance than their ITO/Ag counterparts. Each contact polarity is sensitive to the processing conditions in different ways, and microscopic analysis of the contact stacks revealed that this behavior stems from a combination of hydrogen effusion, Al screening, and Al incorporation into the a-Si:H(n/p) layers.

When these contacts were implemented at the rear of solar cells, J_{sc} and efficiency predictably suffered—relative to ITO/Ag reference cells—due to higher rear parasitic absorption and higher front grid resistivity. However, these losses can be remedied with existing technologies: partial-area dielectric reflectors and low-temperature plating. A significant outstanding challenge for Al metallization to SHJ cells,

however, is expanding the processing window that yields excellent contact properties.

Although a-Si:H(i)/a-Si:H(n)/Al and a-Si:H(i)/a-Si:H(p)/Al contacts have different stability challenges with increasing annealing temperature, each type could benefit by buffering the onset of Al diffusion at its interface with the doped a-Si:H. This could be done by tuning the oxidation of the a-Si:H stack before Al deposition. This is a known approach to slow the interdiffusion process by increasing the Al-Si distance, but must be implemented in a way that does not become prohibitively resistive [42]. Another approach is to incorporate Si into the Al sputter target, which may reduce the driving force for Al diffusion into the a-Si:H layers and the strength of the Si-Si and Si-H bond screening compared to pure Al [43]. For the a-Si:H(i)/a-Si:H(n)/Al contact, a phosphine plasma before Al sputtering or deuterium treatment could increase the stability of the a-Si:H(n) layer and inhibit counter-doping [44, 45]. For the a-Si:H(i)/a-Si:H(p)/Al contact, more insight is needed into the Al diffusion mechanism and how this is impacting V_{oc} , but a diborane plasma on the a-Si:H(p) surface before Al metallization may sufficiently impede Al diffusion without compromising contact quality.

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