RSSI Amplifier Design for a Feature Extraction Technique to Detect Seizures with Analog Computing

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***Abstract*—Advances of machine learning algorithms have led to improvements of seizure detection capabilities in monitoring systems based on electroencephalography (EEG). Seizure detection hardware requires accurate feature extraction, which is conventionally done in the digital domain by extracting power in different EEG frequency bands over a particular time window. This paper presents an analog counterpart to digital feature extraction. A received signal strength indicator (RSSI) circuit is used for extracting EEG power features in the analog domain. A high-precision RSSI circuit was designed in the sub-threshold domain with ultra-low power consumption and low sensitivity to process-voltage-temperature variations with CMOS technology. Simulation results show that the RSSI circuit consumes 24 nW power, and has a dynamic range of 53 dB with a linearity error of $\pm$ 0.5 dB, sufficient to accurately extract features for seizure classification. The analysis of 16 hours of patient EEG data indicates a seizure classification accuracy of 94%, and a non-seizure classification of 86%.**

***Keywords*—Machine learning, analog computing, EEG-based seizure detection, support-vector machine, received signal strength indicator (RSSI), switched capacitor circuit.**

I. Introduction

Epilepsy is a neurological disorder that affects almost 2% of the world's population [1]. Epilepsy causes recurrent seizures which, apart from causing significant discomfort and poor quality of life for patients, can also lead to dangers of accidents, fall, and even death. An accurate treatment of epilepsy involves tracking and profiling of seizures to administer the correct medication. However, current treatment strategies, which include interviewing patients or keeping them in the hospital for a long period to capture a seizure episode, are either inaccurate or impractical [2]. For an accurate characterization of the onset of seizures, not only do we need to continuously monitor the EEG signals, but we also have to do it in an unobtrusive fashion such that the day to day activity of a patient is not affected.

A wearable device that can continuously monitor EEG outside of a hospital will suit this need. However, wearable devices can monitor EEG only for a limited duration due to the relatively high power consumption involved in EEG acquisition and processing. In recent years, several wearable devices and integrated circuit design methods have been introduced to acquire and process EEG signals [3]–[6]. Once the EEG signals have been acquired, the data can be used for the detection of seizures.

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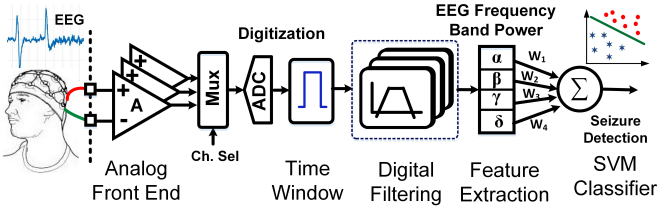

Fig. 1: Seizure classification overview of a conventional EEG processing system using a digital computing based SVM classifier.

Often, the raw EEG data is directly presented to a doctor. However, recent advances in machine learning have led to the development of seizure detection capability within EEG monitoring systems. Seizure onset detection involves the acquisition of EEG signals, and the extraction of features that show abnormal activity. Once features have been extracted, they can be fed to a linear support-vector machine (SVM) classifier to differentiate between seizure and non-seizure observations [7]–[9]. Fig. 1 shows the conventional system-on-chip (SoC) architecture for seizure detection. The processing chain consists of an analog front end (AFE) with relatively high power, followed by an analog-to-digital converter (ADC) and digital signal processing (DSP).

DSP requirements often dictate the SoC architecture, which can involve large memory requirements for data storage and digital filtering needs, significant computing infrastructure such as parallel multiplier and adders (for multiply and accumulate (MAC) operations [10]) and high fidelity data acquisition. Such SoCs using feature extraction and classification capabilities can consume power in the μW range and chip sizes up to $5mm^2$ [9], [11]. There is a need to enable seizure classification engines that can operate continuously from harvested energy with power consumption less than 100s of nW for state-of-the-art internet-of-things (IoT) sensors [12], [13]. In this paper, we present an ultra-low power (ULP) EEG classification system using an analog computing based feature extraction technique. The proposed solution overcomes the variability issues of analog computing to leverage its potential to realize an SVM classification engine with low area and power overhead.

II. Analog Computing Based Seizure Classifier

Analog computing incorporates vast amount of information processing per transistor to realize a few orders of magnitude higher power and area efficiency compared to digital computing [14]–[16]. Recently, an EEG monitoring device was reported that achieves a power consumption of 950 nW

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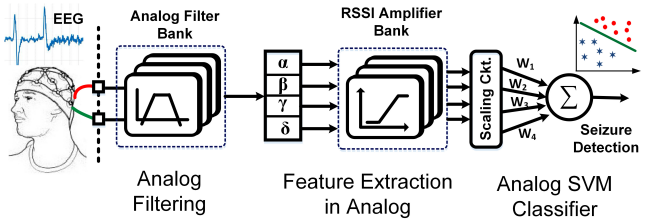


Fig. 2: Proposed seizure classification technique for an EEG system using analog computing based SVM classifier.

by employing an analog feature extraction technique [17]. We propose an analog feature extraction technique that will significantly reduce the power consumption and area of an EEG classification engine. Fig. 2 shows the architecture of our proposed EEG system using analog computing based feature extraction and classification engine.

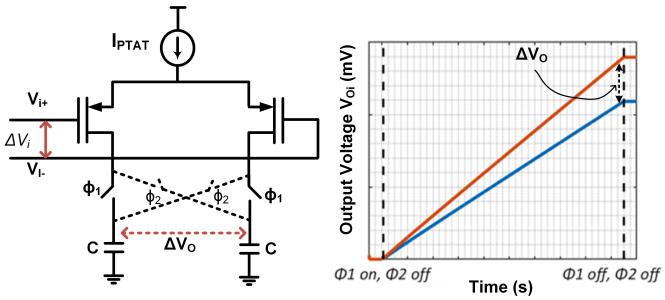
The accuracy of seizure classification depends on the features being fed to the SVM Classifier. Typically, EEG signals are studied by dividing the EEG power spectra in different frequency bands (called delta (δ), theta (θ), alpha (α), beta (β), and gamma (γ)). Each spectral band exhibits characteristic patterns based on the level of consciousness, external stimuli, and other neural responses. Disorders such as epilepsy can alter the power spectrum of the EEG frequency bands [18]–[20]. Conventionally, the energy in different EEG frequency bands is used as a feature for classification. EEG data from all channels is sent through a filter bank consisting of 5 to 7 bandpass filters. Energy in each spectral band is calculated for a given time window, and a feature vector is formed [7], [8].

We propose to extract features, i.e. the power in EEG spectral bands, using analog based received signal strength indicator (RSSI) circuit as detailed in Fig. 2 to present to the classifier. RSSI circuit consists of several cascaded differential amplifier stages to constitute a cascaded limiting amplifier structure to realize a logarithmic amplifier [21]. This circuit, therefore, provides the power level of an incoming signal in analog. The RSSI circuit can consume a small amount of power when biased in the sub-threshold domain. Further, a high accuracy sub-threshold based constant g_m biasing technique can be leveraged to limit process, voltage, and temperature (PVT) variations [22].

We establish the viability of the analog RSSI-based feature extraction by utilizing it to detect the onset of seizures in patient EEG data. A MATLAB model of the RSSI transfer function is used to provide a feature vector to a linear SVM classifier. Analysis of 16 hours of patient EEG data shows a seizure classification accuracy of 94%, and a non-seizure classification of 86%. The following sections explain the design and simulation results of the proposed RSSI amplifier.

III. Analog Computing Circuits

The RSSI circuit is composed of a series of cascaded limiting amplifiers. In this paper, we use a switched capacitor differential amplifier (diff-amp) as the limiting amplifier for the RSSI circuit. Six such diff-amps are cascaded to realize enough gain and linearity for the RSSI. Typically, the amplitude of EEG signal is from a few μV to 100s of μV [23]. The



(a) Switched Capacitor Diff-amp Offset Correction

(b) Simulation Result of the Diff-amp

Fig. 3: Switched capacitor differential amplifier circuit with its simulation results.

dynamic range of RSSI circuit should be over 40 dB to meet the EEG signal variation [11]. Further, the AFE and filters will provide additional gain to set the minimum input voltage for RSSI around 0.25mV. We also achieve low linearity error ($\pm$ 0.5 dB) in RSSI to realize accurate classification results.

A. Switched Capacitor Differential Amplifier

ULP differential amplifiers with nano-amp bias current cannot use a resistive load due to unrealizable resistor values needed (100s of MΩ). For this reason, we use a switched capacitor load to emulate a resistor. A large resistor can be emulated with a small capacitor. Fig. 3(a) shows the circuit architecture of our diff-amp circuit that utilizes capacitor C as the load. This circuit operates in the following manner: The capacitor is at reset before t=0 with it being discharged to ground. When input voltage ΔV_i is applied, the load capacitors will start charging. However due to differential input voltage, each capacitor will charge with different current, and the output voltage after time t=T_{ON} will be given by

$$\Delta V_O = \Delta V_i \frac{g_m T_{ON}}{C} \tag{1}$$

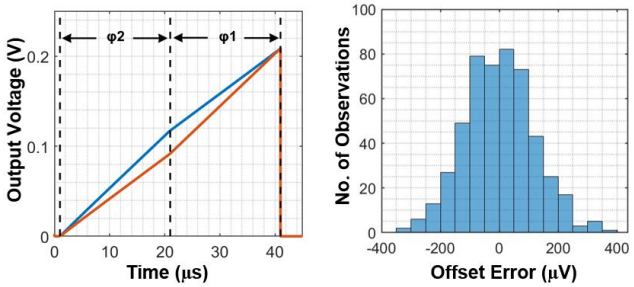
Equation 1 reveals that the desired resistor can be realized using the capacitor C and time T_{ON} with R=T_{ON}/C. Further, the diff-amps are designed to be PVT invariant. To that end, the input transistors are operated in the sub-threshold region, and are biased with a PTAT (proportional to absolute temperature) current source. This ensures that the transconductance of the input transistors is constant:

$$g_m = \frac{I_{PTAT}}{\eta V_t} \tag{2}$$

With this biasing configuration, the PTV variation of the diff-amp can be reduced significantly. The only process dependent component that remains in the circuit's operation is C. However, the effect of C can also be minimized if the PTAT current reference is realized using a switched capacitor bias [22]. Consequently, the diff-amp exhibits a very small gain variation. We designed our diff-amp to have a gain of 2.57 with a T_{ON} of 20 μs with a load cap of 1 pF.

B. Offset Correction

The precision of the amplifier circuit is affected by the offset arising from device mismatches. Since the output of each diff-amp stage is fed as input to the next stage in the RSSI circuit,



(a) Offset Correction Waveform (b) Mismatch Simulation with Offset Correction

Fig. 4: Offset correction waveform and error simulation.

the error introduced by offset grows exponentially with the number of stages. The error at the RSSI output is

$$\Delta V_{OUT,err} = \sum_{i=1}^{6} k^i (V_{OS}) \tag{3}$$

where $k = g_m T_{ON}/C$ is the gain of the amplifier, and V_{OS} is the offset of the amplifier. Hence, an offset correction technique is needed to ensure precision of the RSSI output. Figure 3 also includes an offset cancellation technique that is implemented in the differential amplifier stage by adding phase ϕ_2. If no input signal is applied in phase ϕ_2, then the voltage on the load capacitors at the end of phase ϕ_2 is

$$\Delta V_O = \frac{g_m T_{ON}}{C}(V_{OS}) \tag{4}$$

In the next phase ϕ_1, normal operation is resumed. The load voltage of the capacitors with inputs reversed is now given by,

$$\Delta V_O = \frac{g_m T_{ON}}{C}(-V_{OS}) \tag{5}$$

which is added to the voltage given by (4), hence cancelling the offset.

Fig. 4(a) shows the simulated output voltage in phase ϕ_2 and ϕ_1 when an offset of $10mV$ is introduced at the input. At the end of phase ϕ_1, the difference in the output voltage is reduced to $250\mu V$, suppressing the input offset by 32dB.

Functionality of the offset cancellation circuit was tested by running Monte Carlo mismatch simulations with zero input. Fig 4(b) shows the output voltage at the end of phase ϕ_1. The 3σ error was found to be $351\mu V$.

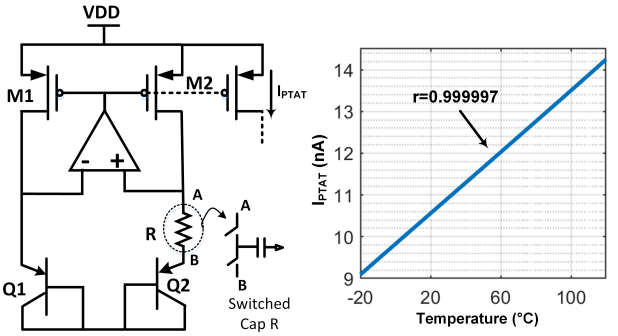
C. Current Source

We explained in Section III.A that the differential amplifier's input transistors are biased to obtain a constant g_m. This is achieved by biasing them with a PTAT current source, shown in Fig. 5. A conventional BJT based current source was modified to replace the poly resistor with a switched capacitor based resistor (SCR). Since capacitors are less prone to variations with process and temperature, the PTAT current obtained is very linear. The SCR resistance is given by,

$$R = \frac{1}{f_1 C_1} \tag{6}$$

where f_1 is the reference clock frequency. The PTAT current is given by,

$$I_{PTAT} = V_T ln(K) f_1 C_1 \tag{7}$$



(a) PTAT Current Source (b) Simulation of Temperature Variation of Current Source

Fig. 5: PTAT Current Source and its simulation with temperature.

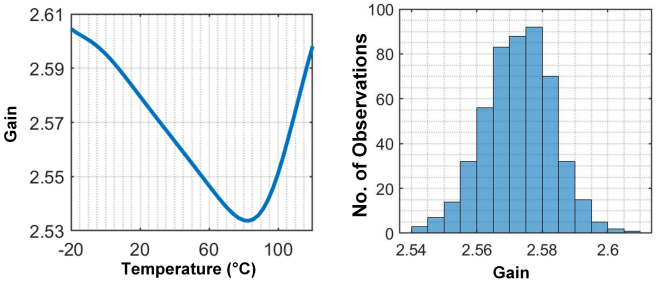
It can be seen that the gain of the diff-amp will be constant with the above biasing configuration using equations 1 and 2. We simulated our proposed diff-amp circuit. Fig. 6(a) shows the variation of the gain with temperature for a range of -20^oC to 120^oC. The temperature variation of the gain of the single stage differential amplifier is 2.88%. The temperature variation of the gain is increased due to non-idealities of switches ϕ_1.

The parasitic capacitances of the switch cause the current through the switches to increase slowly when it is switched on. This introduces an error in the output voltage. Small switches are designed to reduce the effect of parasitic capacitances. Another source of error is charge sharing due to switches ϕ_1 and ϕ_2 switching simultaneously. A small 'dead' time of 1 μs is introduced to reduce error due to charge sharing. Fig 6(b) shows the gain variation with process variability. The 3σ variation is found to be 0.033 for an average gain of 2.57.

IV. RSSI Circuit Architecture

The RSSI circuit is composed of six diff-amps cascaded together as shown in Fig. 7. The first differential amplifier provides an output after time T_{ON}, after which the second differential amplifier is enabled. Similarly, amplifier A_3 is enabled after time $2T_{ON}$, and the output at the end of amplifier A_6 is obtained after $6T_{ON}$. The output of each stage is collected on the capacitors of the differential amplifiers. These output capacitors are then connected in parallel at the end of $6T_{ON}$ to sum the outputs of each stage. The RSSI output voltage corresponding to the signal strength can be given as,

$$V_{RSSI} = \frac{1}{6}\sum_{i=1}^{6} \Delta V_{Oi} \tag{8}$$



(a) simulation of gain with temperature variation (b) Simulation of gain with process variation

Fig. 6: Process and temperature variation of the diff-amp gain.

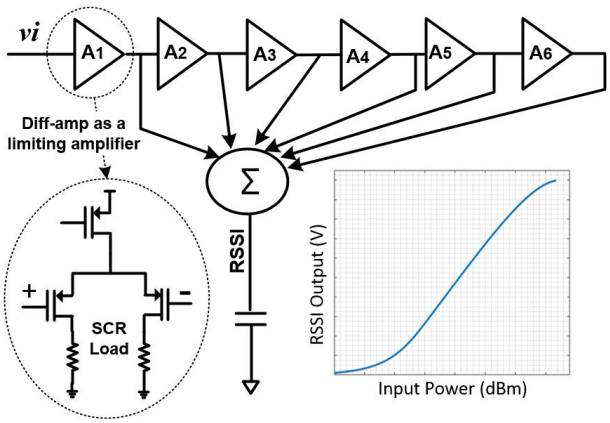


Fig. 7: Circuit architecture and operation of the RSSI.

The amplitude of EEG signals can vary greatly between seizure and non-seizure activity, and from patient to patient. Thus, the RSSI circuit requires an adequate dynamic range to process these signals which depends on the gain and number of stages of the amplifiers cascaded together.

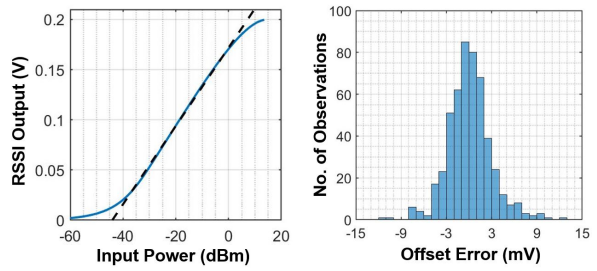
V. Simulation Results

Fig. 8(a) shows the RSSI output waveform with varying levels of input power. The dynamic range achieved is 53 dB, which enables the RSSI circuit to detect an input signal level of 250 μV. Apart from the voltage compression at both ends, the maximum error observed is ± 0.5 dB for the linear range. High linearity is achieved in this architecture because the outputs at every stage are summed together, regardless of the input power. This improves the linearity in comparison to conventional architectures, where the amplifiers that are not saturated introduce an error [21].

The output error of the complete RSSI circuit was estimated with the help of Monte Carlo simulations. Fig. 8(b) shows that the 3σ variation after 500 runs is $9mV$. The total power consumption was found to be $24nW$. The amplifiers are turned on only for the duration of T_{ON}, thus saving power. Table I lists the simulated performance metrics in comparison to other state-of-the art RSSI circuits.

VI. Feature Extraction with RSSI Blocks

The proposed RSSI circuit was used for a seizure detection application using EEG data [28]. The complete analog front-end, along with the RSSI circuit was modelled in MATLAB



(a) RSSI Output and its Linearity Performance

(b) Mismatch Simulation without Input

Fig. 8: Linearity and mismatch performance of the RSSI circuit.

TABLE I: PERFORMANCE COMPARISON

	This work	[24]	[25]	[26]	[27]	[21]
Process	65 nm	180 nm	600 nm	65 nm	350 nm	350 nm
VDD (V)	1	1.8	2	1 or 3	3	2
Dynamic Range (dB)	53	70	75	60	80	65
Power	24 nW	20 mW	6.2 mW	8 mW	5mA-13mA	2.2 mW
Linearity Error (dB)	$\pm$0.5	$\leq$1	$\leq$1	$\leq$1	$\pm$ 0.7	$\pm$0.7
Settling Time (μs)	120	20	N/A	N/A	N/A	N/A

to extract features for the detection of seizure onsets. As visualized in Fig. 2, the front end consists of a bank of analog bandpass filters to split the incoming EEG data into four different frequency bands. The filters provide a gain of 30 dB, and the output signals are provided to the bank of RSSI amplifiers to obtain the signal strength in each frequency band.

The RSSI circuit was modelled as a moving RMS function followed by the transfer function of the RSSI. Data from 23 EEG channels, acquired over 16 hours was provided to the linear SVM classifier. A classification accuracy of 94% and 86% were obtained for classifying the seizures and non-seizures respectively.

Table II compares the proposed RSSI based feature extraction (FE) technique with other reported works. Here, we focus on the performance of our computing circuit compared to the computing circuits of other works. The power consumption of the peripheral circuits such as the AFE and ADC is removed, and only the computing power consumption is compared. Since the RSSI circuit consumes a power of 24 nW, we can achieve a lower power of 96 nW per channel while dividing the EEG signal into four frequency bands for FE. The proposed approach has a classification accuracy comparable to other reported works.

TABLE II: FEATURE EXTRACTION PARAMETERS

	This work*	[11]	[8]	[29]	[30]
FE Power (μW/Channel)	0.096	0.48	100	7	33
% of Seizure Detected	94%	98.5%	84.4%	95.1%	96%
False Postive Rate	14%	4.4/hour	4.5%	0.94%	0.15/hour
# of Channel Used	23	8	8	8	18

$*$ *Simulation based results*

VII. Conclusion

The paper presented an analog alternative to conventional feature extraction. Analog feature extraction was performed based on the model of an RSSI circuit to extract signal strength in the incoming EEG frequency bands. The RSSI circuit was designed by cascading differential amplifiers with switched capacitor loads to reduce the effects of PVT variations. A low-power, high-linearity RSSI circuit consuming 24 nW power and 53 dB dynamic range was designed and simulated.

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