A High Efficiency DC-DC Converter Architecture with Adjustable Switching Frequency to Suppress Noise Injection in RF Receiver Front-Ends

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***Abstract*—This paper presents a high efficiency DC-DC converter architecture with adjustable switching frequency to suppress the baseband noise from a power supply for an RF receiver front-end. The system is composed of a boost converter operating in a discontinuous conduction mode (DCM), an analog frequency-to-voltage converter (FVC), and a digital control loop. To prevent the switching noise of the power supply from mixing into the intermediate frequency (IF) signal band of the mixer, the FVC senses the switching frequency of a boost converter and compares it with a reference baseband frequency. The digital control scheme changes the switching frequency of the boost converter if it is close to the baseband frequency by increasing the bias current of the regulating comparator. The complete system has been designed in a 0.13 μm CMOS process. The simulated efficiency of the boost converter is 84.5% with a 300mV input level. Its peak inductor current control has been designed for different input voltage conditions ranging from 50mV to 300mV. The output voltage of the boost converter is 1V with a 1.35% ripple. The converter was simulated with an RF mixer circuit as load, where the mixer achieved an SFDR of 60.3 dB.**

***Index Terms*—DC-DC converter, boost converter, frequency-to-voltage converter, RF receiver front-end, mixer.**

I. INTRODUCTION

The number of connected Internet of Things (IoT) devices is continuing to grow in our environment and living space. A significant percentage of IoT devices operate at ultra-low power (ULP) levels, either using harvested energy or a small battery with the need to prolong the time between charges or replacements. Due to the limited amount of available energy, their ULP operation is an important system goal to realize. Energy harvesting techniques can help to achieve long lifetimes, but the system should be able to operate efficiently with a small amount of harvested energy and often from low voltages. Typically, the power management technique includes an energy harvester to harvest and store energy on a capacitor, which is followed by voltage regulators to supply the circuit blocks of the system [1]–[6]. In [4], authors have proposed a boost converter that can harvest energy down to a few nanowatts of input power. While the energy harvesting circuit often provides an unregulated storage voltage, regulated supply voltages are usually realized through low-dropout (LDO) regulators [7] or switching converters [1], [8].

LDOs are mostly used to power sensitive analog and radio frequency (RF) circuits because of their high power supply rejection ratio (PSRR) [9]- [10]. DC-DC converters on the other hand create switching noise, which will have a negative impact on the performance of sensitive analog circuits. However, DC-DC converters are now being considered to power ULP IoT systems-on-a-chip (SoCs) [8] because of their higher efficiencies when compared to LDOs. Fig. 1 visualizes IoT SoC operation with a DC-DC converter. This design approach is targeting applications in which the RF communication is periodically enabled, which ensures that the converter is able to aggregate sufficient energy from the energy harvesters (EHs) to be able to turn on the RF receiver front-end for a short burst. The system always sustains the basic functions such as maintaining time, reference voltages and currents, among other functions. The power management system should guarantee operation with high efficiency in both modes for a long system lifetime. A previous study of powering RF receiver front-end circuits [11] with a DC-DC converter revealed that the performance impacts are small for the low-noise amplifier (LNA) and baseband filter in terms of noise figure (NF) and signal-to-noise-and-distortion ratio (SNDR) respectively. However, the spurious free dynamic range (SFDR) of the mixer dropped by 14 dB due to the supply noise from the mixing of the switching noise of the supply and the signal, which captures the noise and distortion performance impacts.

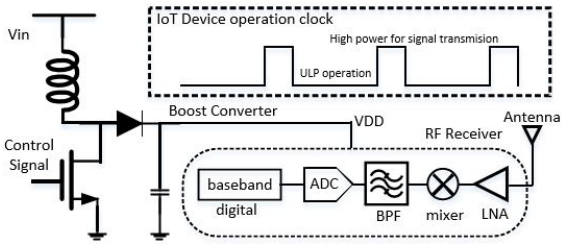

Fig. 1: Example IoT SoC powered by a DC-DC converter.

In this paper, we present a boost converter architecture that can reduce switching noise injection by changing its switching frequency. The associated power management system includes a boost converter operating in DCM, FVC and a digital control loop. The system is capable of providing a stable 1V supply for RF receiver front-ends with very low performance impact. The system architecture is introduced and analyzed in Section II, whereas individual circuit components are explained in Section III. Simulation results are discussed in Section IV, and a conclusion is provided in Section V.

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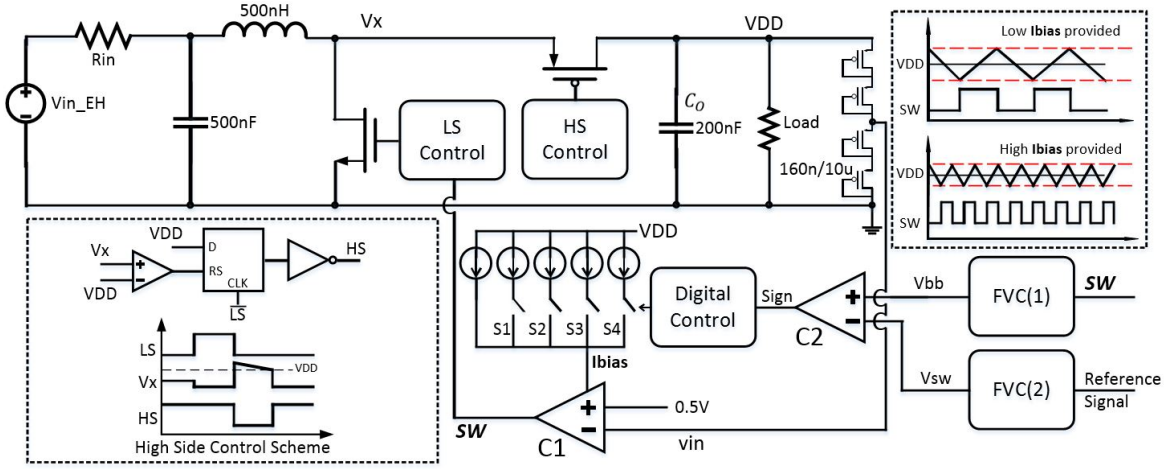


Fig. 2: Overview diagram of the power management system.

II. SYSTEM DESCRIPTION

Fig. 2 displays the system in which the boost converter operates in DCM with inductor peak current control and a zero detection techniques similar to the work presented in [12]-[13], a FVC [14] and digital control blocks. In this work, a power management unit (PMU) with lower noise impact has been developed for RF receiver front-ends, which utilizes a control loop to sense the switching frequency of the supply and shift it up to a higher frequency if it is within the band of interest.

Fig. 2 shows that the output voltage (VDD) of the boost converter is regulated at 1V to supply all other components. The minimum input voltage that the boost converter can harvest from is 50 mV. The simulated efficiencies of the boost converter at 50 mV and 300 mV input voltage are 56.7% and 84.5%, respectively. Additional digital calibration can improve the efficiency to 64% for a 50 mV input. We chose low input voltages for our analysis as they are close to realistic voltages obtained from EHs. More design details are provided in the Section III.

The comparator C1 performs the monitoring task for regulation, and its schematic is shown in Fig. 3. It consists of a two-stage amplifier and an output buffer stage. S1 to S4 are the switches that are controlled by the digital control blocks to adjust the biasing of the comparator. The following theoretical analysis proves the relationship between the switching frequency and the bias current. T_{OFF} is the output transition time, when the output changes to low as shown in Fig. 3, and

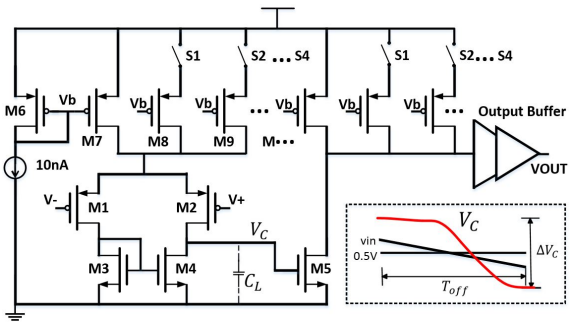
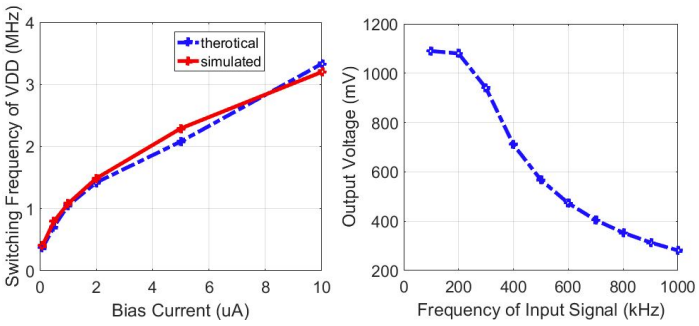


Fig. 3: Output voltage monitoring comparator (C1).



(a) (b)

Fig. 4: (a) Bias current of the output monitoring comparator (C1) vs. switching frequency of the output voltage, (b) characteristics of the frequency-to-voltage converter.

it determines the switching frequency of the converter. C_L is the parasitic capacitance seen at the output of the first stage. The output current charging C_L due to the differential input voltage can be given as:

$$\Delta i_c = g_m \times \Delta v_{in} \tag{1}$$

where g_m is the transconductance of the first stage, and v_{in} is the voltage at the input of the comparator. The above relationship can be rewritten as:

$$\frac{di_c}{dt} = g_m \times \frac{dv_{in}}{dt} \tag{2}$$

Recall that the equation for the capacitor C_L is given as:

$$i_c = C_L \frac{dv_c}{dt} \tag{3}$$

Combining (2) and (3), we can obtain

$$\frac{d}{dt}\left(\frac{dv_c}{dt}\right) = \frac{dv_{in}}{dt}\left(\frac{g_m}{C_L}\right) = \frac{I_{Load}}{C_o}\frac{g_m}{C_L} \tag{4}$$

Note that the rate of change of v_{in} is the rate of change of VDD, which is determined by the load current (I_{Load}) and the output capacitor (C_o). Integrating (4) over T_{OFF}, we get:

$$\Delta V_C = \frac{g_m I_{Load}}{2C_L C_O}(T_{OFF})^2 + K(T_{OFF}) + C \tag{5}$$

where ΔV_C is the voltage swing needed to cause a state transiston of the comparator, as annotated in Fig.3. A similar

relationship can be obtained for rising time T_{ON}. Note that ΔV_C, C_L, C_O, I_{Load} and K are constant, while T_{OFF} is inversely proportional to the switching frequency and the g_m is linear with the bias current in sub-threshold. Therefore, while g_m increases, T_{OFF} will decrease for the same ΔV_C, which implies that the switching frequency increases. Fig. 4(a) shows the simulation results and the theoretical analysis of the boost converter with different comparator bias current under same output load conditions ($1.67mW$). The converter will operate with a ULP bias current of 10 nA for light load, and will use higher bias current during times of heavy load currents with noise reduction capability to maintain high efficiencies in both operating modes of an IoT device.

The FVC circuit (designed as in [14]) is used to continuously sense the switching frequency of the boost converter (f_{sw}), and FVC(1) is used to generate the reference voltage by transforming the reference frequency f_{ref}, which is the cut-off frequency of the band-pass filter. Their two output voltages, V_{bb} and V_{sw}, are compared to provide a logic flag as follows:

$$Sign = \begin{cases} 1, & f_{ref} \geq f_{sw} \\ 0, & f_{ref} < f_{sw} \end{cases} \tag{6}$$

If $Sign$ = 1, the digital control will turn one additional current source on, and more power is provided to the output monitoring comparator, which will speed up the switching activity of VDD. This loop will continue to increase the current until $Sign$ transitions to 0, which the control logic will maintain. We discuss it in details in Section III-C.

III. CIRCUIT DESIGN CONSIDERATIONS

A. Architecture of the boost converter

The low-voltage boost converter is designed to work in DCM. During the low-side (LS) switching cycle, the inductor current is charged to a peak current(I_{peak}); and is discharged to zero during the high-side (HS) switching cycle. Fig. 2 shows the illustration of the switching waveform. The efficiency analysis of the boost converter in DCM as presented in [12] shows that the peak inductor current for maximum efficiency is given by:

$$I_{P,max} = \left(\frac{6V_I(E_{ST} + E_{SW})}{LR_L}\right)^{\frac{1}{3}} \tag{7}$$

In the above equation, E_{ST} and E_{SW} stand for the static loss energy and switching loss energy. R_L is the on-resistance when the switch transistor is conducting. The peak inductor current should be well controlled with respect to V_I for achieving maximum efficiency regardless of the switching frequency of the converter. From an input voltage of 100 mV to 300 mV, the converter operates at maximum efficiency, while the efficiency reaches 56.7% when the input is 50 mV due to the mismatch of the peak inductor current. The efficiency can be improved by using digital calibration, which is done by tuning the capacitance in the LS control according to a look-up table for a given input voltage.

The high side (HS) control is designed with a zero detection technique to avoid reverse inductor current, which would cause extra power loss especially for high frequency synchronous regulators [12], [15]. A high performance comparator is required for the zero current detector (ZCD) to fulfill this goal. Apart from the LS and HS switching period, one more phase is introduced to compensate for the mismatch variation of the comparator design. Fig. 2 depicts the four serially diode-connected NMOS devices that are used to provide half of the output voltage for the monitoring comparator C1. A reference voltage of 500 mV is provided to the regulating comparator C1, such that the switching signal can apply the on/off signal (SW) to the LS control that can turn off the complete system if a zero is conveyed to regulate the output voltage at 1V. The off-chip switching inductor value is 500 nH and the off-chip output capacitor is 200 nF, allowing to achieve higher switching frequency, which is desirable to supply the RF receiver front-end. Similar configurations with off-chip components are presented in [16] and [17] as well.

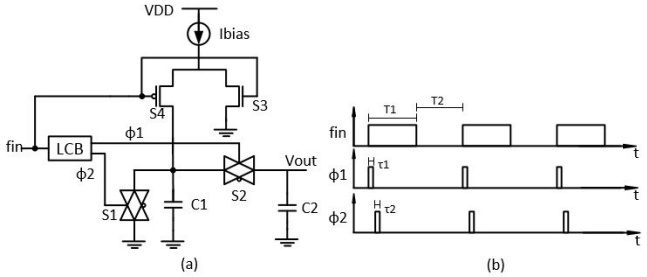


Fig. 5: Frequency-to-voltage converter: (a) block diagram, (b) timing diagram of the control signals.

B. Frequency-to-voltage converter

As introduced in [14], the relationship between the input frequency and output voltage is:

$$V_{out} = \frac{I_c}{C_1} T_1 = \frac{I_c}{C_1(2f)} \tag{8}$$

As presented in Fig. 5(b), T_1 is the time period for which the input signal is high, which is equal to $\frac{1}{2f}$ when the duty ratio of the input signal is 50%. A T (or "toggle") Flip Flop is used to divide the frequency to half of the actual frequency to maintain a 50% duty-cycle to remove error due to duty-cycle distortion. Fig. 4(b) shows the simulated FVC output voltage as its input frequency is varied. The power consumption of the FVC is 300 nW. The switching frequency (SW) is connected to the input of FVC(1) and the reference signal used at the input of FVC(2) has the same frequency as half of the bandwidth of the band-pass filter. We use a complex g_m-C filter whose architecture is similar to the one detailed in [18].

C. Digital control block

The digital control block was implemented in Verilog to sequentially turn on the switches (S1 to S4) according to (6) in order to determine how much current flows to the output monitoring comparator C1. Once $SIGN$ transitions to zero, the digital control scheme will stop and maintain the current state. This one-time calibration starts at the beginning of every

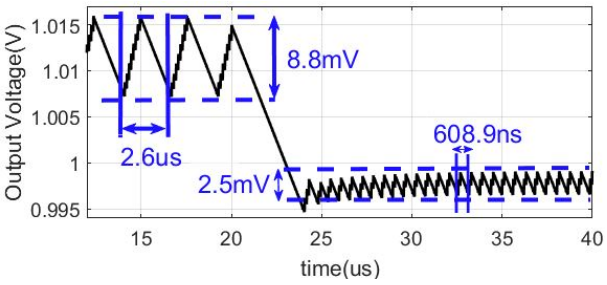


Fig. 6: Boost converter output voltage waveform.

signal transmission period, as indicated in Fig.1, to ensure that the supply noise does not interrupt the performance of the receiver. From the simulation results, the complete system including the mixer and the peripheral control circuits requires $637\mu W$, which is significantly lower than the maximum power that the converter can provide ($7.1\ mW$). Note that the efficiency is maintained at 80% under this light load condition. Each current source provides 1 μA of bias current to realize a significant change in switching frequency of the boost converter, and it was decided to use four switches because the additional 4 μA is sufficient for this system to reach a higher switching frequency than the bandwidth of the filter.

IV. SIMULATION RESULTS

The simulated output voltage of the boost converter with a 1 mW load is displayed in Fig. 6. After the low switching frequency (384 kHz) has been detected, which is within the band of interest, the switches are turned on to increase the bias current of comparator C1. As a result, the ripple decreases to 2.5 mV and the switching frequency increases to 1.64 MHz. A 13 mV voltage drop is seen at the output due to the offset in the comparator C1 caused by reduced output resistance. Down-conversion mixers show significant susceptibility to the inband supply noise [11], while other receiver blocks are more robust to switching noise of the supply voltage either due to their higher operating frequency (e.g., LNA), or due to high PSRR design (e.g., filter). In this section, a double-balanced active mixer based on the design in [19] is investigated in the presence of switching supply noise. For the simulations, the RF carrier frequency was at 1 GHz, and the intermediate frequency output at 10 MHz. The 1 MHz bandwidth of interest is annotated in Fig. 7. The simulated conversion gain is 11 dB, and the power consumption of this mixer is 560 μW.

To evaluate the impact of the DC-DC converter on the mixer in terms of SFDR, it was supplied by an ideal voltage source and by the boost converter that has been designed. The simulated output spectrum of the mixer and its SFDR were observed for comparison. the SFDR of the mixer with ideal supply is 62.9 dB. When the boost converter is operating at the ULP level with only 10 nA bias current for the monitoring comparator, the SFDR falls to 20.5 dB [Fig. 7(b)] due to the harmonics of switching supply noise, which is around 160 kHz. This inband noise cannot be filtered out by the downstream band-pass filter. After activating the system during simulation, it automatically detects the low switching

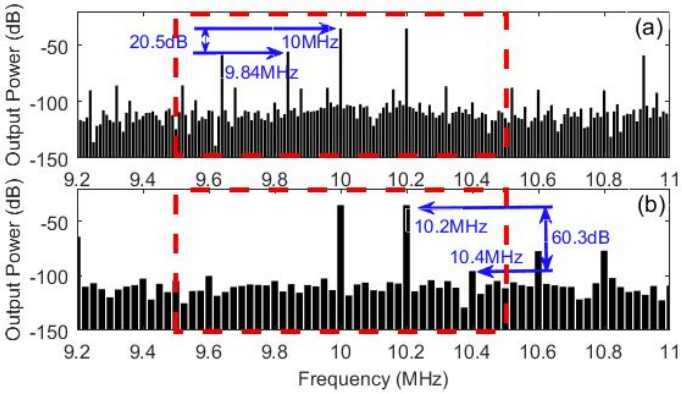


Fig. 7: SFDR of the mixer supplied by the boost converter (a) with 10 nA bias current, (b) with 4 μA bias current.

frequency and increases the bias current to 4 μA. Fig. 7(c) reveals that the SFDR of the mixer improves to 60.3 dB in the final state, representing a high SFDR level. A more than 40 dB of noise spur suppression is realized using the proposed technique, indicating the boost converter feasibility as the voltage supply for RF receiver front-ends. Table I compares the simulated boost converter design from this work with the state-of-the-art. The simulated peak efficiency and switching frequency of this work are comparable with the results in [12] and [20], where it should be considered during the comparison that both of these are measured results.

TABLE I: PERFORMANCE COMPARISON

	This work$*$	**JSSC'15** [12]	**JSSC'16** [21]	**ISCAS'18** [22]	**CICC'19** [20]
Process	$130nm$	$130nm$	$130nm$	$180nm$	$180nm$
Efficiency @ Min Input Voltage	56.7% $@50mV$	53% $@20mV$	58% $@70mV$	29% $@50mV$	77% $@20mV$
Output Voltage	$1V$	$0.9V$	$1.25V$	$1V$ to $1.6V$	$1.2V$
Switching Frequency	$100kHz-3MHz$	–	$0.2MHz$	–	$25kHz$
Peak Efficiency	84.5% $@300mV$	83% $@300mV$	83% $@300mV$	60%	82%
RF Noise Suppression	YES	NO	NO	NO	NO

$*$ *Simulation results*

V. CONCLUSION

A power management system for supplying RF receiver front-end circuits has been introduced. To avoid the interference of the supply noise with the desired intermediate frequency signal, FVCs and control circuits were designed for digitally-assisted operation. The presented approach involves the dynamic shifting of the converter switching frequency up to a high out-of-band frequency, such that the supply noise components can be filtered out by the downstream filter. A mixer was simulated together with the power management system because of its known sensitivity to switching noise on the voltage supply. The results demonstrated that the system improved SFDR reduction due to the noisy supply from 42.4 dB to only 2.6 dB. The simulated efficiency of the boost converter is 84.5% at 300 mV input voltage, which is realized with high switching frequency to suppress noise.

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