Multiscale Simulation of Ferroelectric Tunnel Junction Memory Enabled by van der Waals Heterojunction: Comparison to Experiment and Performance Projection

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Abstract — Atomically thin van der Waals (vdW) heterojunctions are investigated for ferroelectric tunnel junction (FTJ) device application by combining multiscale simulations from atomistic *ab initio* to quantum transport device simulations with experimental studies. The simulation reveals that low quantum capacitance of graphene, weak electronic hybridization of vdW bonds, and high interface quality free of dangling bonds can lead to extremely large vdW interface barrier height modulation at the graphene-CuInP$_2$S$_6$ ferroelectric (FE) interface. As a result, the simulated and experimental I-V characteristics show an unprecedented large tunneling electroresistance ratio. The vdW ferroelectric CIPS material further permits the tunneling barrier to be scaled down to atomic thickness. Quantum transport device simulations indicate that scaling of the FE layer thickness exponentially increases the ferroelectric tunneling ON current and reduces the read latency, leading to nanosecond read speed for the FTJs with CIPS bilayer or trilayer. The FTJ device also shows excellent endurance and retention characteristics.

I. INTRODUCTION

Ferroelectric tunnel junctions (FTJs) have been extensively pursed for memory and information processing applications [1]. Previously studied FTJs are mostly based on perovskite ABO$_3$ and HfO$_2$ ferroelectric materials [2]. Operation of FTJ memory device relies on interface barrier height modulation due to ferroelectric switching and quantum tunneling through an ultrathin barrier layer. Scaling down the ferroelectric tunneling layer and achieving large barrier modulation impose significant challenges for ABO$_3$ and HfO$_2$-based FTJs [1]. In this work, FTJs based on atomically thin van der Waals (vdW) ferroelectric material heterojunctions [3-5], as shown in Fig. 1, are investigated. The vdW heterojunction FTJ devices have the following distinct advantages: (i) extremely large barrier height modulation can be achieved due to low density-of-states in the graphene contact (Fig. 2); (ii) the vdW FE material barrier layer has excellent scalability to atomic layer thickness; and (iii) the vdW interface has high interface quality due to lack of dangling bonds and bond reconstruction. A recent experiment has demonstrated unprecedently high value of the tunneling electroresistance (TER) ratio achieved by the vdW FTJ device [5]. In this study, a multiscale simulation approach from *ab initio* atomistic density-functional (DFT) simulations to quantum transport device simulations is developed to comprehensively understand device physics and model experiment. Furthermore, the ultimate device performance

potential of the vdW FTJs is projected for non-volatile memory applications. The scaling behaviors of the FTJ down to atomically thin tunnel barrier is investigated, which shows exponential increase of the on-current and potential for nanosecond read operation.

II. APPROACH

Multiscale simulations from atomistic *ab initio* simulations to quantum transport device simulations were performed to understand interface and device physics and characteristics. The results are compared to the experimental data.

A. Simulation

The atomistic materials and interface simulations were conducted by density-functional theory (DFT) with Vienna ab-initio simulation package (VASP) codes. Generalized gradient approximation (GGA) method was used with Perdew–Burke–Ernzerhof (PBE) exchange-correlation functional. The weak interaction of vdW force was taken account via DFT-D2 method. The Brillouin-zone was sampled by the $10\times10\times1$ Monkhorst-Pack scheme. The cutoff energy for the wave-function expansion is set to 520 eV.

To obtain the electrostatic band profile, the one-dimensional Poisson equation along the vertical stacking direction is solved self consistently with the equilibrium carrier statistics of the graphene and metal contacts. The ferroelectric polarization charge is located at the FE/contact interfaces and the charge in the FE insulator layer is neglected. Once self-consistency is achieved, the tunneling current is solved by using the non-equilibrium Green's function (NEGF) formalism along the vertical transport direction.

B. Experiment

Graphene/CIPS vdW heterostructure was prepared using try-transfer process. E-beam lithography was used to pattern the metal and graphene contact electrodes. The metal contact was formed with 5 nm Cr and 40 nm Au using e-beam evaporation. The I-V and C-V characteristics of devices were measured in a Lakeshore probe station equipped with a cryogenic system, which allows the measurement of the temperature-dependent I–V characteristics. Kevin probe force microscopy (KPFM) measurement was used to characterize the surface potential modulation in graphene induced by CIPS.

III. RESULTS

Ab initio DFT simulations of the ferroelectric vdW tunnel barrier layer: The ferroelectric material tunnel barrier layer is

the central part of the FTJ device. It is essential to maintain ferroelectricity in a scaled ultrathin film, and at the same time, maintains film uniformity and quality for successful device operation. We, therefore, first examine the 2D vdW ferroelectric material, as exemplified by the CIPS material, to the monolayer thickness limit. Multiple crystalline phases exist in the monolayer CIPS material, including the ground antiferroelectric phase (AFE), a ferroelectric phase which is about 40 meV above the AFE phase per formula unit (f.u.), and a higher-energy paraelectric phase (Fig. 3). Figure 4 shows the measured ferroelectric switching hysteresis loop compared to the modeled characteristics for a CIPS film with a thickness of 4nm and remnant polarization $P_r \approx 8\,\mu C/cm^2$. The calculated FE switching barrier height from nudged elastic band (NEB) simulations (Fig. 5) is comparable to that of FE HfO_2 (190 meV/f.u.), which is consistent with the comparable value of the FE HfO_2 coercive field (at ~1 MV/cm).

Multiscale vdW heterojunction interface simulation: To explore the vdW interface heterojunction at atomistic scale, *ab initio* DFT simulations were performed for the modeled a supercell structure as shown in Fig. 6. The bonds at both the graphene and CIPS surfaces are well satisfied without dangling bonds, which results in high interface quality (Fig. 7). Figure 8 shows the simulated band-structure of the graphene-CIPS heterojunction interface, with the contribution from graphene or CIPS denoted by the colorbar. The result indicates a weak interface electronic hybridization in the energy range of interest. Despite of the vdW interface bonding, the graphene layer maintains its semi-metallic Dirac band structure. It is noted that the DFT simulation has the bandgap underestimation problem for CIPS. To understand the electrostatic coupling and barrier height modulation at the graphene contact and the CIPS interface, a quantum-electrostatic capacitance model is developed (Fig. 9). The graphene quantum capacitance is in series combination with the FE layer capacitance, and the metal contact capacitance limited by the Fermi Dirac screening length in metal. The graphene quantum capacitance is proportional to its density of states, as shown in Fig. 9b. Due to the small quantum capacitance of graphene near the Dirac point [6], and high interface quality, a larger modulation of the graphene Fermi level can be achieved (Fig. 10). As the graphene layer number increases, the density-of-state (DOS) at the Fermi level increases, which results in reduced interface modulation (Fig. 10). The calculated large barrier height modulation at the interface is comparable to the experimentally measured value of ~1eV of height modulation due to FE reversal switching (Fig. 11). The vdW heterojunction interface between graphene and CIPS has the unique features that allow high interface quality and extremely large barrier height modulation.

Device simulation, experiment and performance projection: NEGS simulations of the vdW heterojunction FTJ devices show I-V characteristics in agreement with experiment, with a TER ratio >6×10^7 (Fig. 12). The simulated I-V characteristics at different temperatures agree with experiment and show very small temperature dependence, which is consistent with the tunneling nature of the current (Fig.13). Distribution of the low resistance state, high resistance state and TER ratio, characterized over a large set of device samples, indicates a large memory window and high TER ratio over statistical samples (Fig.14). Experimental characterization and extrapolation show excellent retention of the high TER ratio >10^7 over 10 years (Fig. 15a), and endurance of the TER ratio of ~10^6 for over 10^6 cycles (Fig. 15b).

An important limitation of the FTJ device is its relatively low ON current, leading to slow read operation. The vdW FE materials can permit the FE tunneling barrier to be scale down to atomic thickness with excellent FE film uniformity and high-quality interface. The ON current of the FTJ device exponentially increases as the FE tunneling barrier thickness scales down (Fig. 16), As a result, the projected intrinsic read latency of the memory cell exponentially decreases as a function of the CIPS layer number (Fig. 17). The projection shows the potential to achieve ~1ns intrinsic read latency at a read voltage of 0.5 V for a CIPS FE trilayer, and at a read voltage of 0.3 V for a CIPS FE bilayer. Compared to the MTJ devices whose switching is driven by current, switching in the FTJ device is activated by electric field. The projected intrinsic write energy is proportionally dependent on the FTJ junction area and decreases as the write voltage decreases (Fig. 18). For a scaled junction of 50 nm×50 nm, the intrinsic write energy of the FTJ junction is projected to be ~1 fJ.

Table 1 benchmarks the vdW FTJ device against other FTJs with the metal-ferroelectric-metal (MFM) and metal-ferroelectric-semiconductor structures, MTJ, flash memory, and DRAM device technologies, which indicates the potential of vdW FTJ device for non-volatile memory technologies.

IV. CONCLUSION

A multiscale simulation framework from atomistic *ab initio* DFT simulations to NEGF device simulations is developed to simulate the vdW material heterojunction FTJ devices. The interface simulations indicate large barrier height modulation due to high interface quality free of dangling bonds, weak electronic hybridization of vdW bonds, and low quantum capacitance of graphene. Large barrier height modulation can be achieved even when the graphene layer thickness is increased from monolayer to trilayer. The simulated and measured I-V characteristics show unprecedently large TER ratio (~6×10^7 obtained in experiment). The scalability of the vdW FE layer thickness can result in exponential increase of the ON-current and reduction of the read latency to ~1 ns. The vdW FTJ memory device also shows that the large TER ratio >10^7 can be maintained over a retention >10 years, and the device retains a TER ratio >10^6 after 10^6 switching cycles.

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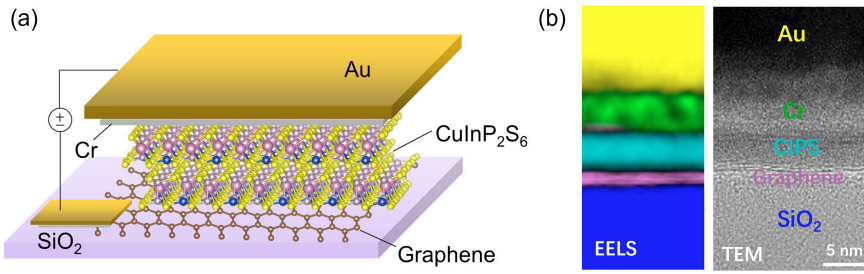
Fig. 1. vdW FTJ device (a) Schematic Device structure of graphene-CIPS vertical van der Waals heterojunction FTJ. The substrate is SiO₂ and the top metal contact is Au. (b) Cross-sectional EELS and TEM of graphene-CIPS FTJ device.
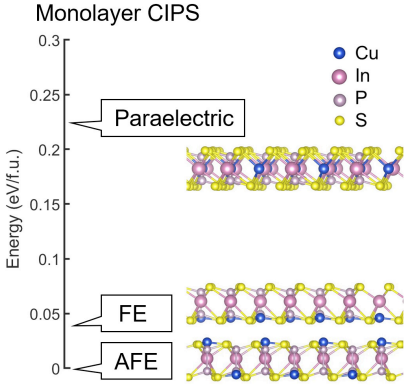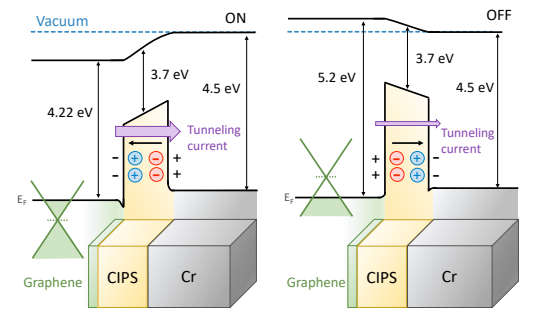

Fig. 2. Band profile of the graphene-CIPS FTJ device at the ON (left) and OFF (right) states, which shows large barrier height modulation

Fig. 3. Energies of monolayer CIPS FE, AFE, and paraelectric phases

Fig. 4. Ferroelectric hysteresis in the CIPS layer: polarization vs electric field relation. The thickness of CIPS is 20 nm. (Experiment: dots, simulation: lines)
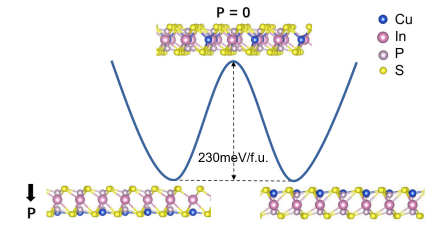

Fig. 5. Kinetic pathway of polarization reversal in monolayer CIPS. The calculated energy barrier, direction of FE polarization and movement direction of Cu atoms are also shown.

Fig. 6. Top view of supercell structure for *ab initio* simulation of the graphene-CIPS vertical vdW heterojunction.

Fig. 7. Cross-sectional view of simulated graphene-CIPS interface charge density. (colorbar: charge density; red: low density; blue: high density). It indicates van der Waals bonding of the heterojunction.
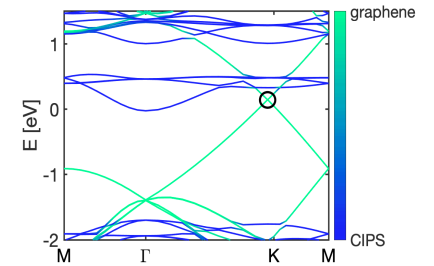

Fig. 8. Bandstructure of the graphene-CIPS vertical vdW heterojunction. The colorbar shows the density weights in CIPS and graphene. The circle shows graphene Dirac point.
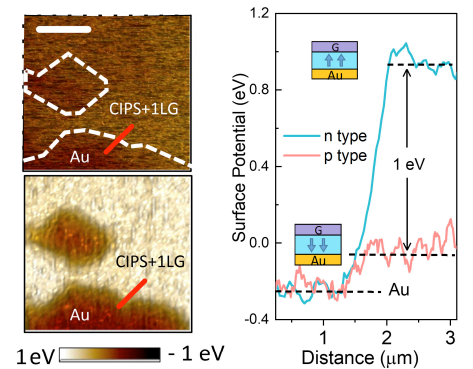

Fig. 9. (a) Capacitance model for calculation of electrostatic potential of graphene-CIPS FTJ device. (b) Quantum capacitance of monolayer, bilayer and trilayer graphene contact vs. energy.

Fig. 10. Fermi level shift for monolayer, bilayer and trilayer graphene contact vs. polarization charge of the FTJ device.

Fig. 11. Experimental measurement on surface potential shift in graphene due to CIPS FE polarization switching.
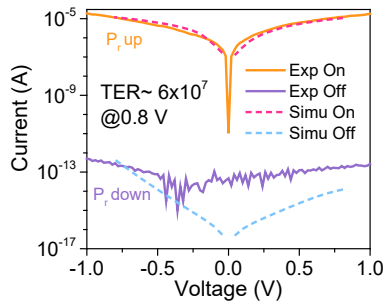
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Fig. 12. NEGF device simulation and experimental *I-V* characteristics at room temperature (300 K). Polarization (P$_r$= 8 µC/cm^2) P$_r$-up is on-state and polarization P$_r$-down is for off-state. The CIPS layer thickness is 4 nm and relative dielectric constant is 10. (Experiment: solid lines; simulation: dashed lines)
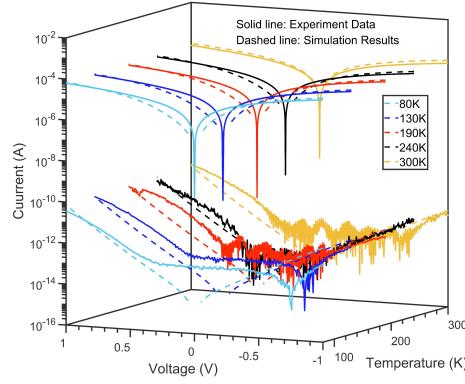

Fig. 13 Temperature dependence of I-V characteristics of the vdW FTJ device. The temperature ranges from 80 K to 300 K. The CIPS layer polarization is 8 µC/cm^2. (Experiment: solid lines; simulation: dashed lines)
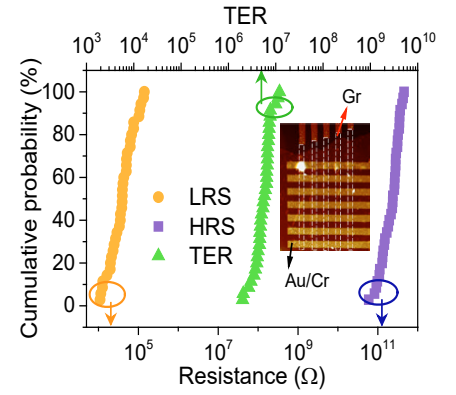

Fig. 14. Statistical distribution of the low resistance state (LRS), high resistance state (HRS), and TER of the vdW FTJ cells (inset).
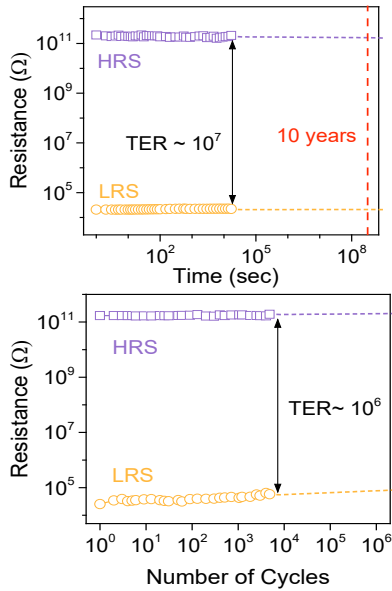

Fig. 15. (a) Retention of the vdW FTJ memory cell with projection to 10 years. (b) Endurance measurement of the vdW FTJ cell with project to 10^6 cycles.
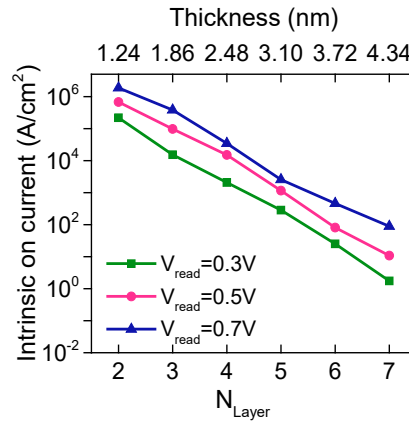

Fig. 16. Scaling behaviors of the simulated on-current as a function of the CIPS number of layers at different applied read voltages. Thickness of per CIPS layer is 0.62 nm. Relative dielectric constant of CIPS is 10 and effective mass of tunneling in vertical direction is $0.8m_e$.
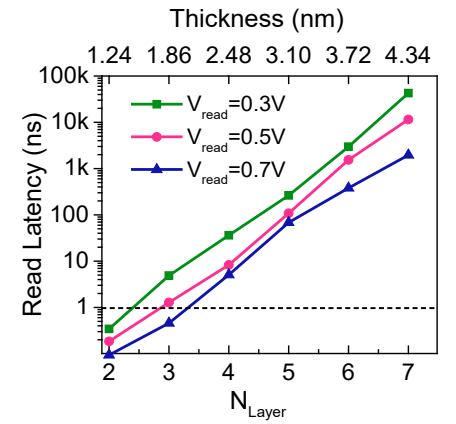

Fig. 17. Simulated intrinsic read latency vs. the number of layers at read voltages of 0.3, 0.5, 0.7 V. The FTJ area is $2 \times (14\,nm)^2$, and the accessing interconnect capacitance is $0.1fF/\mu m$ with a length of $10\,\mu m$. The horizontal dashed line shows 1ns latency for reference.
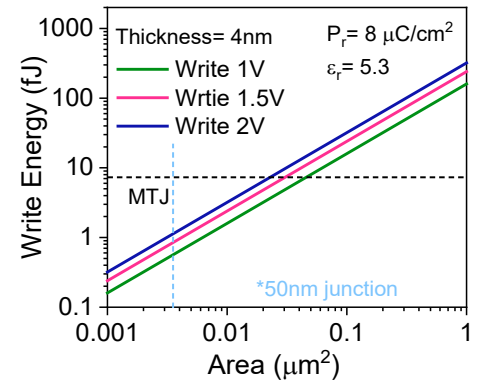

Fig. 18. Projected intrinsic write energy vs. the FTJ device junction size under different write voltages. Only charge on the FTJ device is considered in the intrinsic write energy estimation.

*Simulation with 50 nm wide junction. Data from: [i] D. J. Kim *et al*., Nano Lett. 12, p.5697, 2012; [ii] Z. Xi *et al*., Nat Commun. 8, 15217, 2017; [iii] M. Wang *et al*., Nat Commun. 9, 671, 2018; [iv] N. Papandreou *et al*., IEEE ISCAS, p.329, 2011; [v] A. Chanthbouala *et al*., Nat. Nanotech. 7, p.101, 2011; [vi] C. Ma *et al*., Nat Commun. 11, 1439, 2020; [vii] C. Grezes *et al*., Appl. Phys. Lett. 108, 012403, 2016; [viii] J. Liang *et al*., VLSIT Symposium, p.100, 2011; [ix] O. Golonzka *et al*., IEEE IEDM, p.412, 2018; [x] H. Sato *et al*., IEEE IEDM, p.608, 2018; [xi] J. S. Vetter *et al*., Comput. in Sci. & Eng. 17, 2, p.73, 2015; [xii] L. Thomas *et al*. IEEE IEDM, p.612, 2018; [xiii] Z. Wen *et al*., Nat Mater. 12, p.617, 2013; [xiv] A. Chen *et al*., Emerg. Nanoelec. Dev., 2014; [xv] G. Navarro *et al*., IEEE IEDM, p.570, 2013.