Fabrication of Localized Silicon-On-Insulator Based Rhombus-Shaped Channels in Silicon

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Introduction

- Fabricating localized silicon-on-insulator (LSOI) on bulk silicon eliminates the need for using expensive SOI wafers for silicon waveguides and MEMS applications.
- Fabrication of LSOI in standard silicon wafers is considered to have precise control of the oxide thickness which will lead to effective integration of electronic and photonic devices
- We used rhombus-shaped channel method in the fabrication of LSOI structure that can be produced on any part of a bulk silicon wafer
- A Si structure with funnel width of 14µm and funnel angle of 140° was achieved after etching in a solution of Tetramethylammonium hydroxide (TMAH) with isopropyl alcohol (IPA) for several hours.

Method

- The rhombus-shaped channel is the approach deployed in the fabrication of the localized silicon-on-insulator structure on bulk silicon wafer
- The rhombus shaped SOI is governed by three main parameters namely the width of silicon opening between two rhombic shapes (W), mask width (M) and depth of the trench (D)

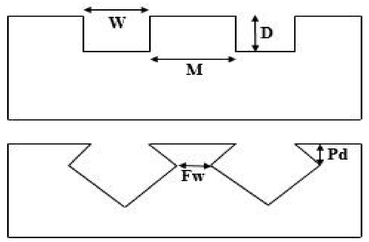

Figure 1.Geometry of the rhombus-shaped silicon channels showing the width of silicon opening between two rhombic shapes W, mask width M, depth of the trench D, Funnel width Fw, and pinch depth P_d,

- The depth of trench is important to avoid the formation of a V channel caused by the <111> crystal planes. Several equations and limitations govern the formation of the funnel structure of local silicon on insulator ;

$$D > \frac{W}{\sqrt{2}}\ ;\ M > \frac{D}{\sqrt{2}}\ ;\ Fw = M - \frac{D}{\sqrt{2}};\ Pd = \frac{D}{2} + \frac{W}{\sqrt{2}}$$

Process Design and Experimental Steps

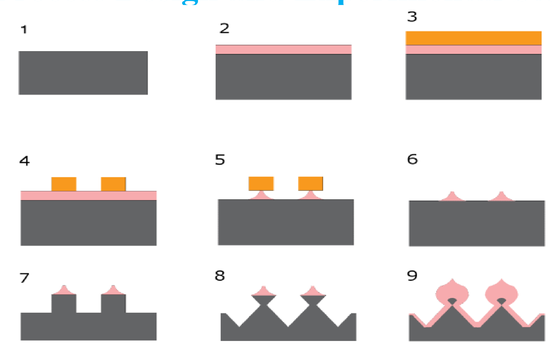

Figure 2. Rhombus-Shaped channel fabrication steps. It begins with a clean <100> silicon wafer (1). A layer of thermal oxide is grown on the wafer (2), a photolithography process is performed on the sample (3,4), the oxide hard mask is etched isotopically in BOE and lift-off process is performed (5,6). RIE step is performed to create the trench depth (7). Anisotropic wet etching is performed (8). The sample is thermally oxidized to create an island of silicon (9).

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Graphical Representation of Funnel Width vs. Mask Width by varying Trench Depth

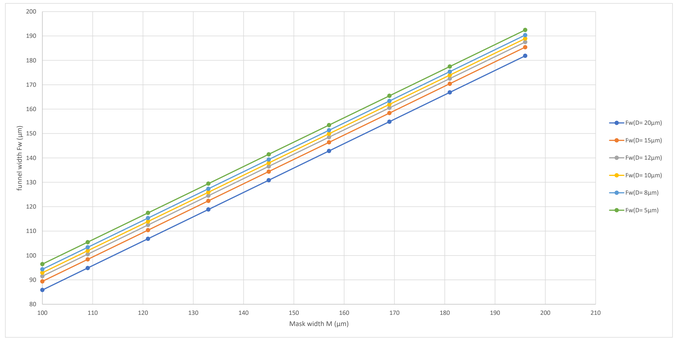

Figure 3. Funnel width Fw vs. mask width M for trench depth W=200µm.

- The graph indicates that the funnel width gets smaller when the depth of trench increases.

Fabrication Process of LSOI Structure

- Fabrication process includes; RCA cleaning, Photolithography, Reactive ion etching (RIE) and Orientation Dependent wet etching.

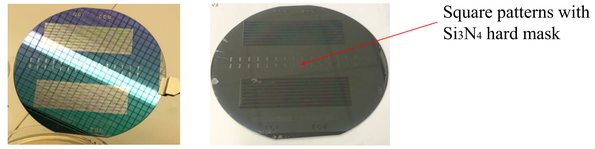

Figure 4. Optical mage shows a wafer after photolithography process (L) and after reactive ion etching (R).

Results

- SEM Images were taken on the wafer sample to see the level of etching on the exposed oxide square pattern after several hours of anisotropy etching

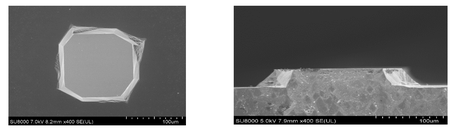

Figure 5. Top and cross-section views of Si island after one hour of anisotropic etching.

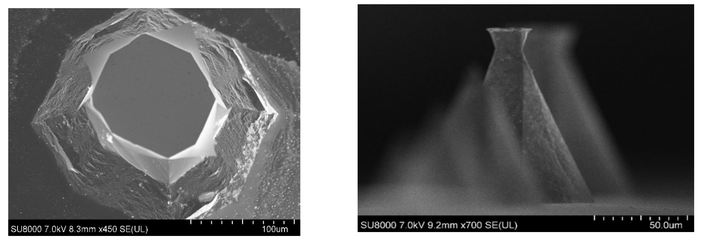

Figure 6. (L) Top view of Si island and (R) cross section of Si island bound by rhombus etching. The funnel angle is 140° . Etching at the bottom is un-pinched as W is too large.

Discussion and Future Work

- The fabrication process to achieve the desired structure was established. The result indicates that the funnel structure was smooth by etching in TMAH/IPA. In addition, the result shows the importance of the depth of trench produced by RIE. More work on thermal oxidation time, and oxide thickness on the SOI funnel will be needed to optimize the rhombus shape.

References

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