Fundamental Improvement to the Efficiency of On-Chip mmWave Phased Arrays Using MEMS Suspension

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***Abstract*—A major shortcoming of current silicon-based millimeter-wave (mmWave) on-chip antennas is the low radiation efficiency (<50%). In this letter, we present a novel on-chip antenna array with the radiation efficiency >80% at 60 GHz. The proposed array addresses the issues of on-chip air-suspension using micro electro mechanical systems (MEMS) processes, thus elevating the hovering radiating elements on a substrate at the height of 35 μm (0.007 λ_0). The micofabricated SU-8 posts serve as the vertical support, ensuring mechanical stability and monolithic integration. The simulated −10 dB fractional bandwidth of this array is 5.5% or 3.4 GHz at 60 GHz. Further, the designed array is capable of scanning of ±55° in the *E* plane and ±58° in the *H*-plane. The non-contact backscattering method is proposed and employed to derive the radiation efficiency from measured radar cross-section (RCS) data. RCS measurements are performed using a precision six-axis robotic arm with the spatial repeatability of 20 μm (λ_0/250). The measured radiation efficiency is 82% at 60 GHz. The measured peak gain of 9 × 9 array is 23.3 dBi versus simulated 23.6 dBi. Fundamental enhancement in suspended array efficiency is achieved by eliminating unwanted radiation in the silicon substrate. Compared to other on-chip integration approaches, the proposed array can be monolithically integrated on a silicon substrate while maintaining high radiation efficiency.**

***Index Terms*—Antenna-on-chip, high efficiency, millimeter-wave (mmWave band), phased array, suspended.**

I. Introduction

ALTHOUGH the increasing demand for wireless connectivity now causes data-traffic congestion at the traditional microwave spectrum, the possibility exists for using untapped millimeter-wave (mmWave) band to reduce this congestion. While the availability of the 7 GHz unlicensed band (57–64 GHz) makes the 60 GHz band a prime candidate for these next-generation indoor communication systems, difficulties continue to hinder the adoption of mmWave technology [1], [2]. For example, the impaired wave propagation by severe path-loss [3], [4] necessitates the use of high-gain antenna arrays. Further, given the need of the transmitter and receiver movement and for multibeam operations, mmWave arrays capable of scanning large angles with high gain are of critical importance.

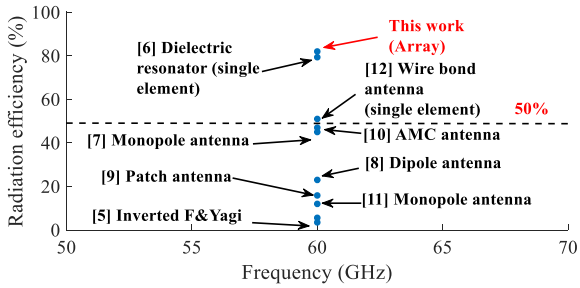

Fig. 1. Radiation efficiency comparison between the proposed and other on-chip antennas.

Low radiation efficiency (5%–10%) and, consequently, low gain are major challenges hindering the use of mmWave antennas for direct and monolithic on-chip integration [5]–[8]. As Fig. 1 demonstrates, none of the present generation of direct on-chip mmWave arrays provides high radiation efficiency for practical applications [9]–[12].

To address the low radiation efficiency, several available on-chip approaches target at substrate properties such as substrate thinning [8], micromachining techniques [13], and proton implantation [14]. For example, the substrate thinning technique is adopted to increase the efficiency to 45% with an on-chip cavity [7]. However, it requires complex feeding structures (e.g., balun, transition, bridge, and cavity), which are impractical and complex for use in array applications. Another approach involved the fabrication of a silicon lens to convert the surface wave into radiation [15]. However, this bulky configuration requires a large lens and another supporting wafer that is inherently incompatible with the array architecture.

In contrast to the aforementioned approaches, this letter presents a novel air-suspended solution that yields 82% radiation efficiency via micro electro mechanical systems (MEMS) fabrication techniques (see Table I). We also refined the feeding network and improved fabrication and measurement capabilities as compared to [17]–[19]. In Section II, a new air-suspended architecture is discussed. The fabrication details and validation

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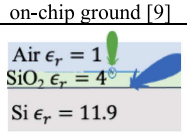
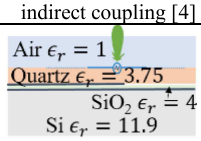
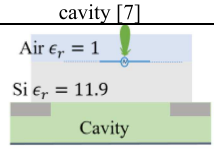
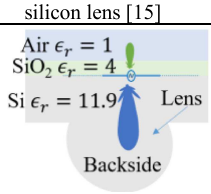
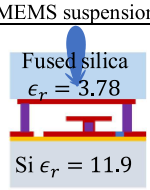
TABLE I
COMPARISON OF PROPOSED ANTENNA WITH OTHER ON-CHIP ARCHITECTURES

	Integration with an on-chip ground [9]	Integration with indirect coupling [4]	Integration with a cavity [7]	Integration with a silicon lens [15]	Integration using MEMS suspension
Model					
Effciency	7%	50%	45%	45%	82%
Fabrication	Easy	Complex	Complex	Complex	Complex

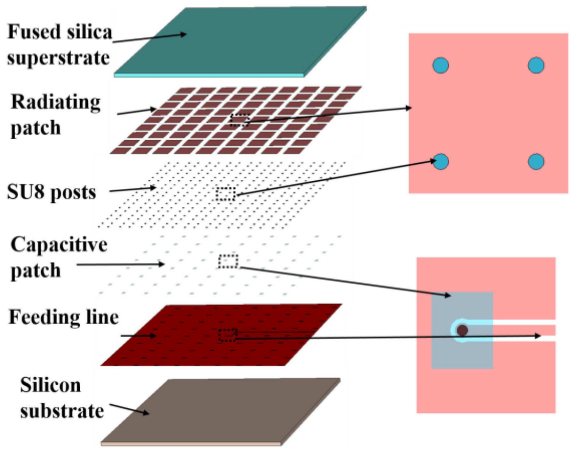


Fig. 2. 3-D view of components of proposed on-chip array.

are presented in Section III. Finally, the measured gain pattern and the radiation efficiency are discussed in Section IV.

II. NEW ON-CHIP AIR-SUSPENDED ARCHITECTURE

For a patch antenna, an air substrate of low-ϵ_r can simultaneously increase radiation efficiency and impedance bandwidth [20]. However, for monolithic on-chip integration, an mmWave air-suspended antenna requires managing the electrical and thermal properties of substrate, integrating with on-chip circuits using flip-chip packaging, and creating a mechanically stable supporting structure. Fig. 2 presents the major components of air-suspended on-chip array. To meet the thermal requirement of on-chip integration, fused silica is used in our design as the superstrate. It has a coefficient of thermal expansion of 2.5 ppm/°C (shown in the far-right column in Fig. 2), and at 60 GHz a dielectric constant of 3.8 with $\tan\delta < 0.001$ [21]. This combination of both electrical and thermal properties makes fused silica suitable for mmWave antenna integration/packaging.

In this proposed architecture, microfabricated posts made of SU-8 photo patternable epoxy serve as the vertical support, thus ensuring mechanical stability and constant air gap at mmWave frequencies. As shown from Fig. 3, for unit-cell configuration, four SU-8 posts support the hovering radiating patch 35 μm ($0.007\lambda_0$) above the ground plane. In addition to the high aspect ratio, SU-8 exhibits low dielectric constant and moderate loss

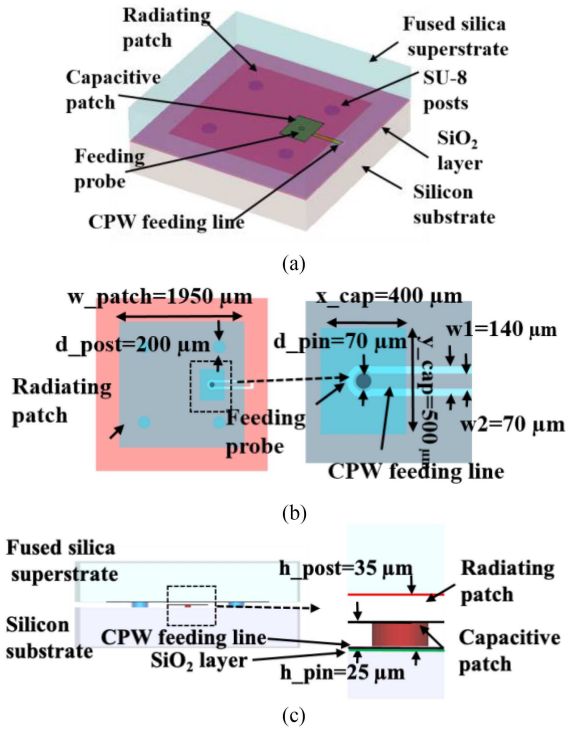


Fig. 3. (a) 3-D view of unit cell of proposed on-chip array. (b) Top exaggerated view of the unit cell. (c) Side exaggerated view schematic of the feeding structure.

tangent ($\tan\delta < 0.027$ below 200 GHz) [22]; however, this is less important as more than 95% of array is hovering in air.

We note that the proposed array can be monolithically integrated with T/R modules in the future. The capacitive feeding is utilized because this configuration enables the direct location of T/R modules underneath each radiating element. Moreover, the radiating patch layer is fabricated onto the fused silica wafer, and the thermal properties of fused silica permit an easy flip-chip mounting to the silicon chip.

The designed finite 9×9 antenna array is simulated using the time-domain CST Design Studio with 15 million mesh elements. The array size is 24.75 mm $\times$ 24.75 mm with an element spacing of 2.75 mm (0.55 λ_0 at 60 GHz). The optimized feeding probe height and post height is 25 (0.005 λ_0) and 35 μm (0.007 λ_0), respectively. Future integration will involve feeding each array element through a separate T/R module for active scanning. Based on the simulation results in Fig. 4, the designed array is

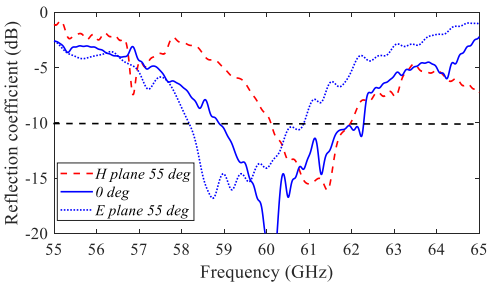


Fig. 4. Simulated reflection coefficient of the center element of 9 × 9 array at broadside and maximum scanning volume showing that −10 dB bandwidth is 3.4 GHz (5.5%) at broadside.

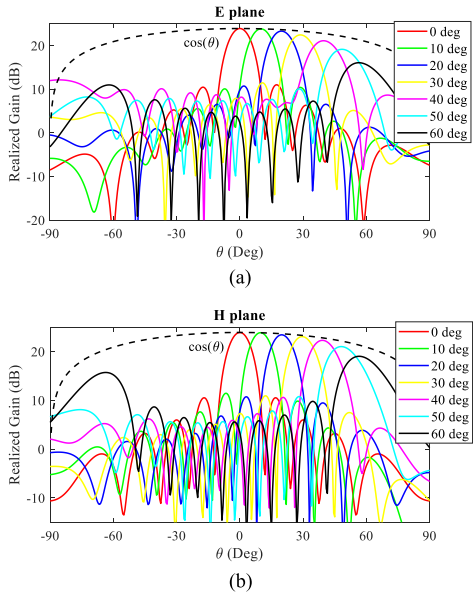


Fig. 5. Simulated (a) *E*-plane and (b) *H*-plane gain pattern of the 9 × 9 array as a function of scanning angles from broadside to 60° with 10° step.

matched at 60 GHz with S_{11}<–20 dB and the −10 dB impedance bandwidth of the array 3.4 GHz (5.5%) at broadside. Fig. 5 shows that the simulated peak realized gain is 23.9 dBi for the broadside with a sidelobe level of –13 dB. Further, this 9 × 9 array is capable of ±55° scanning in the *E*-plane and ±58° scanning in the *H*-plane (shown in Fig. 5). The mid-air suspension of the array ensures a radiation efficiency as calculated, and later on measured (in Section III), of 85%.

III. Simplified Fabrication and Validation

The small wavelength hinders the measurement accuracy of on-chip mmWave antennas. For example, any minor deviations in the measurement setup of a free-space wavelength of 5 mm at 60 GHz results in amplitude and phase errors. For on-chip antenna pattern measurement, the antennas are fed using the probe, which has a robust adverse effect upon measurement performance. Therefore, here noncontact backscattering methods are used to prevent small vibrations from the tube that cause phase errors and degrade the measurement accuracy [23]. These methods focus on the alternative approach to replace the cables or probes with different termination cases. Typically, special

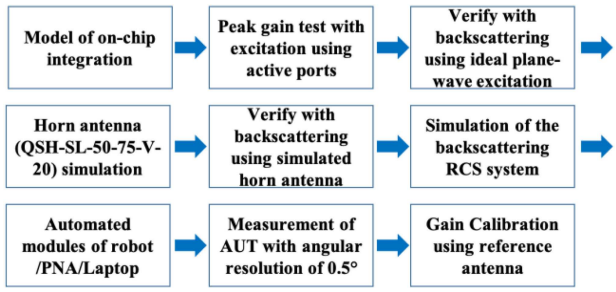


Fig. 6. Structure summary of our proposed backscattering RCS measurement approach.

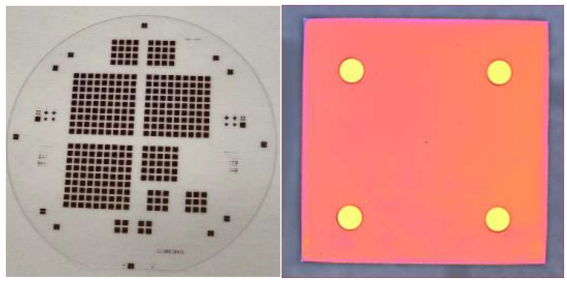


Fig. 7. Fabricated (a) on-chip suspended antenna arrays and (b) unit cell of suspended patch antenna with SU-8 posts.

terminations (e.g., open, short, and 50 Ω loads) are used given the easy-to-characterize reflection coefficient of these loads. Consequently, the unknown reflection coefficients of antenna under test are derived based on known termination cases. Based on radar equation, the effective aperture of antenna under test can be derived from measured radar cross-section (RCS), and consequently, the gain is acquired ($G = 4\pi A/\lambda^2$) [24], [25].

Fig. 6 presents the structure of the proposed measurement system. Our proposed on-chip solution targets the radiation efficiency (or the peak realized gain). First, the standard port excitation is used, and the simulated peak gain is found to be 24.7 dBi with all 81 ports excited. Based on RCS backscattering results, the peak gain of six-layer short terminations is 24.4 dBi. Further, to reduce fabrication complexity, a simplified model is used with the simulated peak gain of 24.2 dBi. The simplified three layers are radiating patch, suspension, and ground layers. Hence, a simplified RCS measurement approach is used to simplify this fabrication process from six layers to three for radiation efficiency/gain pattern analysis. In this simplified three-layer approach, a 0.5 μm-thick copper layer is used for deposition and patterning on a 500 μm-thick fused silica substrate. Next, 35 μm-thick SU-8 supporting posts are spin-coated for suspended elements and patterned lithographically. On a separate silicon wafer, the 0.5 μm-thick SiO_2 layer is first deposited as isolation layer and next a 0.5 μm-thick copper layer is deposited to form the short load termination layer. Finally, the wafer is flipped and bonded to the fused silica wafer. Fig. 7 presents the fabricated antenna array. As shown in scanning electronic micrograph (SEM) of Fig. 8 and optical interferometry measurement results of Fig. 9, the height of fabricated SU-8 posts is 34.9 μm, which agrees with the designed 35 μm.

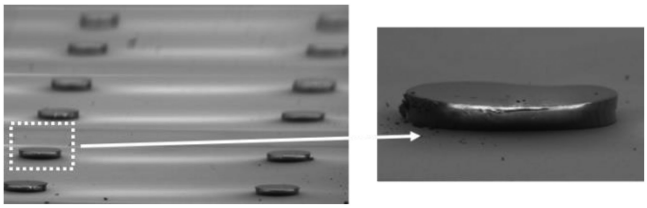


Fig. 8. SEM photographs of fabricated SU-8 post.

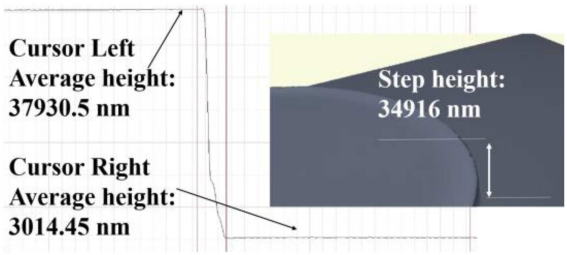


Fig. 9. Measured 3-D profile of SU-8 post height using an optical profilometer showing that the fabricated SU-8 height is 34.9 μm.

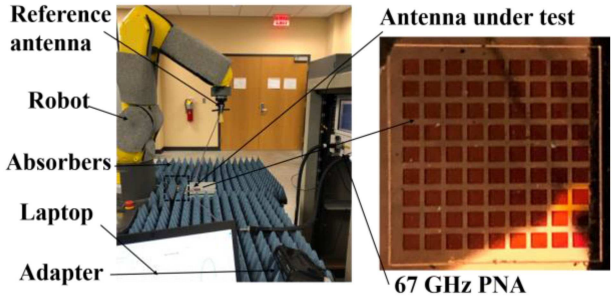


Fig. 10. Robotic antenna measurement system.

The RCS measurement is characterized using an accurate six-axis robotic arm (Fanuc LR Mate200iD) with the repeatability of 20 μm (λ_0/250) [26], [27]. First, the backscattering measurements are calibrated using two standard horn antennas (QSH-SL-50-75-V-20), one used as a probe and the other as a reference. Next, a laser pointer is used to align the horn antenna to the center element of the 9 $\times$ 9 array. Third, a half-circle ($-90°<\theta<90°$) spherical trajectory is performed while acquiring data with 0.5° angular resolution, centered around the antenna under analysis. Finally, a 67 GHz network analyzer is used to capture the reflection coefficient of horn antenna. This simplified approach targets at measured peak RCS value, and the peak gain can be derived based on radar equation with known parameters such as distance, power ratio (reflected to transmitted), and known gain of reference antenna.

IV. Conclusion and Discussion

The antenna measurement system using a precision robotic arm is illustrated in Fig. 10, and a comparison of the simulated/measured gain pattern at 60 GHz in Fig. 11. As shown in Fig. 11, the measured peak gain is 23.3 dBi, showing a good agreement with the simulation results. Fig. 12 presents that the measured radiation efficiency is 82% at 60 GHz. The measured radiation efficiency is constant when the fabricated post height

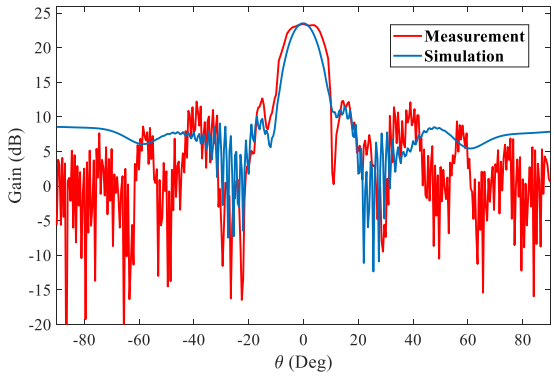


Fig. 11. Comparison of simulated and measured gain pattern at 60 GHz.

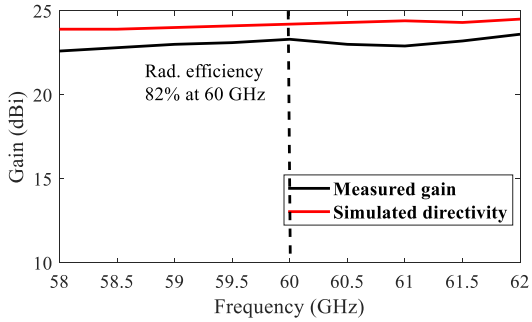


Fig. 12. Relationship of the measured gain and the simulated directivity with frequency showing the radiation efficiency is 82% at 60 GHz.

TABLE II
Comparison of Key Features of the Proposed Antenna

	Rad. efficiency	Scanning
[4]	50%	55°
[7]	45%	Non-scanning
[10]	47%	Non-scanning
[12]	50.9%	Non-scanning
Proposed array	82%	55°

ranges from 34.8 to 35.2 μm. For simplified three-layer model, the conductivity of copper is assumed to be 5.8 $\times$ 10^7 S/m. However, copper conductivity can be lower for fabricated on-chip films. For instance, assuming copper conductivity of 2 $\times$ 10^7 S/m, the radiation efficiency is reduced from 85% to 76% based on simulation results. In addition, as can be seen in Table II, the proposed antenna array achieves high radiation efficiency and moderate scanning volume.

The use of MEMS techniques addresses the issues of air-suspended monolithic on-chip integration, resulting in the reduced effective dielectric constant. The result, via the air substrate, is a decrease in conduction, dielectric, and surface wave losses, manifested in drastic increase in radiation efficiency. Compared to the other on-chip approaches, the proposed architecture maintains monolithic integration and high radiation efficiency with moderate scanning volume.

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