

# A Low-Cost Vertically Integrated Antenna Array at 60 GHz With 85% Efficiency

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**Abstract**—Although the 60 GHz band meets the higher data rate demands for various wireless applications, large path losses and small size of 5 mm free-space wavelength makes the design, fabrication, packaging, and measurement of 60 GHz antenna arrays challenging. In this letter, we present a low-cost and high-efficiency patch antenna array fabricated using a printed circuit board (PCB) process. As the mini-connector size is larger than unit-cell at 60 GHz, it poses challenges for separate feeding for each array element. This optimized configuration not only addresses the mini-connector assembly shortcoming for off-chip antenna measurements in a laboratory environment but also permits future direct flip-chip integration on a transceiver. Embedded thin-film resistors are first used to fabricate 50  $\Omega$  termination and calibration elements on the same board, thus removing associated lossy and bulky external loads and calibration kit. Next, a highly precise robotic antenna measurement system is used to complete the challenging task of measuring far-field pattern at 60 GHz. The proposed 5  $\times$  5 antenna array is matched at 60 GHz with the  $-10$  dB bandwidth of 3.6 GHz (6%). The peak realized gain of the 5  $\times$  5 array is 18.5 dBi, and the measured boresight efficiency is 85% at 60 GHz. Furthermore, the simulated maximum scanning volume is  $\pm 40^\circ$  in the  $E$ -plane and  $\pm 45^\circ$  in the  $H$ -plane. Therefore, the proposed 60 GHz antenna array maintains a low-cost, high-efficiency moderate scanning range with a potential for easy on-chip integration for future communication and sensing applications.

**Index Terms**—60 GHz, antenna array, high efficiency, patch antenna.

## I. INTRODUCTION

THE growing demand for various wireless applications necessitates the use of higher data rates, resulting in the data traffic congestion at commonly used bands. As the millimeter-wave (mmWave) bands remain largely untapped, one solution is the availability of the unlicensed 57–64 GHz band that makes the 60 GHz operational frequency a suitable candidate to address the data rate shortcomings. Although the wave propagation at 60 GHz is impaired by severe path loss, it can be mitigated by high gain, beam-steering, or multipath environment [1]. Therefore, for short-range communication, any 60 GHz antenna array must be capable of scanning with a high gain.

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Compared with monolithic on-chip integrated antennas [2], array solutions on printed circuit boards (PCBs) have several advantages including low cost, fast fabrication, and low complexity. For example, a 60 GHz magnetoelectric dipole antenna was used to maintain wide impedance bandwidth and high gain [3]. The large size of the W-type connector, however, made this magnetoelectric dipole antenna inherently incompatible for phased array architecture. In another study, a dipole array with multilayer configuration was optimized with a packaged feeding network [4]. Unfortunately, the bulky structure hindered the low-profile on-chip integration. Another effort entailed using a broadband slot antenna fed by a substrate integrated gap waveguide, with an end-launch connector to feed the whole array [5]. Consequently, it was not suitable for active scanning. Finally, whereas a ridge gap waveguide feeding layer did yield a high gain, the complicated structure was costly and difficult for on-chip antenna attachment [6]. Therefore, for single-layer [7], [8] or multilayer [9]–[12] configurations at 60 GHz, a series or parallel feeding network is commonly used with a single end-launch connector. As the free-space wavelength at 60 GHz is 5 mm, the connector size is often larger than the unit-cell, thus posing challenges for the active feeding of individual array elements.

To overcome these shortcomings, we describe the following unique features of our proposed antenna array verified using a robotic antenna measurement system.

- 1) The novel feeding configuration addresses the mini-connector assembly (diameter = 2.79 mm) deficiency with individual array elements, resulting in a path for active scanning.
- 2) The embedded thin-film resistors are first used at 60 GHz, thus eliminating the associated expensive and lossy 50  $\Omega$  loads.
- 3) The calibration kit is designed and fabricated on the same PCB with the antenna, improving the accuracy of measurements at 60 GHz.

## II. NEW PHASED ARRAY ARCHITECTURE

### A. Antenna Geometry

As the direct measurement of the whole antenna array necessitates the use of a power divider, phase shifter, and mini-connectors at 60 GHz, the active element pattern measurement approach [13]–[15] is used, i.e., with one element of the array fed with other array elements matched with 50  $\Omega$  resistors. Fig. 1

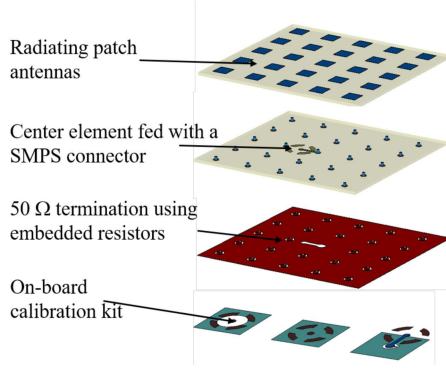


Fig. 1. 3-D view of the proposed 5×5 antenna array.

TABLE I  
OPTIMIZED VALUES FOR ANTENNA PARAMETERS

Parameter	$L_1$	$W_1$	$L_2$	$W_2$	$L_3$	$R_1$	$R_2$
Value (mm)	1.275	1.35	0.1	0.1	0.35	0.114	0.24
Parameter	$R_3$	$h_1$	$W_3$	$W_4$	$R_4$	$R_5$	$R_6$
Value (mm)	0.34	0.254	0.2	0.1	0.2	0.3	0.84

shows the major components of the proposed antenna array. Here, the center element is fed with an *SMPS* mini-connector (SV Microwave#3811-60005), while the other array elements are terminated with the OhmegaPly embedded 50  $\Omega$  resistors. Yet, there are several challenges: 1) a volume limitation of the mini-connector ( $r_{\text{connector}} = 2.79 \text{ mm} > 0.5\lambda_0$ ); 2) impact of external lossy termination loads; 3) a transition design of the mini-connector assembly.

The OhmegaPly embedded resistor technique is utilized instead of external loads, i.e., the 50  $\Omega$  resistors are fabricated on the PCB [16]–[18], ensuring a compact, low-loss, and low-cost solution. To employ the embedded resistors, CLTE-XT laminate (from Rogers) with  $\epsilon_r = 2.94$  and  $\tan\delta = 0.0012$  (at 10 GHz) is adopted. Previously, we used RO3003 laminate ( $\epsilon_r = 3$ ,  $\tan\delta = 0.0013$  at 10 GHz) as the substrate material [19]. However, the low modulus and the ceramic filler particles of the latter alter the resistor value uniformity. In contrast, the woven glass reinforcement in CLTE-XT enhances the rigidity of the material. In addition, a pure polymer layer at the interface between the resistive layer and the dielectric provides a more uniform surface.

Because the mini-connector size is larger than  $0.5\lambda_0$  at 60 GHz, the element spacing is increased to 3 mm ( $0.6\lambda_0$ ). As the element spacing increases above  $0.5\lambda_0$ , the sidelobe level degrades due to mutual coupling [20]. The substrate height is 0.254 mm ( $0.05\lambda_0$ ) as a thicker substrate produces more surface waves and mutual coupling, thus decreasing the efficiency by coupling additional power to unwanted surface/guided wave modes. The unit-cell design is in Fig. 2 and the optimized antenna parameters are in Table I.

To address the volume limitation issues of the via-feeding assembly, the feeding transition is designed as shown in Fig. 2(a). For off-chip antenna measurement, the assembly layout is designed for *SMPS* mini-connectors. As a consequence, each array

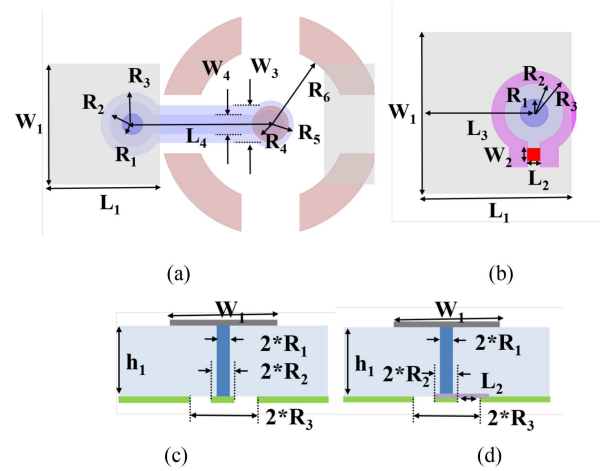


Fig. 2. Top view of the unit-cell including (a) termination elements and (b) center element by via-fed approach; side view of the unit-cell including (c) termination elements and (d) center element fed by via-fed approach.

element is fed separately for active scanning. This feeding scheme is applicable to flip-chip integration. Unlike low frequency applications, wire bonding produces a large insertion loss at 60 GHz. Therefore, the advantages of flip-chip integration including compactness, high speed, and flexible connection [2] are maintained in our approach.

### B. On-Board Termination and Calibration Design

As the sheet resistivity is chosen, the size of the resistive foil determines the electrical resistance ( $R = R_s \times (\frac{L}{W})$ ) [17]. The circular shape of the via-feed assembly, however, makes it difficult to etch the resistive layer and calculate the accurate resistance. To address this issue, the designed resistive structure [shown in Fig. 2(a)] shifts the etching area to a square shape ( $W_2 = L_2 = 0.1 \text{ mm}$ ), making it easy to align the etched area to achieve an accurate resistor value. As with the on-board termination process, the 50  $\Omega$  calibration utilizes the embedded resistor rather than external loads. As a result, the calibration kit is fabricated on the same PCB board, resulting in an accurate mmWave measurement.

### C. Simulation Results

The designed 5×5 antenna array, consisting of 13 million mesh elements, is simulated using CST Studio and a time-domain solver. We studied and analyzed the scanning performance of a finite array with all 25 ports excited. Fig. 3(a) presents the designed layout and Fig. 3(b) shows the simulated reflection coefficient of the center element with broadside and two maximum scanning cases. As the scanning angle increases, an increase in mutual coupling is observed. As shown in the simulated gain pattern in Fig. 4, the designed array is capable of moderate scanning of  $\pm 40^\circ$  in the *E*-plane and  $\pm 45^\circ$  in the *H*-plane at 60 GHz. The simulated radiation efficiency is 87% at broadside. We also studied and modeled the layout and coupling effects of the nearby array elements, the results of which are in Fig. 5. As shown in Fig. 5(b), the mutual coupling loss is calculated based on the location of the array elements.

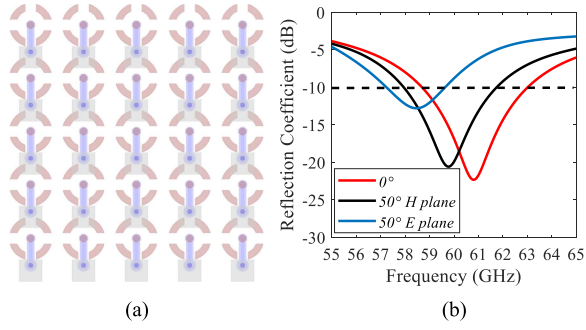


Fig. 3. (a) Layout of the  $5 \times 5$  array with all ports excited and (b) simulated reflection coefficient of the center element of the  $5 \times 5$  array at broadside and two maximum scanning angles.

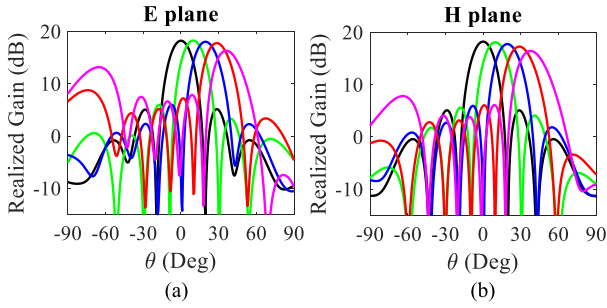


Fig. 4. Simulated radiation patterns (realized gain) of the  $5 \times 5$  array as a function of the scanning angle ( $0^\circ$ – $50^\circ$  with  $10^\circ$  steps). (a)  $E$ -plane. (b)  $H$ -plane.

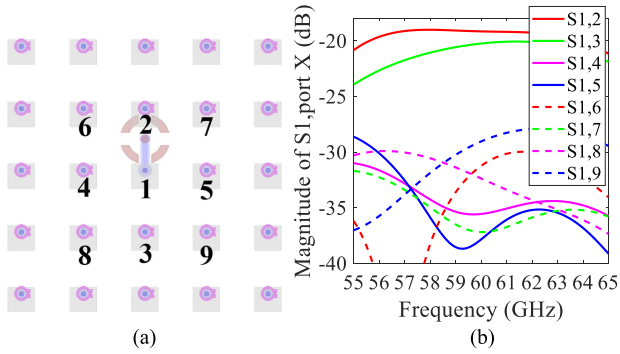


Fig. 5. (a) Measurement layout and (b) simulated port-to-port coupling of nearby elements.

### III. FABRICATION AND MEASUREMENT

Figs. 6 and 7 present the fabricated prototype composed of a single  $5 \times 5$  array and a calibration kit. The array size is  $15 \text{ mm} \times 15 \text{ mm}$  with an element spacing of  $3 \text{ mm}$  ( $0.6\lambda_0$  at  $60 \text{ GHz}$ ). The active element pattern strategy [14] is utilized for the antenna measurement. As shown in Fig. 6, the center element is fed while the other elements are matched. The mutual coupling losses are included by utilizing  $50 \Omega$  on-board loads. The gain is given as

$$G_{\text{array}} = N G_{\text{element}} \left( 1 - \sum_{n=1}^N |S_{1n}|^2 \right) \quad (1)$$

where  $S_{1n}$  is the mutual coupling between port  $N$  and center port 1,  $N$  is the numbers of array elements, and  $G_{\text{element}}$  and  $G_{\text{array}}$  are the gain of the center element and array, respectively.

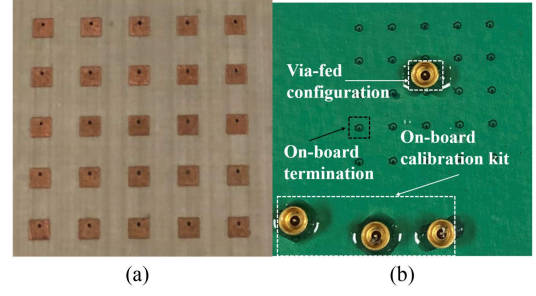


Fig. 6. (a) Top view and (b) bottom views of the fabricated  $5 \times 5$  antenna array.

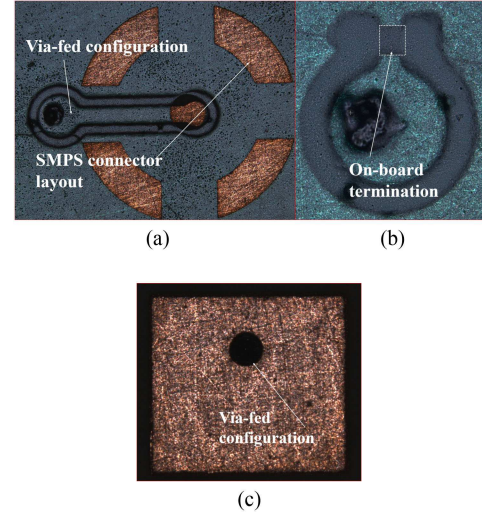


Fig. 7. Microphotos of the fabricated unit-cell. (a) Bottom view of the center element. (b) Bottom view of the termination element. (c) Top view of the patch antenna.

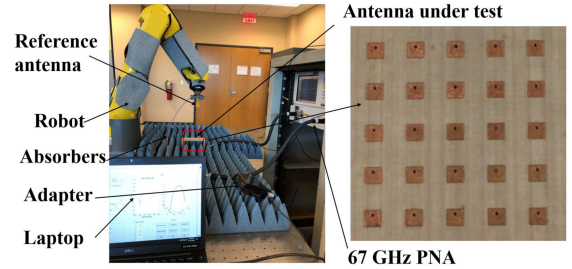


Fig. 8. Antenna measurement system at  $60 \text{ GHz}$  using robotic arm.

Hence, the array gain is obtained from the pattern measurements for the center element in conjunction with all port-to-port mutual coupling loss.

Fig. 8 presents the antenna measurement system. After calibration via the on-board standards, a network analyzer is used to measure the reflection coefficient of the center element. The far-field measurements are calibrated using two standard gain horn antennas (QSH-SL-50-75-V-20), one used as a probe and the other as a reference. The probe antenna is attached to a robotic arm (Fanuc LR Mate 200iD) that operates as a precession positioner and is connected to the network analyzer [21], [22]. The fabricated array is fixed on top of a mounting structure and connected to the second port of the network analyzer. The center of the horn antenna is aligned to the center element of



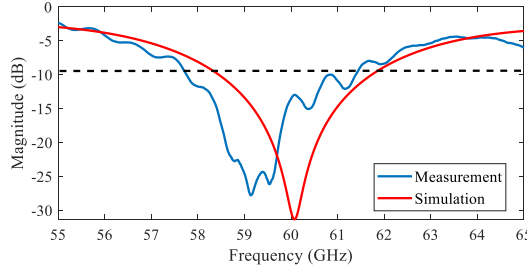


Fig. 9. Comparison of the simulated  $S_{11}$  with measured center element of the  $5 \times 5$  array showing the  $-10$  dB bandwidth of 3.6 GHz (6%).

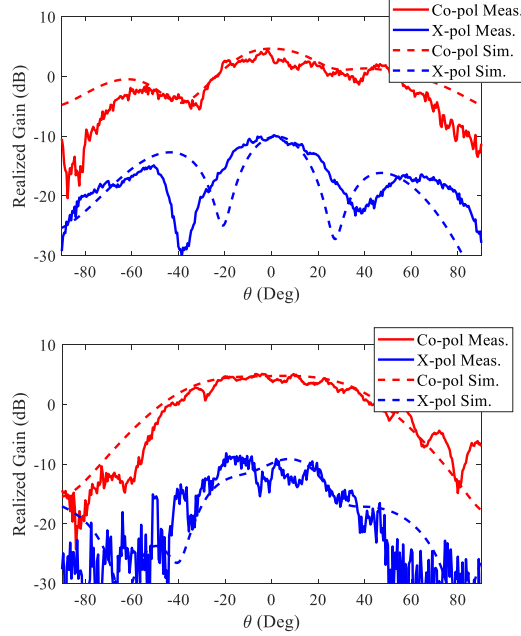


Fig. 10. Comparison of the simulated and measured pattern (realized gain) for the center element at 60 GHz in the  $E$ -plane (top) and  $H$ -plane (bottom).

the array using a laser pointer. A half circle ( $-90^\circ < \theta < 90^\circ$ ) trajectory centered on the antenna under analysis is performed while acquiring  $S$ -parameters with  $0.5^\circ$  angular resolution.

#### IV. CONCLUSION AND DISCUSSION

Fig. 9 presents the simulated and measured impedance matching results. The measured  $-10$  dB impedance bandwidth of the array is 3.6 GHz (6%), which is sufficient for most wireless applications. Fig. 10 provides a comparison of the simulated and measured element pattern at 60 GHz in the  $E$ - and  $H$ -planes. The measured pattern closely matches the simulation result. Note that in Fig. 11, the measured radiation efficiency is 85% at 60 GHz. Finally, the comparison in Fig. 12 of the simulated and measured array pattern at the  $E$ - and  $H$ -planes shows a measured and simulated peak gain of the  $5 \times 5$  array at 18.5 and 18.7 dBi, respectively, at 60 GHz.

As shown in Table II, unlike other 60 GHz arrays using PCB techniques, our proposed architecture achieves high efficiency. Our scheme also addresses the issues of mini-connector assembly and permits future flip-chip on-chip integration. On the same board, the embedded termination design eliminates

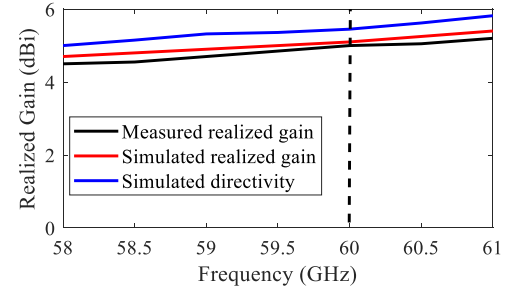


Fig. 11. Comparison of the measured realized gain and simulated realized gain/directivity showing a measured boresight efficiency of 85% at 60 GHz.

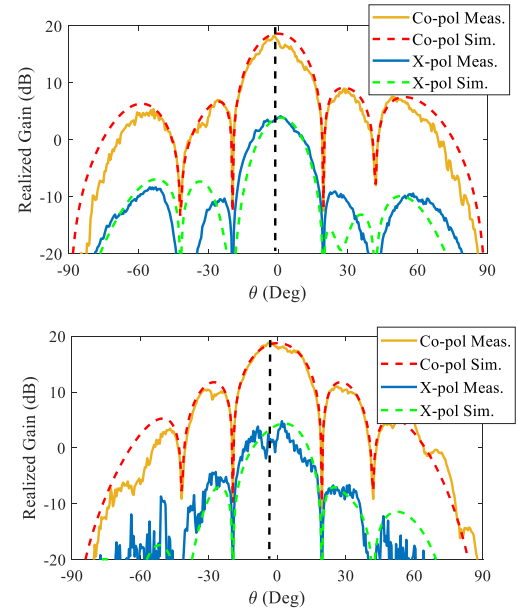


Fig. 12. Comparison of the simulated pattern (realized gain) with the measured of the  $5 \times 5$  array at 60 GHz in the  $E$ -plane (top) and  $H$ -plane (bottom).

TABLE II  
COMPARISON OF KEY FEATURES OF DESIGNED ARRAY

	Efficiency	On-chip
[4]	85% at 32 GHz	Wire-bond
[10]	80% at 60 GHz	Wire-bond
[11]	72.2% at 60 GHz	Wire-bond
[12]	63.6% at 59 GHz	Flip-chip
This work	85% at 60 GHz	Flip-chip

the associated lossy external termination loads, thus enhancing efficiency.

The assembly limitations of *SMPS* mini-connectors required increasing the element spacing above  $0.5\lambda_0$ , which also decreases the maximum scanning volume with  $10^\circ$ – $15^\circ$  due to the degraded sidelobe level. Based on our previous work [23], it is possible to improve the scanning to  $\pm 60^\circ$  at the  $E$ - and  $H$ -planes using a dielectric superstrate layer. In addition, the scanning volume can be further increased to  $\pm 65^\circ$  at both the  $E$ - and  $H$ -planes with the use of the planar frequency selective surface superstrate [24].

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