

Capacitive Link for Data Communication Between Free Floating mm-sized Brain Implants

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Abstract—Establishing communication between free floating brain implants is critical in applications that require a population of implants to operate in an organized manner or in a real-time feedback loop. We present a feasibility study of a data transmission link between mm-sized free floating brain implants through capacitive coupling. The proposed capacitive link utilizes metal plates integrated on a bottom and a sidewall of the implant. We demonstrate that the minimum required input power for establishing the data link is 31 nW at the operating frequency of 915 MHz. We demonstrate the feasibility of the data link up to a distance of 2 mm between the implants.

Index Terms—Capacitive Coupling Link, Inductive Link, Mm-sized Brain Implants, Data Telemetry, Wireless Data Transfer

I. INTRODUCTION

Large distributed arrays of free floating sub-mm and mm-sized implantable device have been proposed recently as the next generation of the recording and stimulation technology in neuroscience [1]. These devices enable the high spatial and temporal resolution recording and stimulation covering a wider area of the brain than the conventional approaches that employ monolithic microelectrode arrays (MEAs) with fixed electrode placement [2], [3]. Additionally, the proposed free floating implant technology offers less invasive implantation process, increased safety and robustness to long term scarring [4]. With the increasing coverage area of the brain surface, the number of these implants quickly grows. The large number of implants introduces new challenges in the design of the wireless power transfer from the external device. The wireless power delivery to the miniaturized implants has been implemented through ultrasound coupling, inductive coupling and capacitive coupling. While in the case of the deep implantation depth ultrasound coupling is favored, the integration of implant on a single chip and higher sensitivity to misalignment favor inductive and capacitive coupling [5].

Data transfer between the external device and the implanted device has been implemented by applying the same coupling mechanisms. The multi-access networking design has been mostly investigated using backscattering principle in an inductive/RF link data link. Frequency-division multiple access [6] and time-division multiple access [7] have been demonstrated for sub-mm sized implants. Time, spatial, and frequency division multiplexing have also been implemented

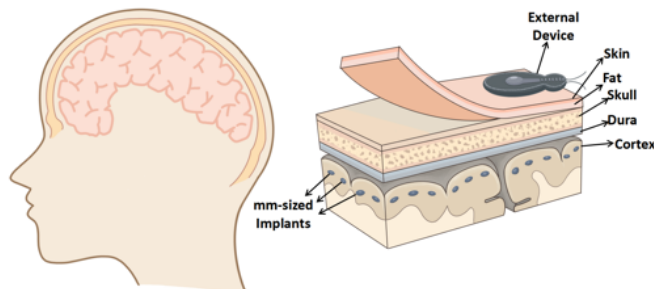


Fig. 1. Illustration of mm-sized free-floating implants in a human brain.

using ultra-sound links with separated transmitting and receiving transducers integrated on a sub-cm sized implant [8]. These methods are based on a centralized network design, in which each implant communicates with an external device. As the number of implants increases, the performance of these networks deteriorates. Additionally, in some of the envisioned applications of densely distributed sub-mm and mm sized implants, these implants could perform tasks like neural recording in an organized manner. In a similar fashion, recording and stimulating implants could operate in a real-time feedback loop. Enabling communication between implants could alleviate constraints posed by such applications. We have recently investigated the feasibility of the backscatter-based communication between the sub-mm sized implants to improve the scalability of network of such implants [9].

Capacitive coupling has also been utilized for data transfer with sub-cm sized implants [10]. Conventionally, a capacitive coupling link comprises four metal plates, horizontally or vertically arranged, forming two capacitive couplers for data transfer. One set of these plates is implanted, while the other set is located on the surface of the skin. We proposed a study of the feasibility of the capacitive link for implant to implant data transfer. Compared with the inductive coupling, capacitive coupling relieves the relatively severe electromagnetic interference (EMI) on other implants and the sensitive analog circuitry in the system. Capacitive link is feasible to separate power and data carriers. It allows for multi-telemetry link even on the same platform and operates at the same carrier frequency [10], [11], which is a especially suitable candidate for mm-sized brain implants to implants communication.

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TABLE I
GEOMETRY PARAMETERS FOR CAPACITIVE LINK AT 915 MHZ

L (mm)	W_1 (mm)	W_2 (mm)	T (μ m)	R (mm)	d (mm)
1	1	0.2	7	0.8	1

The paper is organized as follows. Section II presents a circuit model of capacitive link with modeling of the two mm-size chips surrounded by brain grey matter. Simulation results of the link performance and comparison with two different capacitive link structures are presented in Section III. Section IV concludes the paper with outline of the future work.

II. CAPACITIVE LINK MODEL

Developed as a single channel stimulation and recording devices, sub-mm and mm-sized implants have been integrated as an application specific integrated circuit (ASIC) chips without bulky off-chip components. Instead of the external electrodes for stimulation and/or recording, to further miniaturize the implant, the on-chip electrodes in a form of metal plates can be integrated on the same chip. Au plates with deposited conductive polymer (PEDOT:PSS) and carbon nanotubes (CNT) have been demonstrated as functioning stimulation electrodes [6].

We investigate if these integrated electrodes can be used to establish a capacitive link for the communication between two implants. In the simplified model used in the following analysis, we assume that these metal plates are deposited on the sidewall and on the bottom side of the implant¹, as illustrated in Figure 2(a). The sidewall plate is covered with biocompatible silicone coating material and the bottom plate is exposed to grey matter. We first develop a lump model of the link that is then evaluated against a complex EM simulator.

The capacitance C_{fwd} and resistance R_{fwd} between the two parallel side plates of the communicating implants are

$$\begin{aligned} R_{fwd} &= \frac{d}{\sigma_t(f)W_2L} \\ C_{fwd} &= \frac{\epsilon_o\epsilon_{r,t}(f)W_2L}{d} \end{aligned} \quad (1)$$

where W_2 and L are the dimension of the plates and d is the distance between plates. σ_t and $\epsilon_{r,t}$ are conductivity and relative permittivity of the material in which implants are immersed. In this study, we assume a brain grey matter. C_{bwd} and R_{bwd} denote the coupling between the pair of the bottom plates. C_{bwd} is estimated as [12]

$$C_{bwd} = \frac{\epsilon_o\epsilon_{r,t}(f)L}{\pi} \left(\log\left(1 + \frac{2W_1}{d}\right) + \exp\left(\frac{-(T+d)}{3d}\right) \right) \quad (2)$$

where W_1 is the width of bottom plate, T is the thickness of plate and L is the length of plate. The first term in C_{bwd} is conformed radial electric field and the second term is the electric field line at semicircular region. The self-coupling between the plates on the same implant has significant impact on the data link performance as it degrades the power efficiency

¹The top side of the implant contains an on-chip inductor for powering the implant through an inductive link.

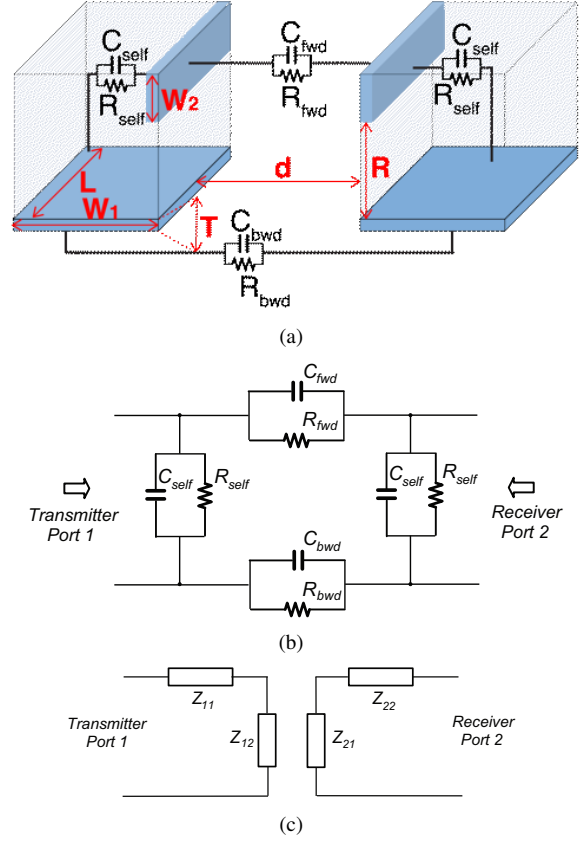


Fig. 2. (a) Capacitive coupling link for wireless data transfer between two mm-sized implants. (b) Electrical circuit and (c) two-port model of a capacitive coupling link.

of the link. The self-capacitance, C_{self} , is estimated as [13], [14]

$$\begin{aligned} C_{self} &= C_{ext} + C_{int} \\ &= \epsilon_o L \left(\epsilon_{r,t} \frac{K'(k_{ext})}{K(k_{ext})} + \epsilon_{r,s} \frac{K'(k_{int})}{K(k_{int})} \right) \end{aligned} \quad (3)$$

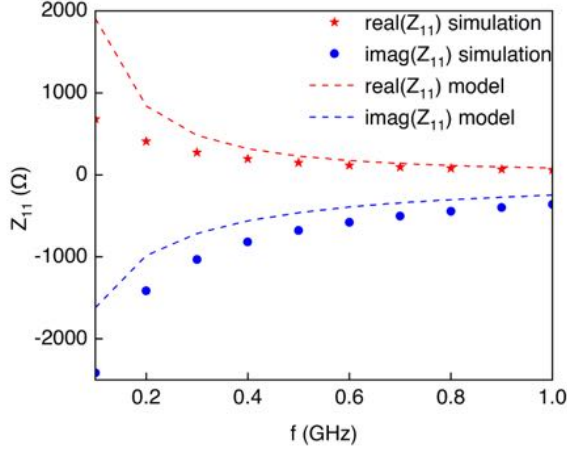
where C_{ext} and C_{int} denote the capacitance that come from the exterior and interior chip coupling, respectively. $\epsilon_{r,s}$ is the relative permittivity of the substrate material on which the plates are deposited. FR4 is assumed as the substrate material in this study. $K(k)$ is the complete elliptic integral of the first kind and k_{in} and k_{out} are defined as

$$k_{in} = \sqrt{\frac{R^2((R+W_2)^2 + W_1^2)}{(R^2 + W_1^2)(W_2 + R)^2}} \quad (4)$$

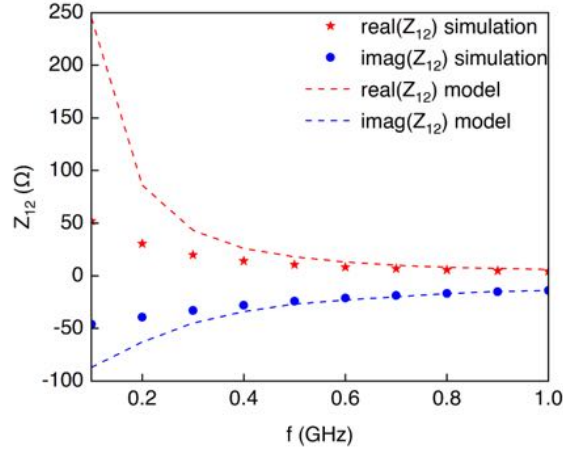
$$k_{out} = \sqrt{\frac{R^{\frac{2}{3}}((R+W_2)^{\frac{2}{3}} + W_1^{\frac{2}{3}})}{(R+W_2)^{\frac{2}{3}}(R^{\frac{2}{3}} + W_1^{\frac{2}{3}})}} \quad (5)$$

where R is the gap between the bottom and sidewall plate and W_2 is the width of sidewall plate.

The corresponding impedance Z_{fwd} and Z_{bwd} are scaled by fitting variables α and β that account for the plate shielding



(a)



(b)

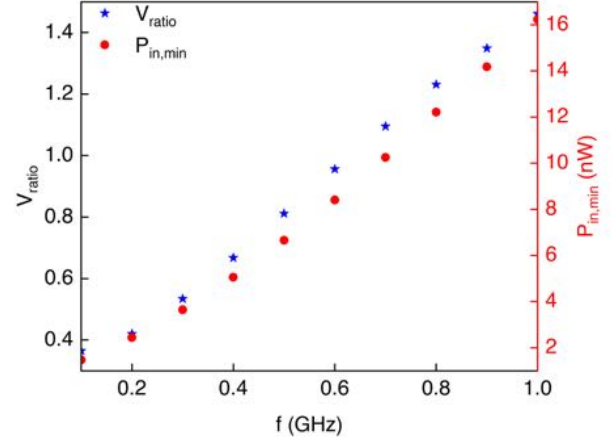
Fig. 3. Z parameters for two-port model calculated based on the lump model and obtained through HFSS simulation. (a) Real and imaginary parts of Z_{11} and Z_{22} , (b) Real and imaginary parts of Z_{12} and Z_{21}

effect. Taking Z_{bwd} as an example, the existence of a side metal plate prevents the bottom plate top to top electrical field coupling and C_{bwd} is reduced. In the proposed lump model, the cross impedance between side plate on one implant and bottom plate on the other implant is neglected.

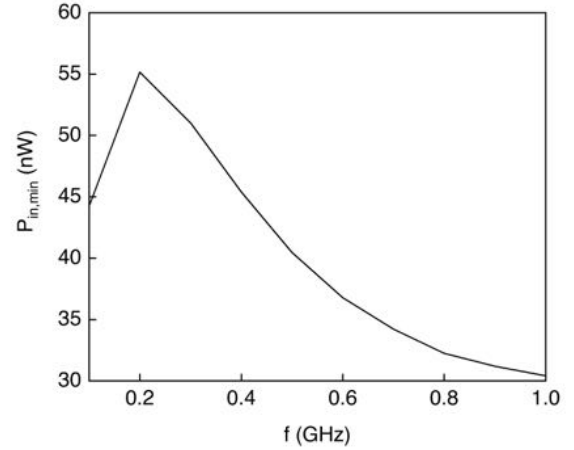
The resulting equivalent circuit model is shown in Fig. 2(b). Based on the calculated lump values of the resistors and capacitors, a two-port model between transmitter and receiver implant is obtained as

$$\begin{aligned} Z_{11} = Z_{22} &= \frac{Z_{self}(Z_{self} + Z_{bwd} + Z_{fwd})}{2Z_{self} + Z_{bwd} + Z_{fwd}} \\ Z_{12} = Z_{21} &= \frac{Z_{self}^2}{2Z_{self} + Z_{bwd} + Z_{fwd}} \end{aligned} \quad (6)$$

The geometry parameters used for the computation of the equivalent two-port Z model are shown in Table. I. The



(a)



(b)

Fig. 4. (a) The ratio between voltage at the receiving side V_{out} and transmitting side V_{in} of the link and the input power P_{in} required for the input voltage of 1 V. (b) The input power required to achieve a minimum output voltage that can be resolved at the receiver for operating link.

frequency-dependent dielectric properties of the brain grey matter are obtained from [15]. The calculated values of Z_{11} and Z_{12} from the lump model are plotted in Fig. 3, along with the values obtained by simulation of the capacitive link using 3D EM solver Ansys HFSS. The plots verify the proposed lump model of the link.

III. SIMULATION RESULT

Capacitive link is modeled as a two-port network shown in Fig. 2(a)(c). To characterize the link, both the transmitting and the receiving side of the link operate at the resonant frequency to increase in order to increase the power efficiency and the output voltage. The load impedance at receiver side R_L is set as 1 MΩ. The output voltage at the receiver $V_{out} = R_L I_{out}$

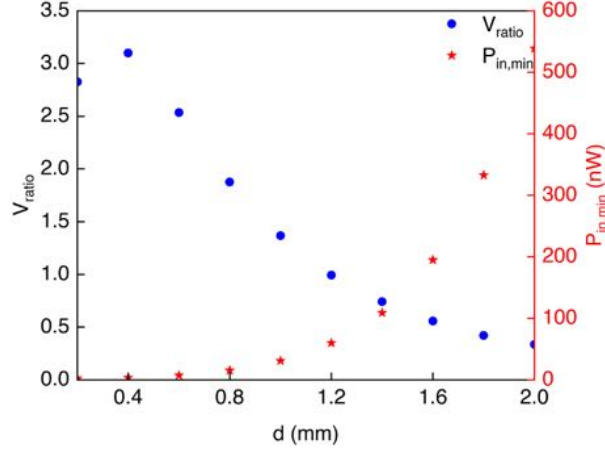


Fig. 5. The ratio between the voltages at the receiving and transmitting implant and the minimum input power as a function of the distance between implants.

is then obtained from

$$\begin{bmatrix} V_{in} \\ 0 \end{bmatrix} = \begin{bmatrix} Z'_{11} & Z_{12} \\ Z_{21} & Z'_{22} + R_L \end{bmatrix} \begin{bmatrix} I_{in} \\ I_{out} \end{bmatrix} \quad (7)$$

where Z'_{11} and Z'_{22} include the added impedance at the transmitting and receiving side in order to achieve resonance.

A. Frequency Analysis

We first investigate the dependence of the link performance on the operating frequency. With the increasing frequency, both Z_{11} and Z_{12} decrease, due to higher conductivity and lower permittivity of the surrounding material, as shown in Figure 3. The ratio between the voltage at the receiving and transmitting side is computed as

$$V_{ratio} = \frac{V_{out}}{V_{in}} = \frac{Z_{12}Z_{2L}}{Z'_{11}(R_L + Z'_{11}) - Z_{12}^2} \quad (8)$$

and is shown in Fig. 4(a) as a function of frequency, from 0.1 GHz to 1 GHz, along with the input power, P_{in} , obtained for the input voltage V_{in} equal to 1 V. To find the minimum input power at which the link can operate, we fix the output voltage at the minimum value that can be resolved on the receiving side. We assume amplitude-shift keying(ASK) modulation and the minimum output voltage of 2 mV is obtained based on our previously designed self-biased ultra-low power ASK demodulator [16]. Based on the minimum output voltage and the voltage ratio, the minimum input power, $P_{in,min}$ is obtained and it is shown in Figure 4(b) as a function of frequency. Less input power is required for establishing the data link at higher frequency. 915 MHz is chosen for compatibility with other industrial, scientific and medical (ISM) device, and power consumption is 31 nW.

In Fig. 5, we show the voltage ratio and the minimum required input power as a function of the distance between the implants. At the distance of 2 mm, V_{ratio} is higher than 33.5%, while the minimum required input power is 538 nW.

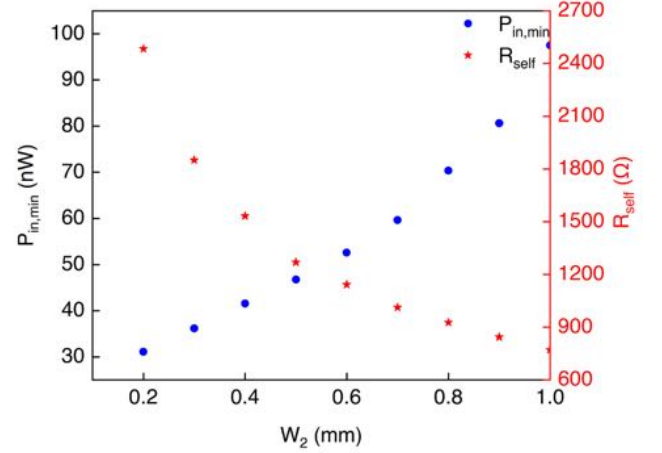


Fig. 6. Minimum input power and R_{self} as a function of sidewall plate width.

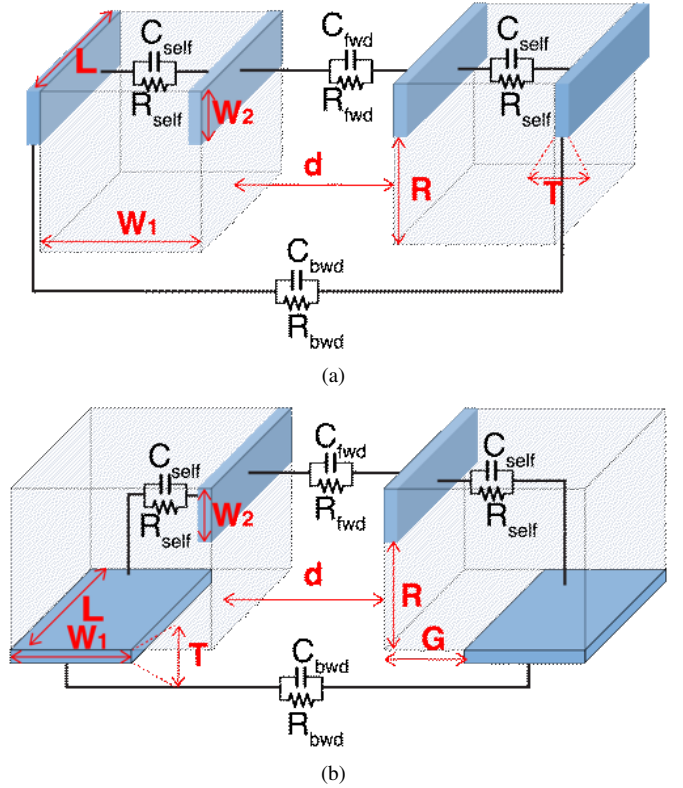


Fig. 7. Two proposed capacitive link structures. (a) Design 2 with only sidewall plates. (b) Design 3 with larger gap between bottom and sidewall plate.

B. Three Structures Comparison

The power consumption on the impedance Z_{self} represents a leakage power. From the simulation results, in the studied structure, it adds a significant contribution to the overall input power. In the proposed structure in Figure 2(a), the width of the sidewall plate, W_2 is chosen as 0.2 mm. Increasing

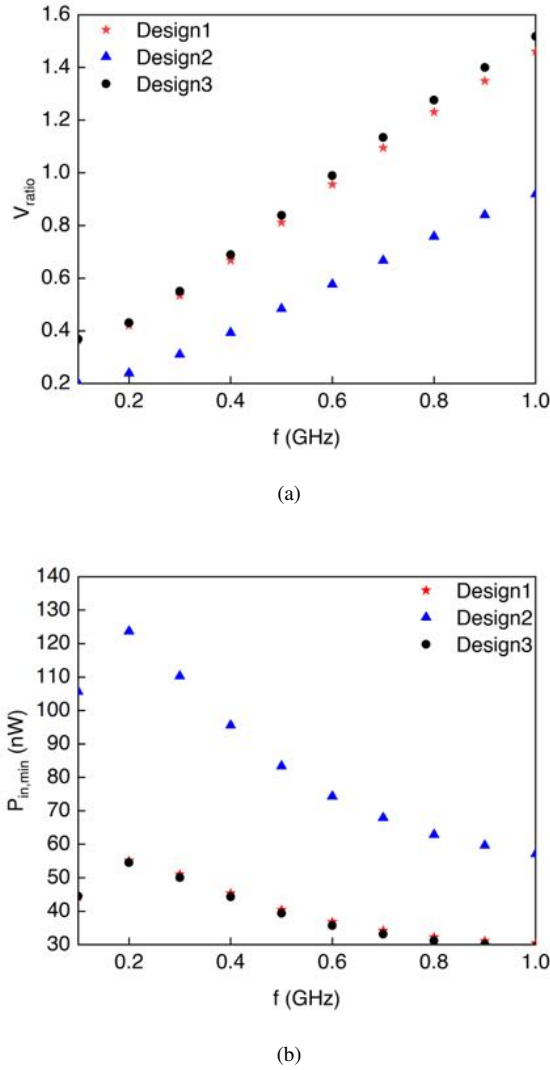


Fig. 8. (a) The ratio between the voltages at the receiving and transmitting implant and (b) the minimum input power as a function of the distance between implants.

W_2 increases the coupling between the sidewall plates of the transmitting and receiving implant, which in turn increases the voltage ratio. However, the facing area of the sidewall plate and bottom plate on the same implant also increases and through R_{self} significantly increases leakage power. Fig. 6 shows that R_{self} changes from 2483 Ω to 771 Ω when the side plate width increases to 1 mm and at the same time leads to higher minimum input power required for establishing the communication link.

We analyze two more structures that increase R_{self} and study the effect on the minimum required input power. The first structure uses only sidewall plates (denoted as Design 2), while the second one is moving bottom plate away from the side plate by 0.5 mm (denoted as Design 3), in illustrated in Figure 6. The structure in Figure 2(a) is denoted as Design 1. The voltage ratio and the minimum input power

for all three designs are shown in Figure 7. Although R_{self} in Design 2 increases, the increased distance between the opposing sidewall plates of the two implants reduces coupling effect through backward path resulting in a drop of voltage ratio. Design 3 lowers normalized input power consumption by 1 nW at the cost of increased width of the implant. Taking into account the input power and fabrication technology, the proposed Design 1 presents the most promising option for data transfer and it is compatible with the sub-mm sized implant proposed in [6].

IV. CONCLUSION

The proposed capacitive link for communication between mm-sized brain implants has been investigated. The developed lump circuit model provides a good estimate of the two-port model and enables insight into the link performance. With the operating frequency of 915 MHz, the communication link is established at the input power of 31 nW. Three different structures have been proposed and compared with the focus on reducing leakage power. In our future work, we will continue optimization of the implant structure, as well as the parameters like the thickness of the coating material and thickness of the chip. The effect of the misalignment between the implants will also be studied.

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