Heterogeneous Integration for Silicon Photonic Systems: Challenges and Approaches

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Abstract

The promise of silicon integrated circuits with their electronic or photonic functionality enhanced via heterogeneous integration has motivated significant work in understanding and overcoming the barriers to realizing such an IC. Additional hurdles must be overcome when integrating devices that are highly sensitive to temperature variation such as semiconductor lasers. Challenges in the heterogeneous integration process will be reviewed, and approaches for heterogeneous integration that have the potential to enable silicon ICs with enhanced functionality will be discussed in the context of integrated photonic systems.

(Keywords: Heterogeneous Integration, Silicon Photonics, Manufacturing, CMOS)

Introduction

Enhancing the functionality of silicon through the integration of other materials such as III-V semiconductors has been recognized as a path to overcoming limitations imposed by characteristics fundamental to silicon's material physics while still capitalizing on properties that have enabled the success of the global integrated circuit industry [1-3]. High-speed electronic devices, devices with high breakdown voltages, light emitting/detecting devices, and devices for photon control can all be integrated with conventional CMOS to perform specialized electronic or photonic functions if suitable methods for forming such heterogeneously integrated regions are available that provide high yield and are compatible with fabrication processes that occur subsequent to the heterogeneous integration process. Technical challenges include lattice mismatch, thermal expansion coefficient differences, having the capability to form low-resistance electrical contacts using materials that are compatible with CMOS, more generally managing cross-contamination in tools used for front-end-of-line processing after III-V regions are established on the silicon wafers, and thermal management for the heterogeneously integrated devices or circuits. These together create formidable obstacles, but there is also the obstacle of defining a business case for creating hybrid wafer fabs given the applications that would be served by ICs with enhanced functionality. Bringing functions that are off chip onto the chip needs to be justified both technically and financially.

Heterogeneous Integration Methods Over Time

A variety of approaches have been explored over time to achieve the function and performance of non-native devices on silicon. Early attempts at direct growth of III-V materials on silicon yielded devices that functioned, but the high defect density resulting from the growth of epitaxial layers thicker than the critical thickness resulted in devices with impaired performance or limited lifetime [4-5]. Even with the use of thick buffer layers and strained superlattice structures intended to keep defects away from the device active region, the combination of light and heat provide sufficient energy for defect propagation, especially dark line defects [5]. Beyond a certain point, limited progress was made on direct growth. Around the same time, the idea of using a patterned silicon wafer as an optical bench was advanced. In this method, precision placement tools were used to accurately bond fabricated III-V die onto a silicon wafer having patterned alignment features and V-grooves for fiber attach. This method was successful and is still used today, but the low throughput of the process given the time needed to place die with micron-scale tolerance limited scalability. Additionally, the vision of integrating CMOS electronics onto the silicon optical bench was never commercially justified given the performance-cost-yield trade-off. More recent efforts on heterogeneous integration have explored growth on transferred "seed" crystals [6], growth of quantum wires [7], and growth of quantum dots [8]. These techniques have yielded promising device results but have the challenge of being higher-temperature processes that complicate CMOS compatibility. Other methods specific to silicon photonics have either used evanescent coupling to bonded III-V gain material [9] or edge coupling of metal-bonded III-V gain material [10] to form lasers. These techniques have the advantage of eliminating the need for precision alignment at the individual device level, and have shown promise for defining a path forward for wafer-

scale integration of photonic functions.

Heterogeneous Integration at UIUC

Work on heterogeneous integration methods at the University of Illinois at Urbana-Champaign have focused on epitaxial transfer, as depicted in Fig. 1 below.

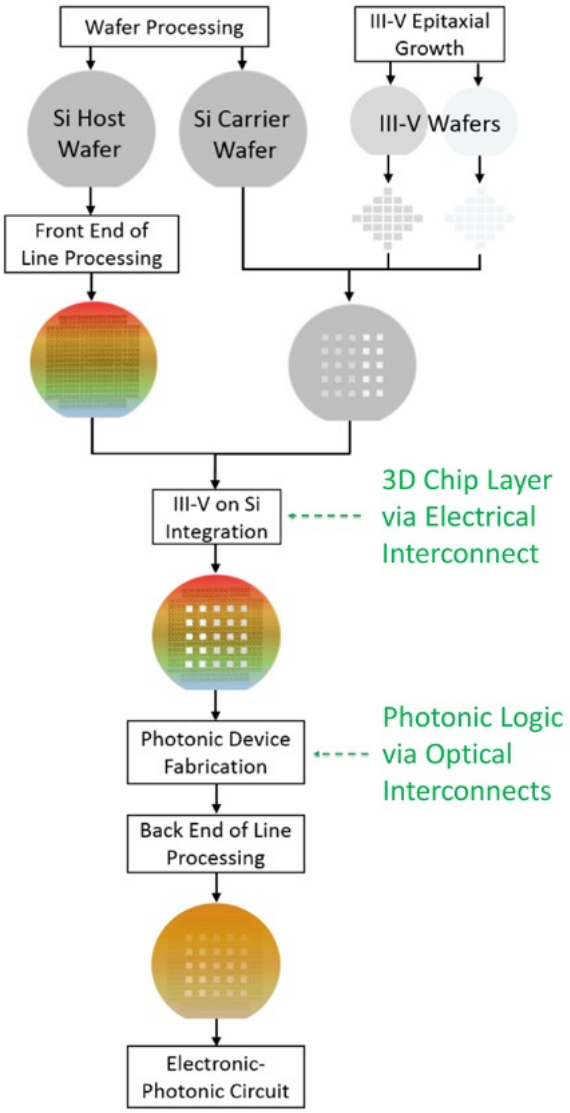

Fig. 1. Depiction of high-level process flow for heterogenous integration via epitaxial transfer using a silicon carrier wafer.

In this method, a first silicon wafer is processed in a standard CMOS wafer fab through the full front-end-of-line process while a second wafer is used as a transfer wafer for other materials such as laser gain structures, modulator structures, detector structures, passive waveguide structures, isolator crystals, or other materials needed to effect a specific device function. Multiple distinct materials can be transferred in a single transfer step. The transfer step may also be repeated to create a 3-D stack of heterogeneously integrated material above the plane of the CMOS host wafer surface. The transfer wafer is prepared by depositing a temporary bonding material such as spin-coat bonding films from AI Technologies. Pieces of III-V epitaxial wafers or other materials are coarsely bonded to the transfer wafer, and lapping, polishing, and plasma or wet chemical thinning are used to reduce the thickness of the bonded material to typically a few microns – approximately the thickness of the epitaxial layers. A hard mask is then deposited and photolithographically defined, and the bonded material is fully removed via wet or dry etching in all unmasked regions. What is left on the transfer wafer are islands of material such as III-V epitaxial device structures defined on the wafer and relative to each other with photolithographic precision.

A scanning electron microscope (SEM) photomicrograph of such an island is shown in Fig. 2 below.

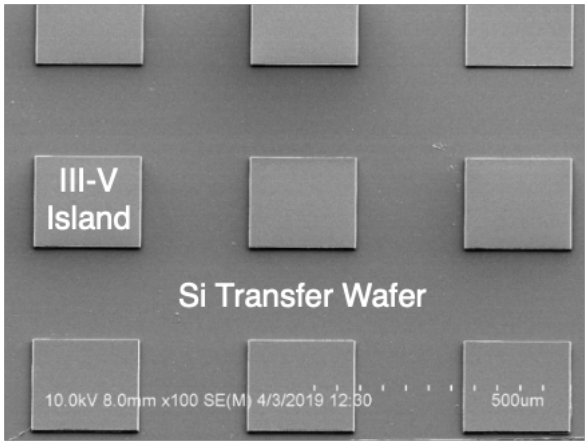

Fig. 2. SEM image of III-V islands of epitaxial material on silicon transfer wafer after patterning and etching to precisely define location.

The III-V islands are composed of an epitaxial layer structure used for photonic devices.

A single wafer bonding step using a permanent bonding material can then be used to bond all of the material on the transfer wafer onto the CMOS host wafer. Given the capability of modern wafer bonding tools, this can be done with micron-level precision at production scale. Fabrication of photonic devices takes place on the silicon CMOS host wafer after the epitaxial transfer process. Optical alignment of individual devices is not required, as all photonic elements are defined within the layer registration specification of the photolithography tool.

Using the above method, light-emitting transistors (LETs) were fabricated on epitaxial material after transfer from a first silicon wafer to a second using the described method [11]. A SEM image of a LET fabricated on transferred material is shown in Fig. 3 below.

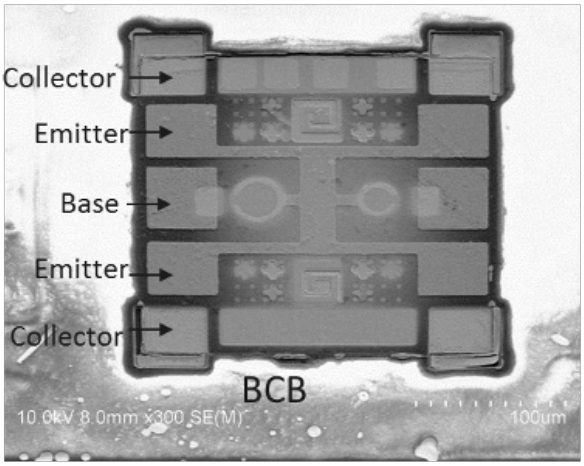

Fig. 3. Light-emitting transistor fabricated on transferred III-V epitaxial material.

The LET devices fabricated via epitaxial transfer have reasonable performance characteristics, and could eventually be used for the integration of on-chip or chip-to-chip optical interconnects.

Conclusion

A review of approaches for the integration of material such as III-V epitaxial device structures onto silicon has been provided, and various challenges have been discussed. A method to overcome these challenges in a wafer-scale process has been explored.

Acknowledgments

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