

A Trimodal Wireless Implantable Neural Interface System-on-Chip

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Abstract—A wireless and battery-less trimodal neural interface system-on-chip (SoC), capable of 16-ch neural recording, 8-ch electrical stimulation, and 16-ch optical stimulation, all integrated on a 5×3 mm² chip fabricated in 0.35- μ m standard CMOS process. The trimodal SoC is designed to be inductively powered and communicated. The downlink data telemetry utilizes on-off keying pulse-position modulation (OOK-PPM) of the power carrier to deliver configuration and control commands at 50 kbps. The analog front-end (AFE) provides adjustable mid-band gain of 55–70 dB, low/high cut-off frequencies of 1–100 Hz/10 kHz, and input-referred noise of 3.46 μ V_{rms} within 1 Hz–50 kHz band. AFE outputs of every two-channel are digitized by a 50 kS/s 10-bit SAR-ADC, and multiplexed together to form a 6.78 Mbps data stream to be sent out by OOK modulating a 434 MHz RF carrier through a power amplifier (PA) and 6 cm monopole antenna, which form the uplink data telemetry. Optical stimulation has a switched-capacitor based stimulation (SCS) architecture, which can sequentially charge 4 storage capacitor banks up to 4 V and discharge them in selected μ LEDs at instantaneous current levels of up to 24.8 mA on demand. Electrical stimulation is supported by 4 independently driven stimulating sites at 5-bit controllable current levels in $\pm(25\text{--}775)$ μ A range, while active/passive charge balancing circuits ensure safety. *In vivo* testing was conducted on 4 anesthetized rats to verify the functionality of the trimodal SoC.

Keywords—trimodal neural interface, optogenetics, switched-capacitor based stimulation, charge balancing, wireless power and data transmission

I. INTRODUCTION

A subset of implantable microelectronic devices (IMD) known as neural interfaces are aimed at establishing a direct communication pathway with the central nervous system (CNS) for understanding of brain functions and performing promising treatment of neurological disorders [1]–[3]. Deep brain stimulation (DBS) has been proven therapeutically effective for

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neurological disorders, such as Parkinson's disease, epilepsy, and Alzheimer's disease [4], [5]. DBS involves injecting a designated amount of charge into the target neural tissue to initiate the functional response of neurons in patients unresponsive to pharmaceutical treatment [6].

In addition to neuromodulation, neural interface devices are also expected to be able to sense and register neural activities with high spatiotemporal resolution [7], [8]. Analyzing neural signals helps researchers to observe and interpret the changes in neural activities in response to various stimulation patterns. The recorded data also provides feedback on the evoked neural activities to help adjust stimulation parameters/patterns to optimize them in terms of efficacy, safety, side effects, and power efficiency in what is known as closed-loop neuromodulation [7], [8]. To meet these requirements, several IMDs capable of neural recording and electrical stimulation have been developed for closed-loop neuromodulation applications [9]–[14].

A much more recent approach to neuromodulation, known as optical stimulation, has rapidly become popular among neuroscientists. It has distinct advantages over electrical stimulation, such as cell-type specificity, sub-millisecond temporal precision, rapid reversibility, and elimination of electrical artifacts, and can potentially substitute/complement traditional neuromodulation [15], [16]. Recent demand on neural interface devices for optical neuromodulation application has resulted in the development of neural interface devices offering optical stimulation capability [17]–[22]. A weakness of these devices from a translational standpoint is their high power consumption, which is inevitable because of the high threshold of light intensity, in the order of 1 mW/mm² at 470 nm, needed to elicit selective neuromodulation. Therefore, it is hypothesized that applying a small subthreshold current during the optical stimulation could reduce the threshold of the optical stimulation, and consequently the power needed for the selective optical stimulation. Therefore, a comprehensive neural interface furnished with both optical and electrical stimulation capabilities, plus neural recording of the evoked activity for closing the loop is expected to offer unprecedented flexibility for end-users to execute sophisticated hybrid neuromodulation paradigms in a closed-loop fashion [23]–[26].

Another key feature, which brings such advanced neural interface devices closer to clinical use is wireless operation in terms of both power delivery and data transmission. The conventional communication pathway requires cable tethering between the device and the external data aggregator, which imposes several limitations for studies of freely behaving

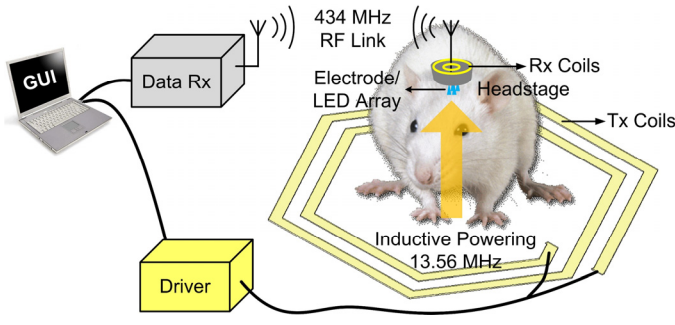


Fig. 1. Conceptual view of wirelessly operating the trimodal SoC built in a device, which is mounted on the head of a freely moving rat.

animals [27]-[29]. These limitations include potentially biased behavioral outcomes, tangling or breakage of cables during experiments, and potential discomfort and stress of the animal subjects [30]-[32]. Although battery powered IMDs are available for low power applications, such as pacemakers or DBS, they do not seem to be able to support long term optical stimulation experiments even in small animal subjects. Optical stimulation suffers from high power consumption because of the high threshold of light intensity needed to elicit selective neuromodulation, which at 470 nm is $\sim 1 \text{ mW/mm}^2$ [33].

In this paper, we elaborate on [26], where we reported for the first time a fully-integrated, wireless and battery-less trimodal neural interface system-on-chip (SoC) for 16-channel neural recording, 8-channel electrical stimulation, and 16-channel optical stimulation. We confirmed the functionality of the proposed trimodal SoC by demonstrating evoked neural activities and immunostained tissue response *in vivo*. An overview of the experimental setup for wirelessly operating the trimodal SoC is given in Section II. Section III presents a detailed design of the SoC. Section IV shows benchtop

measurement results. Section V and Section VI describe the *in vivo* and *in vitro* results, respectively, followed by discussion and conclusion.

II. SYSTEM ARCHITECTURE

Fig. 1 shows the conceptual view of the experimental setup, including the trimodal SoC and the wireless power/data links, for performing behavioral studies on small freely moving animals, such as rodents. The SoC, together with several commercial-off-the-shelf (COTS) components (e.g. passive capacitors and inductors), receiver (Rx) coils, and a transmitter (Tx) antenna, can be incorporated in a head-mounted device, which unlike cables, will not bias the animal subject's behavior.

Wireless power delivery to the trimodal SoC is achieved through a multi-coil inductive link operating at 13.56 MHz. The Tx coils in this case can be a wirelessly powered rodent homecage, like the EnerCage-HC system [31], [32]. Wireless data communication with the SoC is bi-directional. The downlink data telemetry, which is achieved by modulating the amplitude of the power carrier of the inductive link, delivers configuration and control commands to the SoC. Once receiving the user-defined parameters, the SoC will generate stimulation pulses to either drive μLEDs for optical stimulation or inject current through stimulation sites for electrical stimulation, while recording evoked neural activities through a separate electrode array. For the uplink data telemetry, the recording data is digitized and transferred to the data Rx outside the homecage through a separate 434 MHz RF link.

Considering the large volume of the recorded raw data, the receiver (Data-Rx) in this case is a custom-designed data acquisition system, which incorporates multiple BladeRF software defined radios (SDRs) for complete spatial coverage without any blind spots that operate in parallel via USB links to

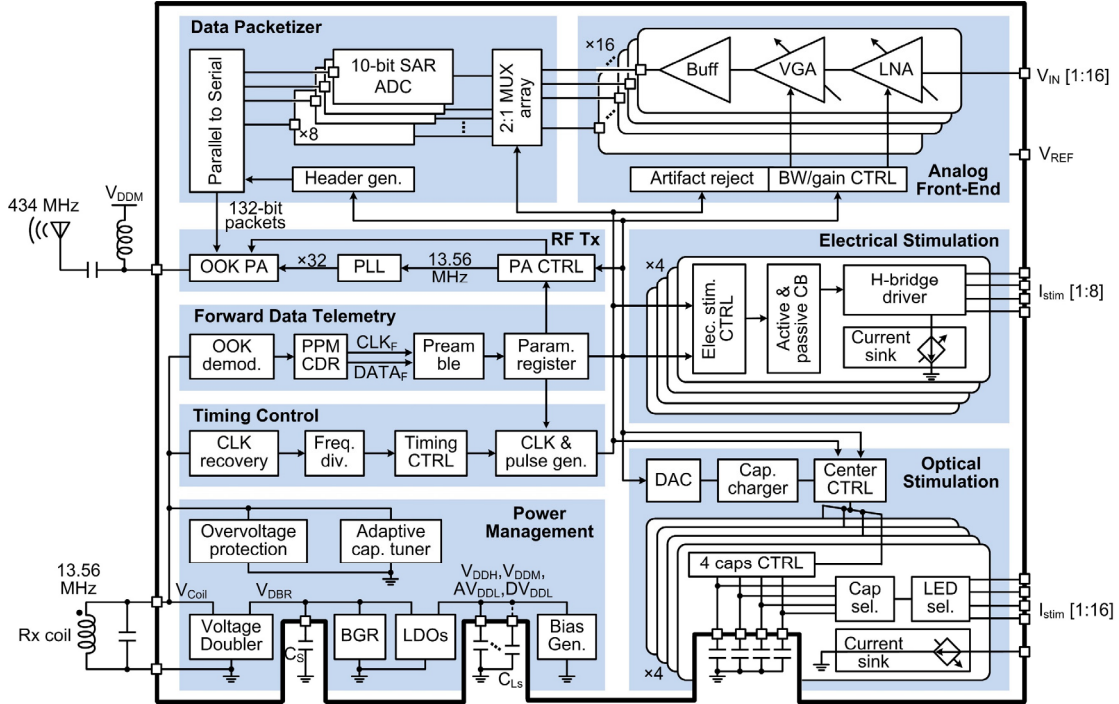


Fig. 2. Overall block diagram of the trimodal SoC.

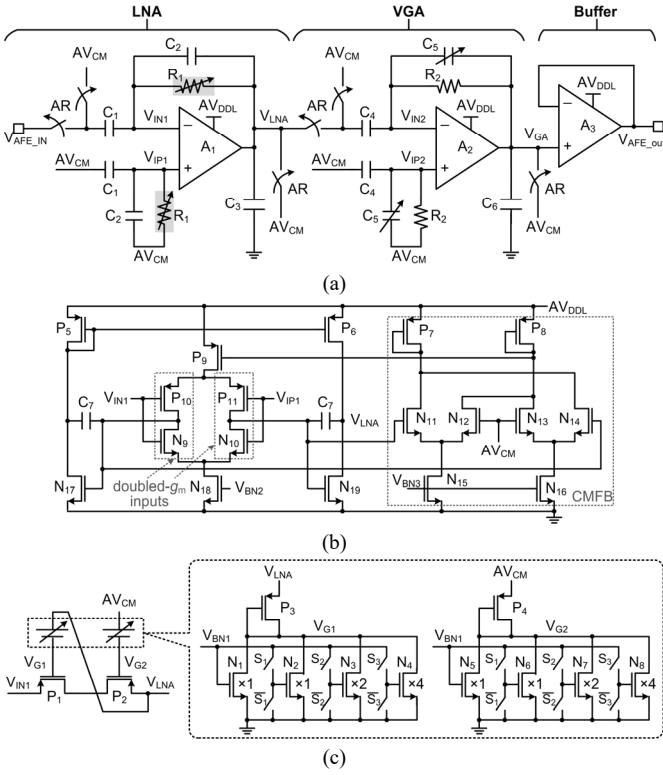


Fig. 3. Schematic diagram of (a) a single AFE channel, (b) the amplifier, A_1 , and (c) the adjustable pseudo resistor, R_1 .

a PC that performs real-time data recovery, processing, display, and storage [34].

III. TRIMODAL SoC ARCHITECTURE

Fig. 2 shows the top-level block diagram of the WINeRS-9 SoC. The power management block generates regulated supplies (1.8 V, 3.3 V, and 4.2 V) and biasing for the rest of the SoC from the 13.56 MHz power carrier, while an adaptive capacitor tuner compensates the resonance capacitance variations. The timing control block recovers a 13.56 MHz clock from the power carrier and generates control signals to sync other blocks. The forward data telemetry block recovers adjustable parameters from the on-off-keying (OOK) modulated coil voltage, V_{COIL} , to configure stimulation and recording settings.

The SoC generates stimulation pulses based on the user-defined stimulation types and patterns. Optical stimulation employs a switched-capacitor based stimulation (SCS) architecture, which can deliver instantaneous currents large enough for the intensity of light produced by the flashing μ LEDs to be large enough to surpass the optogenetic neuromodulation threshold without overloading the inductive link or creating a mismatch [35]. For electrical stimulation, an H-bridge drives stimulating sites with constant current in a biphasic-bipolar fashion, while both active and passive charge balancing (CB) circuits can be engaged to ensure the residual voltage difference across a pair of active site staying within a safe window (± 50 mV) [36], [37].

The recording function is performed by 16 analog front-end (AFE) channels, which amplify and filter recorded neural signals with the user-defined gain and bandwidth. An artifact rejection

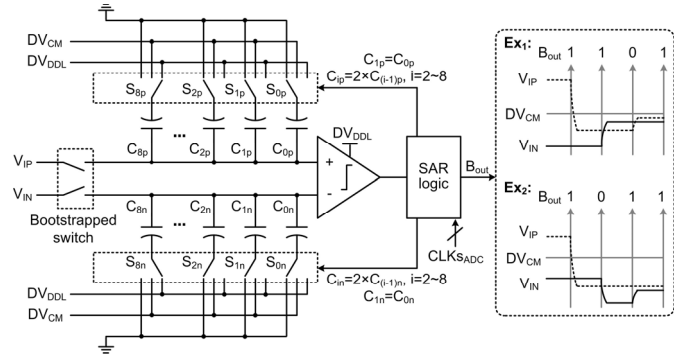


Fig. 4. Schematic diagram of the 10-bit SAR ADC, with two examples of the comparator input waveforms.

(AR) circuit is adapted to prevent the AFE from saturation during stimulation periods. Each successive approximation register (SAR) analog-to-digital converter (ADC) takes sample alternatively between two AFE channels at 50 kS/s, resulting in 25 kS/s for each channel. Each digitization cycle generates 132 data bits, which are serially sent to the RF Tx block, in which the serial data bit stream OOK modulates a 434 MHz carrier before being transmitted by the PA through a small monopole antenna. The power supply of the 434 MHz matching network is provided by one of the on-chip LDOs. Each 132-bit data package produced includes parity check bit and 11-bit preamble ahead of the ADC raw data in order to improve the accuracy of packet detection on the data Rx side.

Each AFE channel includes three stages, as shown in Fig. 3a: a low noise amplifier (LNA), a variable gain amplifier (VGA), and an analog buffer. The LNA and VGA employ DC blocking capacitors, C_1 and C_4 , at the input to remove DC offset, while their common-mode voltages are biased at half of the supply voltage, AV_{CM} . The LNA utilizes doubled transconductance (g_m) input stages to help achieve low input-referred noise [38]. The common-mode feedback (CMFB) amplifier sets the internal voltage of doubled- g_m input stages to AV_{CM} . The buffer is able to drive the large switched-capacitor array of the SAR ADC. The ‘AR’ pulse, synchronized with the stimulation pulse, detaches the AFE from the recording electrodes and connects the inputs and outputs of LNA and VGA to AV_{CM} so that the recording function of the AFE can recover right after the stimulation pulse is over. The low cutoff frequency of the AFE is set by the LNA at $1/(2\pi \cdot R_1 \cdot C_2)$, while the high cutoff frequency of the AFE is determined by the VGA bandwidth. The mid-band gain of the AFE is determined by the gains of the LNA and VGA, which are set by C_1/C_2 and C_4/C_5 , respectively. C_5 is a 3-bit binary-weighted capacitor array and adjusts the VGA gain. In Fig. 3c, R_1 is implemented using a cross-coupled pseudo resistor, which prevents DC current flow through transistors, P_1 and P_2 [39]. This pseudo resistor and its 3-bit programmable current source sets the low cutoff frequency.

We adopted the low power and robust SAR ADC architecture in [40] and modified it for this particular application. In the sampling phase, the input signals, V_{IP} and V_{IN} , are sampled onto the top plates of the capacitor arrays through bootstrapped switches. In the following comparison phase, the bootstrapped switches turn off and the bottom plates of the capacitor arrays are switched between DV_{DDL} , DV_{CM} , and

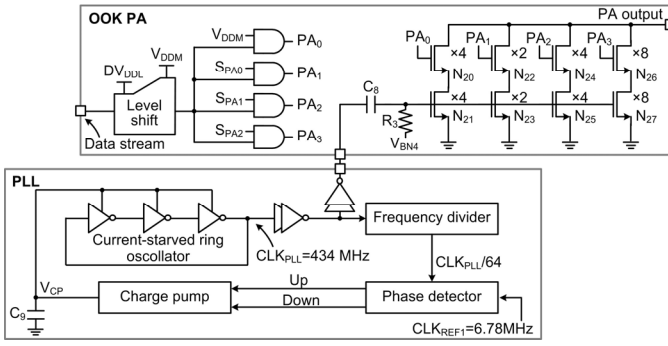


Fig. 5. Schematic diagram of the RF Tx, including PLL and OOK PA.

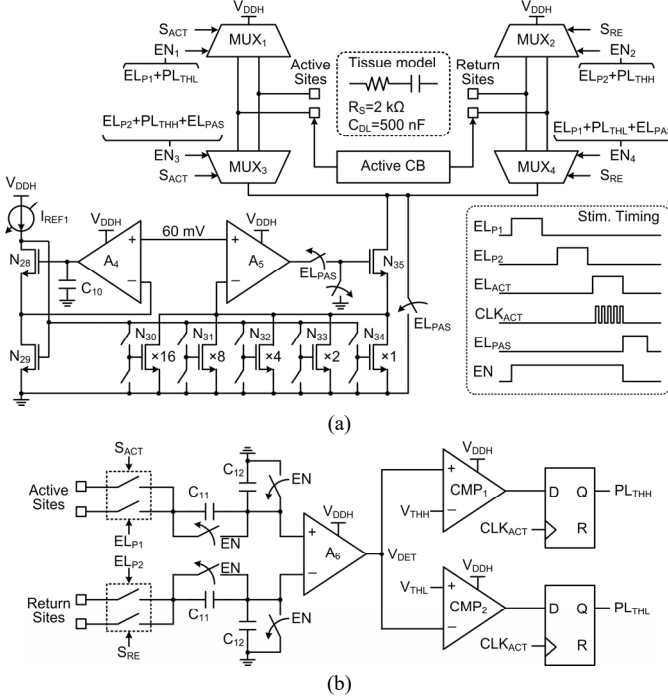


Fig. 6. Schematic diagram of (a) a single group in the electrical stimulation block and (b) the active CB circuit.

ground, where DV_{DDL} is the digital supply voltage, and DV_{CM} equals $DV_{DDL}/2$. By taking the capacitor switching scheme in [40], the number of capacitors in this ADC is reduced by 75% over the conventional architecture in [41]. Moreover, by dramatically reducing energy consumption in the first 3 bit-cycles and reducing the switching step of each capacitor by half, power saving can be achieved.

In Fig. 4, the comparator input waveforms resulted from the switching scheme in [40] show that if '1' is generated after the second bit cycle, the comparator input will successively approach to DV_{CM} in the following bit cycles; otherwise, the comparator input will successively deviate from DV_{CM} . However, thanks to the halved switching step, the comparator input derivation from DV_{CM} is still less than that in the monotonic switching scheme in [41].

As shown in Fig. 5, the RF Tx mainly consists of a phase-locked loop (PLL) and OOK PA [42]. In the PLL block, the clock, CLK_{PLL} , generated by a 3-stage ring oscillator is divided by 64. The phase detector compares the divided clock with a 6.78 MHz reference clock, CLK_{REF1} , which is derived from the

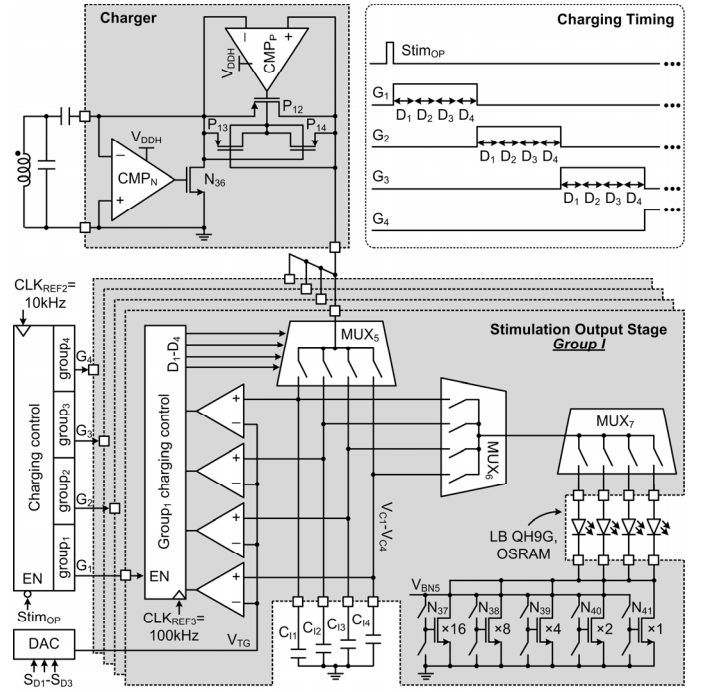


Fig. 7. Schematic diagram of the optical stimulation block.

13.56 MHz clock. The charge pump charges/discharges the capacitor, C_9 , to control the bias voltage of the ring oscillator, V_{CP} , based on the 'Up/Down' output pulses from the phase detector. When the loop is stabilized, CLK_{PLL} becomes $64 \times CLK_{REF1} = 434$ MHz, which is buffered to drive the PA. The output power of the OOK PA is 3-bit adjustable. The data bit stream is serially sent out by OOK modulating the PA carrier at 6.78 Mbps.

The electrical stimulation block includes four independent groups, one of which is shown in Fig. 6a. A current stimulator employs four 4:1 multiplexers (MUXs) in an H-bridge configuration, which interface with two active and two return sites. A controller selects the MUXs in pairs to generate anodic and cathodic stimulation phases with a single current driver, which consists of a 5-bit current steering digital-to-analog converter (DAC), implemented with low dropout transistors [43]. The feedback loops, using amplifiers A_4 and A_5 , set the drain-source voltages of N_{30} - N_{34} transistors at 60 mV in the triode region to reduce the voltage headroom of the current driver output, while boosting its output impedance [37]. As shown in Fig. 6b, the active CB circuit monitors the voltage difference between the active and return stimulating sites selected by control signals, S_{ACT} and S_{RE} , during the stimulation and active CB periods, when $EN = 1$. When the stimulation starts, $EN = '1'$, the site voltage difference is capacitively attenuated before being converted to a single-ended output voltage, V_{DET} . If the site voltage difference goes above a ± 50 mV window, V_{DET} will exceed the bounds set by V_{THH} and V_{THL} . In response, a sequence of pulses, either PL_{THH} or PL_{THL} will be generated to control the four MUXs, which will push or pull additional current pulses into the tissue to keep the sites' voltage difference within the safe window. After the active CB period, the passive CB circuit is then activated to further remove the residual charge by shorting the two stimulating sites to ground.

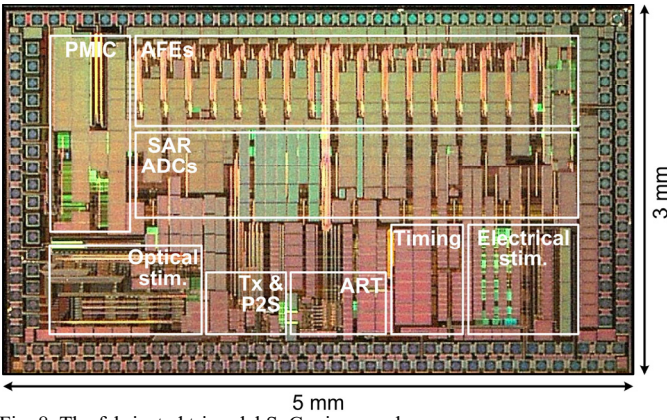


Fig. 8. The fabricated trimodal SoC micrograph.

Fig. 7 shows a simplified schematic diagram of the optical stimulation block, which utilizes the SCS architecture [35]. The capacitor charger consists of two switches driven by two high-speed comparators, CMP_N and CMP_P , sequentially charging four off-chip capacitor banks during their corresponding charging periods, G_1 - G_4 , which are adjustable by the charging control circuit. The charging cycle continues until the next stimulation flag signal, $Stim_{OP}$, arrives. Each capacitor bank includes four surface-mount (SMD) capacitors. In each group, the charging control circuit adjusts the charging periods, D_1 - D_4 , for the 4 capacitors, C_{11} - C_{14} , to be charged in sequence to a target voltage, V_{TG} , set by a 3-bit DAC, through MUX_5 . MUX_6 controls which capacitor(s) of C_{11} - C_{14} to dump their charge into one of the 4 μ LEDs, decided by the MUX_7 , for performing optical stimulation with adjustable pulse width and frequency. A current limiter, implemented using a 5-bit current sink with binary-weighted transistors, sets an upper bound to the exponentially decaying current that flows through the μ LED.

IV. MEASUREMENT RESULTS

The die photo of the trimodal SoC, shown in Fig. 8, was fabricated in the TSMC 0.35- μ m 4M2P standard CMOS process and occupies 5×3 mm² of silicon area including pads.

Fig. 9a presents the measured AFE input-referred noise spectrum. The thermal noise level is observed at 10 nV/ $\sqrt{\text{Hz}}$ and $1/f$ noise corner occurs at 20 Hz. Integration under this curve from 1 Hz to 50 kHz yields a root mean square (RMS) noise voltage of 3.46 μ V_{rms} for the AFE, with a noise efficiency factor (NEF) of 2.95 [38]. Fig. 9b presents the measured frequency response of the AFE. The low cutoff frequency of the AFE is adjustable from 1-100 Hz, while the gain of the AFE is changed from 55-70 dB. The high cutoff frequency of the AFE, determined by the VGA bandwidth, is at 10 kHz. Fig. 9c shows measured waveforms of electrical stimulation and stimulus artifact rejection. The SoC injects a series of ± 500 μ A current pulses into a tissue model consisting of $R_S = 2$ k Ω and $C_{DL} = 500$ nF connected in series [37], while amplifying and filtering a 1 mV_{pp}, 600 Hz sinusoidal input. When the stimulation starts, 'AR' signal is generated to force the AFE output staying at 0.9 V and to recover the recording function in 0.4 ms after the stimulation, protecting the AFE against large stimulus artifacts.

With a 1.8 V_{pp}, 400 Hz sinusoidal waveform applied to the ADC input, we applied 2048-point fast-Fourier transformation

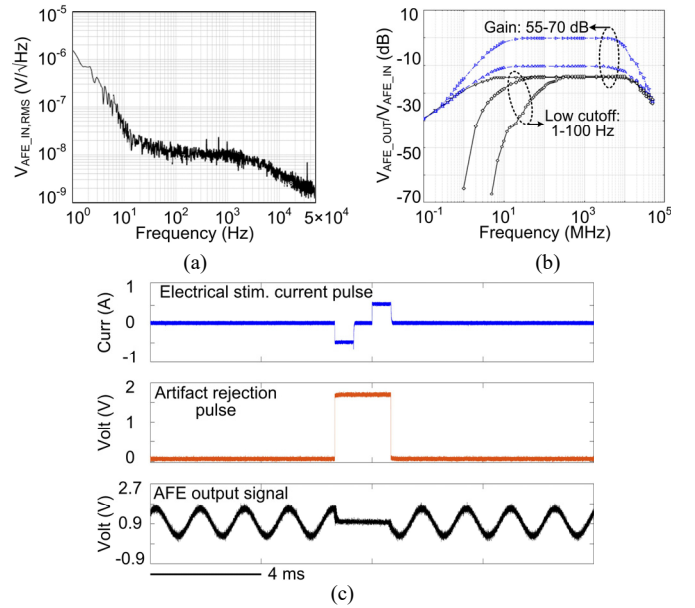


Fig. 9. Measurement results of (a) input-referred noise spectrum, (b) frequency response of the AFE, and (c) stimulus artifact rejection.

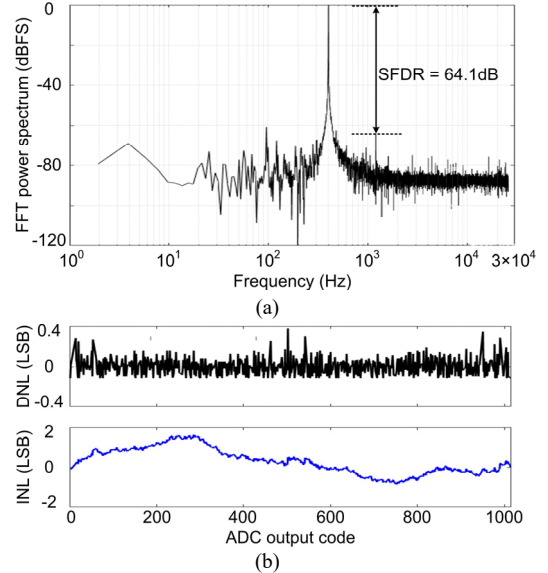


Fig. 10. (a) Measured 2048-point FFT power spectrum of the ADC output and (b) DNL and INL of the ADC.

(FFT) on the ADC output data bits. The produced FFT power spectrum indicates signal-to-noise ratio (SNR) of 54.2 dB and spurious-free dynamic range (SFDR) of 64.1 dB, representing effective number of bits (ENOB) of 8.7. To accurately measure differential nonlinearity (DNL) and integral nonlinearity (INL), a 0-1.8 V linear ramp with 100 bits per ADC output code was applied to the ADC, resulting in the DNL/INL resolution of 0.01 least significant bit (LSB). In Fig. 10b, the DNL and INL are within (+0.39, -0.12) LSB and (+1.50, -0.75) LSB, respectively.

Fig. 11a shows the transient data transmission waveforms. The data bit stream OOK modulates the 434 MHz PA carrier. The PA with its output matched to the 50 Ω impedance of the antenna transfers the data bits at a rate of 6.78 Mbps. Fig. 11b shows the measured PLL phase noise, which is -95.5 dBc/Hz at 1 MHz offset from 434MHz carrier. The spurs below 1 MHz are

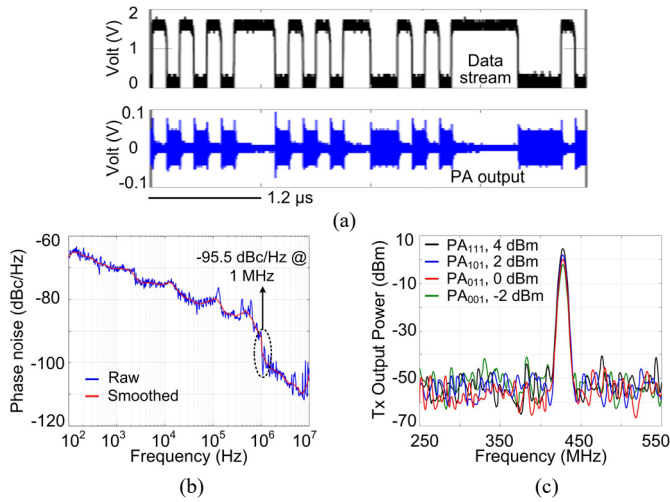


Fig. 11. Measurement results of (a) data stream at the PA output, (b) PLL phase noise, and (c) Tx output power as a function of its 3 control bits.

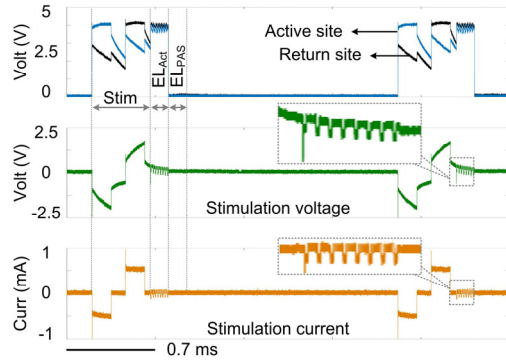


Fig. 12. Measured stimulation waveforms with active CB being activated.

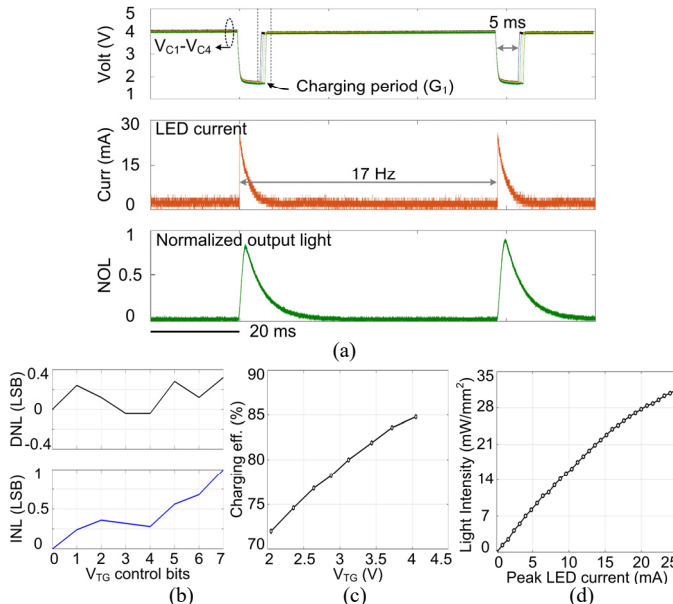


Fig. 13. Measurement results of (a) charging a capacitor bank up to 4 V and discharging in a selected μLED for optical stimulation, (b) DNL and INL of the 3-bit DAC, (c) charging efficiency at different V_{TG} , and (d) light intensity of the selected μLED as a function of the μLED current.

caused by interference from low-frequency reference clocks in the SoC. The induced interference on the 434 MHz carrier

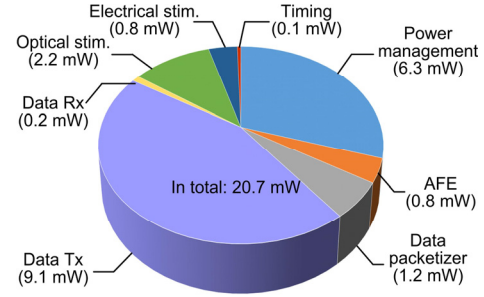


Fig. 14. Power consumption of the main blocks in the trimodal SoC

TABLE I: TRIMODAL SOC MEASURED SPECIFICATIONS

Optical Stimulation		Electrical Stimulation	
V_{TG}	2–4 V, 3 bits	Charge balance	Active+Passive
Freq.	2–50 Hz, 4 bits	Freq.	8–400 Hz, 4 bits
Pulse width	1.25–20 ms, 4 bits	Pulse width	40–640 μs, 4 bits
Current	0.8–24.8 mA, 5 bits	Current	±(25–775) μA, 5 bits
Light intensity	0–31.5 mW/mm ² , 5 bits	Interphase delay	40–640 μs, 4 bits
ADC		Data Tx	
Sampling rate	50 kS/s	Data carrier	RF 434 MHz, OOK
FoM	78.6 fJ	Packet loss rate	<0.13%
DNL	(-0.12–0.39) LSB	Tx-Rx distance	Up to 150 cm
INL	(-0.75–1.5) LSB	Date rate	6.78 Mbps
SNR	54.2 dB	Output power	-3–4 dBm, 3 bits
SFDR	64.1 dB	Data Rx	
ENOB	8.7	Data carrier	Inductive link, 13.56 MHz, OOK
Neural Recording		Data rate	50 kbps
LNA gain	40 dB	SoC	
VGA gain	15–30 dB, 3 bits	Chip area	3×5 mm ²
Low cut-off	1–100 Hz, 3 bits	Average power consumption	20.7 mW
High cut-off	10 kHz	Supply volt.	1.8/3.3/4 V
Input-referred noise	3.46 μVrms with in 1 Hz–50 kHz	Voltage doubler eff.	82%
NEF	2.95		
Recovery time	<0.4 ms		

frequency is small, which does not corrupt functionality. Fig. 11c shows the measured PA output power under four different settings. The maximum output power of the PA is 4 dBm.

Fig. 12 presents the measured electrical stimulation waveforms while delivering current pulses with ±550 μA and 150 μs in amplitude and width, respectively. Pulses are delivered to the tissue model at 400Hz with 120 μs interphase delay. After stimulation, the voltage difference between two stimulating sites exceeds the upper bound of the ±50 mV safe window. The active CB circuit injects a series of 60 μA cathodic current pulses with 20 μs pulse width within 150 μs. It can be seen that the active CB circuit successfully returns the site voltage difference back within the safe window.

Fig. 13a presents the SCS operation to conduct optical stimulation with 5 ms pulse width at a rate of 17 Hz. The four capacitors in each group are charged to 4 V, and all four are selected to dump their charge into a selected μLED, creating an exponentially decaying current, which peak is limited to 24.8 mA. The emitted light from the μLED during stimulation pulse was collected by a photodetector (Newport 883-SL) connected to an optical power meter (Newport 1835-C). The normalized output light (NOL) expectedly follows the stimulation current variation with a slight delay. After each stimulation, all four capacitors are recharged back to 4 V. The target charging voltage, V_{TG} , is adjustable from 2 V to 4 V by a 3-bit DAC,

which DNL and INL are 0.32/-0.04 LSB and 1/0 LSB, respectively (Fig. 13b). The charging efficiency of this circuit changes from 72% to 84.8% depending on the target voltage, as shown in Fig. 13c. The charging efficiency is defined as the stored DC energy in the capacitor banks over the total input energy of the capacitor charging block during the charging period. Fig. 13d shows the light intensity under different current limits, which matches the μ LED specifications [44]. We used μ LED (TR2227TM, Cree) with a size of $220 \times 270 \times 50 \mu\text{m}^3$. The light intensity is calculated as the amount of light collected during a pulse divided by the surface area of the μ LED, $220 \times 270 \mu\text{m}^2$. Ignoring the losses, the peak value of the light intensity under 24.8 mA is 31.5 mW/mm^2 , which is well above the 1 mW/mm^2 threshold of effective neuromodulation [33].

The average SoC power consumption is 20.7 mW when all three functions, neural recording, optical stimulation, and electrical stimulation, are enabled, and the two stimuli amplitudes are maxed out. The pie chart in Fig. 14 shows that the data Tx has the highest power consumption followed by the power management block. Table I summarizes the measured specifications of the trimodal SoC prototype.

V. IN VIVO EXPERIMENT

A. In Vivo Experiment Design

To verify the functionality of the trimodal SoC, we conducted *in vivo* experiments on two male adult Sprague Dawley rats (350-400 g) by following our established protocols approved by the Institutional Animal Care and Use Committee (IACUC) at Michigan State University. We injected adeno-associated virus (AAV) that carries optogenetics opsin (AAV-hSyn-hChR2 (H134R)-mCherry; UNC Vector Core) into each subject's bilateral visual cortex (V1), using the stereotaxic surgery protocol in [20]. Then, we housed the subjects separately in the animal facility for postoperative recovery. For optogenetic neuromodulation, we waited 4 weeks following the virus injection to ensure that cortical neurons have expressed light excitability in channelrhodopsin-2 (ChR2).

Although the *in vivo* setup in Fig. 15a shows the optical stimulation experiment, the same setup was used for performing electrical stimulation. Each subject received unilateral stimulation on the right V1 lobe, while the left V1 lobe of the same animal acted as control. A flexible 4×4 electrode array with channel arrangement shown in Fig. 15c was attached to the right V1 lobe. In Fig. 15b, a PA wirelessly delivered power to a trimodal evaluation board through a resonance-based multi-coil inductive link formed by a Tx coil, L_1 , and two Rx coils, L_3 and L_4 . The current trimodal evaluation board with dimensions of 7 cm (length) $\times$ 5 cm (width) $\times$ 3 cm (height) and weight of 17 g was designed for verifying the functionality of the trimodal SoC in experiments with anesthetized animals. A microcontroller unit (MCU) OOK modulated the power carrier of the inductive link to send user-defined stimulation and recording parameters to the SoC. The SoC generated stimulation pulses, acting on the tissue where the Ch-9 electrode was located. At the same time, the SoC recorded local field potentials (LFP) from the 4×4 electrode array. The digitalized LFP data was wirelessly sent to our data acquisition system, in which a pair of SDR Rx with

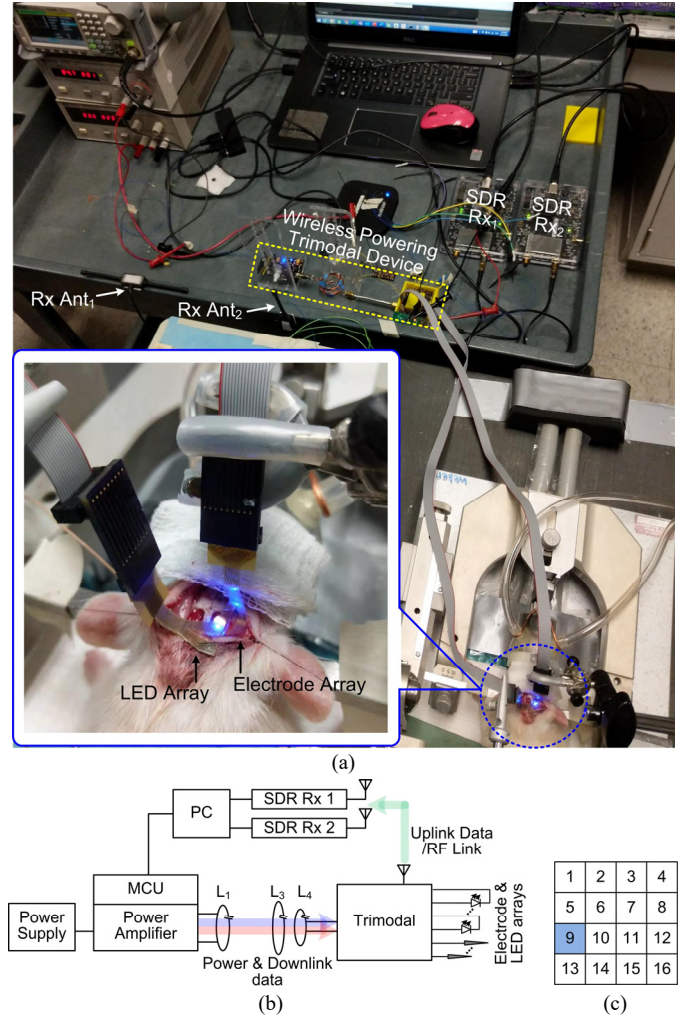


Fig. 15. (a) *In vivo* experimental setup of performing optical stimulation. (b) Block diagram of the experimental setup. (c) Arrangement of the recording electrodes in an array.

orthogonal antennas picked up the OOK modulated RF signal and recovered the LFP data.

In optical stimulation, a flexible $4 \times 4 \mu\text{LED}$ array was placed above the electrode array and aligned to locate the selected μLED ($220 \times 270 \times 50 \mu\text{m}^3$, TR2227TM, Cree) above the Ch-9 electrode. The selected μLED was driven by pulses with 5 ms width, 8 mA current limit, and 2 Hz frequency, resulting in light intensity of 11.8 mW/mm^2 . In electrical stimulation, the SoC injected $\pm 100 \mu\text{A}$ pulses into a tungsten electrode, which reached the tissue at the depth of $100 \mu\text{m}$ underneath the Ch-9 electrode. The current pulses had $150 \mu\text{s}$ width, $150 \mu\text{s}$ interphase delay, and 8 Hz pulse rate.

In each stimulation mode, we compared the LFPs recorded in 4 conditions: LFP-I and LFP-II are LFPs recorded from Ch-9 and Ch-4 using trimodal SoC, respectively; LFP-III is spontaneous LFPs recorded from Ch-9 using trimodal SoC when stimulation is completely off (baseline), and LFP-IV is LFPs recorded from Ch-9 using a commercial Intan system (RHD2132) without artifact rejection function.

B. Electrical Stimulation Results

Fig. 16 compares the LFPs recorded in the abovementioned

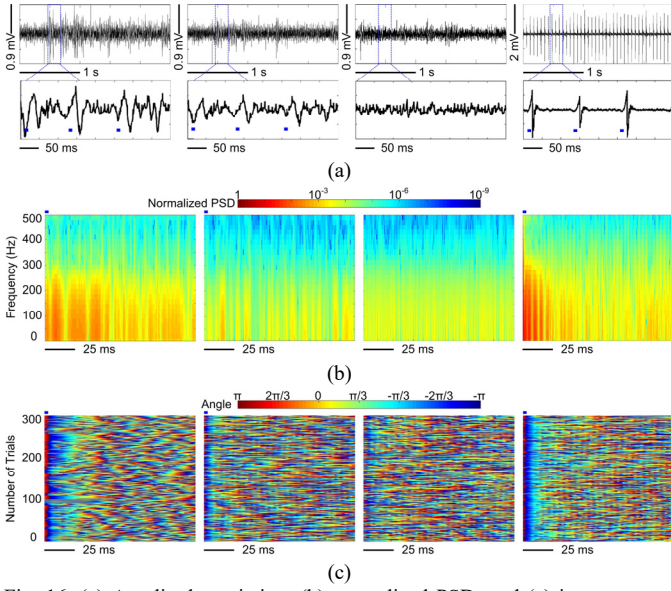


Fig. 16. (a) Amplitude variation, (b) normalized PSD, and (c) instantaneous phases of LFP-I, LFP-II, LFP-III, and LFP-IV (from left to right) when the subject received electrical stimulation.

4 conditions in terms of amplitude, power spectrum, and phase synchronization. Fig. 16a shows the sample recorded LFPs over a 2.5 s time span. The stimulation flags in the close-up view mark the stimulus pulses. Compared to the baseline, LFP-I and LFP-II were evoked by the electrical stimulation. Due to the reduced stimulation effect at Ch-4 location, LFP-II has lower amplitude than LFP-I. Without the artifact rejection function, large stimulus artifacts were observed in LFP-IV. In contrast, LFPs recorded using trimodal SoC were effectively protected from stimulus artifacts. We applied FFT on averaged LFPs over 100 electrical stimulations, resulting in time-frequency maps of the color-coded normalized power spectral density (PSD) [45]. As expected, LFP-I showed significant PSD upregulation. In contrast, the reduced stimulation effect in LFP-II only caused a slight increase in PSD as compared to the spontaneous LFPs. In LFP-IV, increase PSD at the onset of stimulus can be attributed to the artifacts. Moreover, we applied Hilbert transformation to extract the color-coded instantaneous phases of LFPs within 1-25 Hz frequency band over 300 stimulations [46]. The instantaneous phase of the LFPs over 300 stimulations were aligned to the concurrence of the stimulus and stacked, as shown in Fig. 16c. The spontaneous LFPs with random phases did not show phase synchrony. In contrast, long and reliable phase-locked synchronization was observed from the LFP-I across 300 stimulations. The instantaneous phase resulted from the LFP-II showed slight synchronization, as expected. The LFP-IV also had strong phase synchronization. However, it was induced by the strong and periodically repeated artifacts at the onset of each stimulation.

C. Optical Stimulation Results

Similarly, by comparing the amplitude, power spectrum, and instantaneous phase of the LFPs recorded in the above 4 conditions, we prove the efficacy of optical stimulation. Fig. 17 shows that LFP-I waveforms, which are closest to the stimulation source, have the largest amplitude variations,

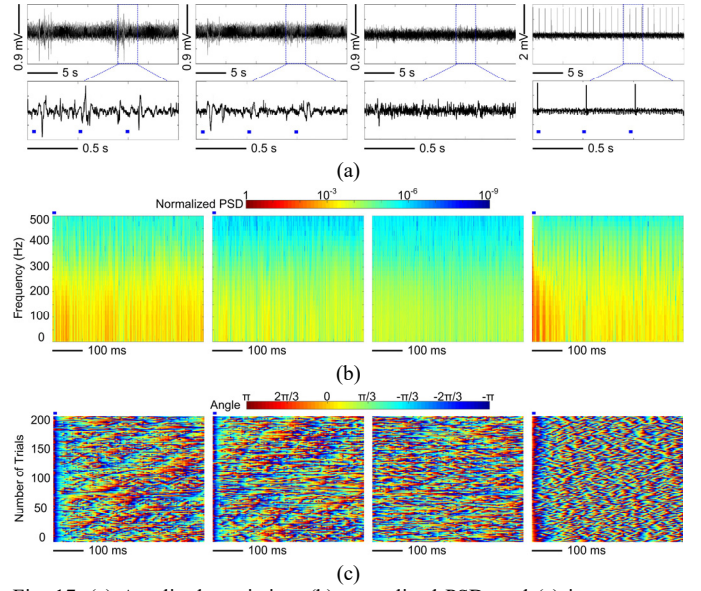


Fig. 17. (a) Amplitude variation, (b) normalized PSD, and (c) instantaneous phases of LFP-I, LFP-II, LFP-III, and LFP-IV (from left to right) when the subject received optical stimulation.

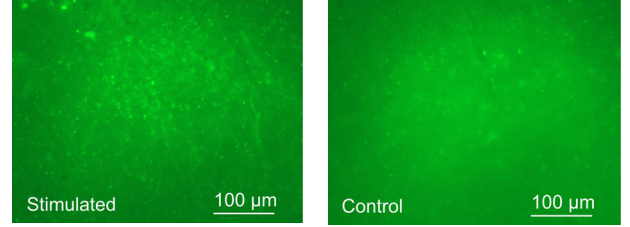


Fig. 18. C-Fos expression in the right (stimulated) vs. left (control) V1 lobes.

highest PDS elevation, and longest phase synchronization, compared to LFP-II and LFP-III. Moreover, although we still observed light-induced photoelectric artifacts along with LFPs in LFP-IV, the photoelectric artifacts were much smaller, compared to the electrical artifacts seen in Fig. 16. This result confirms a key advantage of optical stimulation over electrical stimulation, which is less disturbance in the simultaneous neural recording [15], [47].

In addition to LFP comparison, we conducted immunostained tissue analysis. Fig. 18 shows the c-Fos fluorescent images of the post-processed 50 μ m-thickness brain section, taken under 10 $\times$ magnification. The green fluorescence spots indicated Chr2 transfected cells expressing c-Fos, a biomarker indicating the upregulation of neuronal activities induced by optical stimulation [48]. As opposed to the control side, increased c-Fos expression was observed in the stimulated V1 lobe.

VI. IN VITRO EXPERIMENT

We have tested the feasibility of wirelessly powering the trimodal SoC *in vitro* using the EnerCage-HC system [31], [32]. In the experimental setup shown in Fig. 19, the EnerCage-HC system, built on a 13.56 MHz resonance-based 4-coil inductive link, delivered power and user-defined parameters to the trimodal SoC prototype board, which in turn drove a selected μ LED while acquiring pre-recorded neural signals. Digitalized data was wirelessly transmitted via the 434 MHz RF link and

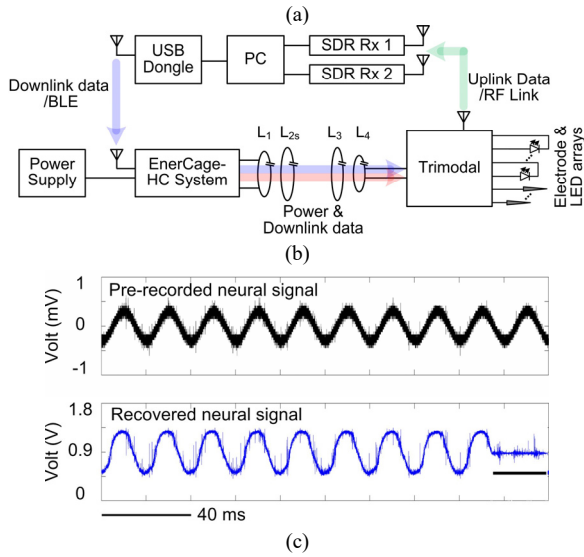
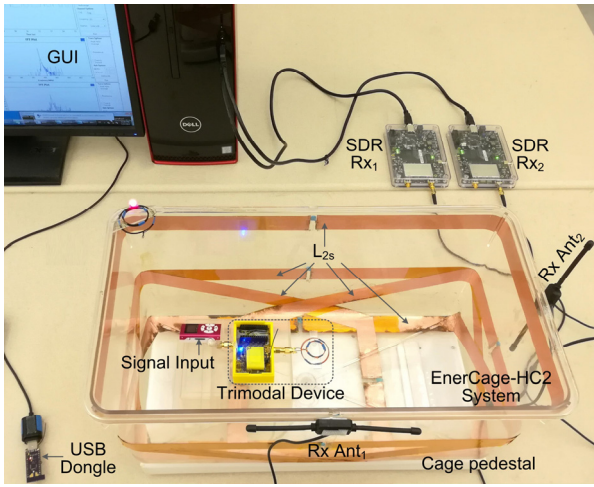


Fig. 19. (a) Experimental setup of wirelessly powering the trimodal evaluation board in the EnerCage-HC system. (b) Block diagram of the experimental setup. (c) Recovered neural signal from the pre-recorded neural signal.

picked up by the two SDR data Rxs outside of the homecage. To emulate a real recording, the pre-recorded neural signal contains spikes in hundreds of μV_{pp} range added to a 50 Hz sinewave, which represents LFP in the background. Fig. 19c

shows a short 2 s interval of the pre-recorded neural signal that was applied to the AFE (upper trace) and the recovered data by the SDR Rxs (lower trace). The stimulation flag indicated the optical stimulation pulse. In the trimodal SoC, the low cutoff frequency of the AFE was set at 1 Hz. It can be seen that both low-frequency LFP and spikes can be recovered. Besides, at the onset of optical stimulation, the recovered neural signal was pulled to the half of the supply voltage, which was performed by the artifact rejection circuit to protect the AFE from stimulus artifacts. These results can demonstrate the functionality of the trimodal SoC, wirelessly powered in the EnerCage-HC.

VII. DISCUSSION

The main novelty of our work lies at the successful combination of circuit blocks for three individual modes of interfacing with the central nervous system (CNS) into a fully-integrated, wireless and battery-less, multi-functional and versatile neural interface SoC. As such, each circuit block was carefully designed for the purposes of power efficiency, design robustness, and reliable integration with each other as a whole. Besides, the specifications of the individual modalities remain competitive with state-of-the-art, such as the high current driving capability of the optical stimulation front-end, low noise level of the recording front-end, etc. The combination of benchtop, *in vitro*, and *in vivo* results also validate the functionality and reliability of the novel trimodal SoC for its intended application.

Table I benchmarks the trimodal SoC prototype against recently reported neural interfaces, presenting its key advantages over the prior art. In terms of application, the trimodal SoC features wireless power and data transmission, which allows for long-term *in vivo* tests on freely behaving animal subjects, and a step closer to clinically viable devices in which wireless operation is necessary. Although using battery is a simpler option for power delivery, its limited lifetime will limit the experiment duration, not suitable for high power applications, such as optical stimulation.

In terms of system integration, this trimodal SoC features high-level integration by combining 16 neural recording channels, 8 biphasic electrical stimulation channels, 16 SCS-based optical stimulation channels, ADCs, wireless data Tx,

TABLE II: BENCHMARKING OF STATE-OF-ART MULTIFUNCTIONAL NEURAL INTERFACE SOC

Publication	2017 [11]	2019 [14]	2018 [24]	2018 [19]	2019 [25]	This work
Technology	0.13- μm	0.18- μm +FPGA	0.18- μm	0.13- μm +MCU	0.18- μm +COTS	0.35- μm
No. interfacing modalities	2	2	2	2	3	3
No. recording channels	64	128	N/A	10	2	16
Input-referred noise / bandwidth	1.13 μV_{rms} / (0.1-500 Hz)	1.6 μV_{rms} /	N/A	3.2 μV_{rms} / (10 Hz-7 kHz)	1.2 μV_{rms} / (25.4 Hz-25.6 kHz)	3.46 μV_{rms} / (1 Hz-50 kHz)
Channel gain / bandwidth	/ (0.01-500 Hz)	/ Up to 500 Hz	N/A	46 dB / (0.5 Hz-7 kHz)	27 dB / Up to 187.5 Hz	55-70 dB / (1-100) Hz -10 kHz
Electrical stimulation channels	64	128	4	N/A	1	8
Electrical stimulation current	10-1350 μA	20 μA -5 mA	22 μA -5 mA	N/A	0-510 μA	25-775 μA
Charge balancing	Yes	Yes	Yes	N/A	Yes	Yes
Optical stimulation channels	N/A	N/A	1	4	1	16
Optical stimulation current	N/A	N/A	22 μA -5 mA	0-35 mA	Up to 120 mA	0.8-24.8 mA
Light intensity	N/A	N/A	Up to 23 mW/mm ²	N/A	Up to 50 mW/mm ²	Up to 31.5 mW/mm ²
Power transmission	Inductive link	Battery	Ultrasound	Battery	Battery	Inductive link
Downlink data	ASK / Inductive link	BLE	ASK / Ultrasound link	Nordic TRx	OOK TRx	OOK-PPM / Inductive link
Uplink data	UWB	BLE	N/A	Nordic TRx	OOK TRx	OOK / 434 MHz RF

wireless power and data Rx's, and digital blocks, all in a 5×3 mm² silicon chip. The custom-designed SoCs presented in [14] and [19], on the other hand, still need to work with commercial MCU for data transmission.

In terms of the versatility of neural interfacing modalities, we have demonstrated one of the most comprehensive multifunctional SoC, offering users flexibility to execute sophisticated hybrid neuromodulation paradigms. In [25], although all three functions are presented, the optical stimulation circuits are not fully integrated on chip, the recording/stimulation channel counts are limited to two/one, respectively, and the power source is still a battery with limited lifetime.

For the *in vivo* results, the LFP-based comparisons suggest that the electrical and optical stimulation applied using our trimodal SoC can effectively evoke neural activities, and the artifact rejection circuit can adequately prevent the LFPs from being submerged by the stimulus artifacts. The successful observation of neuronal oscillation, known as synchronized activities across the local population of neurons [49], proved the recording functionality of our SoC. The immunohistochemical analysis results further validated the efficacy of the optical stimulation.

The *in vitro* experiment is a major step towards developing a wireless implantable trimodal neural interface device, compatible with the EnerCage-HC system, to support *in vivo* experiments on small freely behaving animals over extended periods. Currently, we are developing a smaller version of the implantable trimodal device in a way that it can be attached to or implanted in small animal models without causing any discomfort or interference with their behavior.

As shown in Fig. 14, in addition to the data Tx block, the power management block also has high power consumption. To reduce it, we will improve the voltage doubler and LDOs. We have previously demonstrated an adaptive active voltage doubler/rectifier, which can automatically switch between active voltage doubler and active rectifier modes depending on which mode provides high power conversion efficiency (PCE) [50]. Besides this, we intend to design a boost converter, which features higher PCE than the current LDO.

VIII. CONCLUSION

We have presented a trimodal wireless implantable neural recording and optical/electrical stimulation SoC with all the necessary blocks to support wireless operation of these key neural interfacing functions. The AFE offers low-noise performance while the artifact rejection circuit can effectively prevent the AFE from being saturated by stimulus artifacts. The SCS method implemented in the SoC is capable of generating large instantaneous current pulses to drive selected μ LEDs and generate light flashes that would surpass the optogenetic neuromodulation threshold. With both active and passive charge balancing, the SoC also ensures the safety of the biphasic electrical stimulation. The complete SoC functionality has been successfully verified both *in vitro* and *in vivo* on anesthetized rat model, while LFP signal and immunostained tissue analyses

demonstrate functionality of the three neural interfacing modalities.

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