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Robust power grid network design considering EM aging effects for multi-segment wires☆

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ABSTRACT

This paper presents a number of power grid network design and optimization techniques that consider the electromigration (EM) effects for multi-segment interconnect wires. First, we consider a new EM immortality constraint due to EM void saturation volume for multi-segment interconnects. It helps reduce conservativeness in the EM-aware on-chip power grid design. Along with the EM nucleation phase immortality constraint, we show that both EM immortality constraints can be naturally integrated into the existing programming based power grid optimization framework. Second, to mitigate the overly conservativeness of the immortality constrained optimization methods, we further explore three strategies: we first size up failed wires to meet one of the immortality conditions subject to the design rules; second, we consider the EM-induced aging effects on power supply networks for a target lifetime, which allows some short-lived wires to fail and optimizes the remaining wires; third, we propose a large change sensitivity-based optimization scheme to perform localized fixing based on recently proposed coupled EM-IR drop analysis method. Numerical results on a number of IBM-format power grid networks demonstrate that the new method can reduce more power grid area compared to the existing EM immortality constrained optimizations. Moreover, the new method is able to optimize power grids with nucleated wires, which would not be possible with the existing methods. Results also show the sensitivity-based localized power girds fixing can fix EM-induced IR drop violations in a few minutes for synthesized power grid networks from ARM core designs.

1. Introduction

Electromigration (EM) remains the top killer for the copper based interconnects in current and near-future advanced VLSI technologies. The International Roadmap for Devices and Systems (IRDS) [2] and the International Technology Roadmap for Semiconductors (ITRS) [3] predict that the allowable current density continues to decrease due to EM while the required current density to drive the gates continues to increase. As a result, the EM-related aging and reliability will become worse for current 7 nm and below technologies.

For practical VLSI chip, the on-chip power supply or power-ground (P/G) networks are most susceptible to EM failures due to large and unidirectional current densities [4–7]. The interconnect usually contains multiple segments, which is a multi-segment wire. As a result, designing robust power supply networks to satisfy the demanding design requirements remains a challenging task.

During the power grid synthesis in a typical design flow, an important step is to size the wire width of the power grid stripes after the topology of the power supply networks has been determined. The area of the power grids is optimized while electromigration and excessive IR drop constraints are met. There is a rich body of previously proposed work for the power supply network optimization, based on nonlinear or sequence of linear programming (SLP) methods [8–15]. To satisfy the EM reliability, most methods used the current density of individual wires as the constraint, which is mainly based on the highly conservative Black's EM model [4]. Furthermore, most of them failed to consider the multi-segment interconnects, which consists of continuously connected high-conductivity metal within one layer of metallization. Recent studies show that the hydrostatic stress in multi-segment interconnect wires (as shown in Fig. 1) are coupled and the EM failure conditions must be considered for the whole interconnect wire [16–25]. For instance, the parameter change of one wire segment may affect the EM

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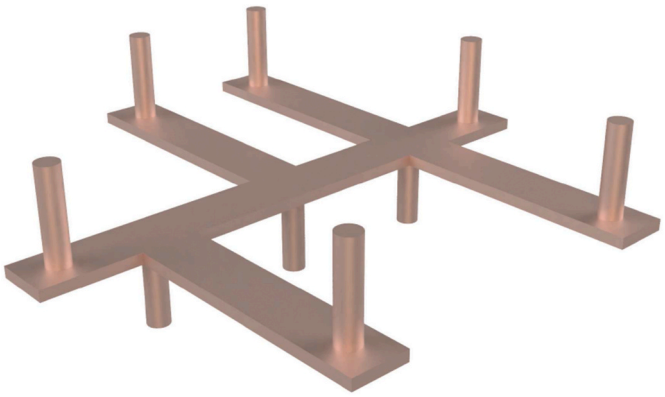

Fig. 1. Example of a multi-segment wire.

stress condition of another wire segment in the same interconnect tree, which provides more powerful potential to optimize a power grid subject to EM constraints for a multi-segment wire compared with the traditional current density based methods.

In [15,26], a power grid network sizing method considering the multi-segment interconnects has been proposed based on the multi-segment EM immortality check criteria [27]. It can automatically consider all the wire segments and their interactions in an interconnect tree. However, the proposed EM immortality constrained optimization can still be conservative as it requires all the wire segments in each tree to be immortal, i.e., void nucleation is not allowed.

For a multi-segment interconnect, once a void is formed in a segment, it will start to grow. However, the void growth will stop when the compressive stress in the remaining wires reaches steady state status in other words, the back force from the compressive stress is equivalent to the force for void growth. The void volume at this time is called *saturation volume*. If the saturation volume of a void is smaller than the so-called *critical volume* or *critical area* as shown in Fig. 2, then the wire will still be considered immortal. The *critical volume/area* is defined as the volume (or area in the two-dimensional case) that the void must meet or exceed to completely block the current flow in the copper interconnect and shunt it to the metal liner. Therefore, the conservative nature of the power grid optimization process can be relaxed if this saturation volume effect is considered, which will be a major focus of this work.

In this article, we propose a number of new power grid network sizing techniques based on the state-of-the-art EM models for multi-segment interconnects [22,25]. Our new contributions are as follows:

- First, we consider the recently proposed saturation volume estimation method for general multi-segment interconnect wires [28]. We demonstrate how the immortality constrained EM wire sizing problem can be reformulated considering the new EM saturation volume for general multi-segment interconnects. Then we show how the new constraints can be used in the existing sequence of linear programming based power grid optimization framework.
- We illustrate that many of the power grids that cannot be optimized using existing EM immortality constraints can be further optimized with the new EM immortality criteria while the resulting power grid networks with some failed interconnects can still be considered immortal. Furthermore, we consider two EM immortality constraints: *EM nucleation phase immortality* and *EM incubation phase immortality*, and we show that both EM immortality conditions and check criteria can be naturally integrated into the existing programming based power grid optimization framework, which remains the most efficient power grid optimization method.
- To mitigate the overly conservative nature of the optimization formulation, we first size up failed wires to meet one of the immorality conditions subject to the design rules so that the programming based optimization can be carried out.
- We further consider the EM-induced aging effects on power supply networks for a target lifetime, which allows some short lifetime wires to fail and optimizes the rest of the wires in the linear programming framework.
- Last but not least, we propose a large change sensitivity-based optimization scheme to perform localized power grids fixing based on recently proposed coupled EM-IR drop analysis method for power grid networks.

Numerical results on a number of IBM-format power grid networks demonstrate that the new method outperforms the existing immortality constrained optimizations. Furthermore, the new method can optimize the on-chip power grids with nucleated wires, which was considered EM mortal and cannot be optimized by the existing immortality constrained optimization methods or leading to more area reduction than the previous methods. Results also show the large change sensitivity-based localized power grid fixing can fix EM-induced IR drops in a few minutes for synthesized power grid networks of ARM core designs from Synopsys ICC tool suite.

This paper is organized as follows: Section 2 reviews the EM basics, the recently proposed EM saturation volume model and the corresponding immortality check method employed in this work. Section 3 presents the basics of our saturation volume based EM-aware P/G network optimization method. Section 4 introduces the new saturation volume based EM immortality and lifetime constrained P/G network sizing strategies for tree based multi-segment wires. Section 5 discusses the IR drop constrained power grids optimization methods. Experimental results on several P/G networks and the comparison with the voltage based EM constrained method are summarized in Section 6. Section 7 concludes this paper.

2. Review of EM physics and stress modeling

2.1. Steady-state EM-induced stress modeling

EM is the physical phenomenon of the migration of metal atoms along the direction of the applied electrical field. Atoms, either lattice atoms or defects/impurities, migrate along the trajectory of conducting electrons. Due to momentum exchange between atoms, hydrostatic stress is generated inside the embedded metal wire during the migration process. Before the hydrostatic stress reaches the critical level, the atomic flux flowing caused by electron flow from cathode to anode can still balance with the atomic flux caused by inhomogeneous distribution of hydrostatic stress. When the stress reaches the critical level, a void and a hillock caused by atom migration will be formed at the cathode end and anode end, respectively. However, if the hydrostatic stress cannot reach the critical level, the void will not be formed or nucleated.

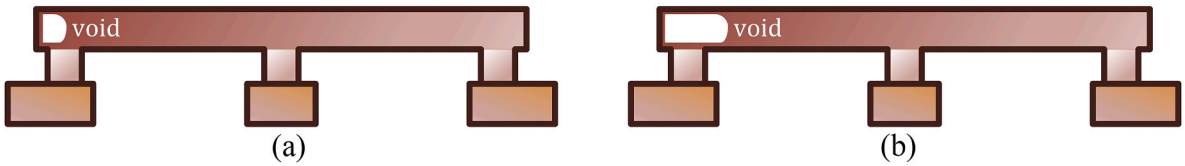

Fig. 2. (a) Void is smaller than the critical area. (b) Void is larger than the critical area.

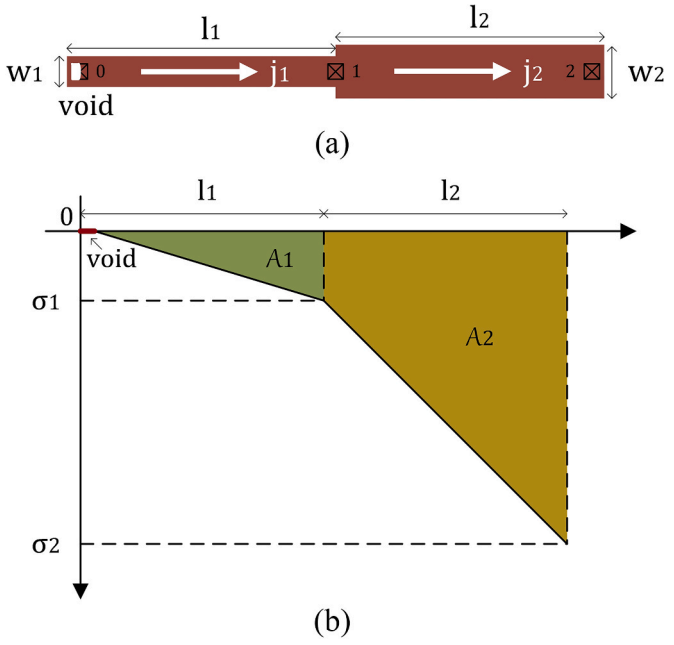

Fig. 3. (a) A two-segment wire and the direction indicates electron flow. (b) Stress integration area of a two-segment wire.

The case where a void cannot be formed is called EM nucleation phase immortal.

After a void is formed, it will keep growing until saturation. Void saturation happens when two kinds of flux balance with each other. One is the flux of atoms previously located in metal which is consumed by the growing void and the other is the back flux of atoms generated by a gradient of growing stress. If the void volume is smaller than the volume of the intersection which is recognized as critical volume $\mathcal{V}_{crit}$, current can still flow through the copper wire since the wire cross-section is not blocked by the void. Once the void size is large enough and occupies the wire cross-section, current has to go through the liner whose resistivity is much higher than copper and the resistance of the wire will increase, indicating that the wire enters growth phase. As can be seen, if the saturation volume is smaller than critical volume, the wire is still immortal even if a void is formed. This case is called EM incubation phase immortal.

A model predicting the saturation volume $\mathcal{V}_{sat}$ was proposed in Ref. [28]:

$$\begin{aligned}\mathcal{V}_{sat} &= \sum_i \mathcal{V}_{sat,i} = h \times \sum_i \mathcal{A}_{sat,i} \\ &= h \times \sum_i [(-2\sigma_{c,i} + \frac{j_i l_i \rho e Z}{\Omega}) \times \frac{l_i w_i}{2B}] \\ &= h \times \sum_i [(-2\sigma_{c,i} + \frac{V_i e Z}{\Omega}) \times \frac{l_i w_i}{2B}]\end{aligned} \tag{1}$$

where h is thickness of the wire and $\mathcal{V}_{sat,i}$, $\mathcal{A}_{sat,i}$, $\sigma_{c,i}$, j_i, l_i and w_i represent the contribution to void volume, contribution to void area, stress at the cathode, current density, length and width of the ith segment, respectively. For the segment in which a void has been nucleated, $\sigma_{c,i}$ is 0 on the cathode. Except for the segment with the void, the steady-state stress on cathode of the other segments are the same as the anode of the segment connected to them.

As shown in Eq. (1), voltage and width on each branch i contribute to the void volume, so the saturation void volume can be adjusted by modifying the voltage and width of the branches in order to make the wire incubation phase immortal.

Fig. 3 uses a two-segment wire to illustrate this method. Here, stress at node 1 and node 2 can be calculated as

$$\begin{aligned}\sigma_1 &= 0 - \frac{(\mathcal{V}_1 - 0)eZ}{\Omega} = -\frac{j_1 l_1 \rho e Z}{\Omega} \\ \sigma_2 &= -\sigma_1 - \frac{(\mathcal{V}_2 - \mathcal{V}_1)eZ}{\Omega} = -\frac{(j_1 l_1 + j_2 l_2)\rho e Z}{\Omega}\end{aligned} \tag{2}$$

Fig. 3(b) shows the stress at steady state versus branch length. $\mathcal{A}_1$ and $\mathcal{A}_2$ in the figure are the contribution of the two branches on void area, which indicate that the stress on both branches has contribution to the void formation.

In addition, critical volume $\mathcal{V}_{crit}$ is defined as

$$\mathcal{V}_{crit} = h \times w \times d \tag{3}$$

where h is thickness of the wire, w is the wire width and d is the via diameter. For wide wires, multiple vias may be applied, then d is equivalent to w. In this case, we can assume that $\mathcal{V}_{crit}$ is proportional to w^2.

In order to determine whether the wire is EM incubation phase immortal or not, the saturation volume is compared with the critical volume, more specifically, the wire is incubation phase immortal if

$$\mathcal{V}_{sat} < \mathcal{V}_{crit} \tag{4}$$

2.2. Full-chip EM-induced IR drop modeling

EM aging process typically leads to resistance increase or even open wire segments, it may further cause the increase of IR drops over time. However, for on-chip mesh-structured power grid networks, due to its inherent design redundancy, a few wire failures may not immediately result in significant IR drop increase. But as more wires nucleate, the IR drop will eventually lead to timing violations. As a result, the power grid networks become time-varying networks with time-varying IR drops due to the EM induced aging process [19,21]. On the other hand, the failed wire segments alter the current distributions of all the interconnect wires, which may further accelerate the failure process. Hence, one has to consider the interplay between the two physics: electrical characteristics and hydrostatic stress in the interconnect wires.

A number of full-chip EM analysis for power grid networks have been proposed recently [19,21,27,29]. These methods can predict the EM lifetime of the power grid and obtain failed trees. Specifically, Huang et al. [19,30] proposed the first physics based full-chip EM analysis method. However, only nucleation and growth phases are considered in this EM model, incubation phase is ignored. Chatterjee et al. [21,29] proposed finite difference method (FDM) based full-chip EM analysis tool to get better EM accuracy. Cook et al. [23] accelerated the FDM by applying Krylov subspace based reduction technique. However, these methods focus only on the EM stress without considering impacts from wire resistance changes. Recently, Sun et al. [24] proposed a full-chip EM-induced IR drop analysis, which considers dynamic interplay between the hydrostatic stress and electronic current/voltage in a power grid network. This method, called *EMspice*, solves the coupled time-varying partial differential equations in time domain and simulates the stress evolution in multi-segment interconnect trees.

After checking the wire immortality conditions for both nucleation and incubation phases, *EMspice* solves the stress and IR drop of interconnect wires in a coupled way. The coupled solver consists of a finite difference time domain (FDTD) solver for EM stress [21,23] and a linear network DC IR drop solver, which can be described as

$$\begin{aligned}\mathbf{C}\dot{\sigma}(t) &= \mathbf{A}\sigma(t) + \mathbf{P}I(t), \\ \mathcal{V}_v(t) &= \int_{\Omega_L} \frac{\sigma(t)}{B} d\mathcal{V}, \\ \mathbf{M}(t) \times u(t) &= \mathbf{P}I(t), \\ \boldsymbol{\sigma}(0) &= [\sigma_1(0), \sigma_2(0), \ldots, \sigma_n(0)] \ at \ t = 0\end{aligned} \tag{5}$$

where $\mathbf{M}(t)$ is the admittance matrix for the power grid network, which

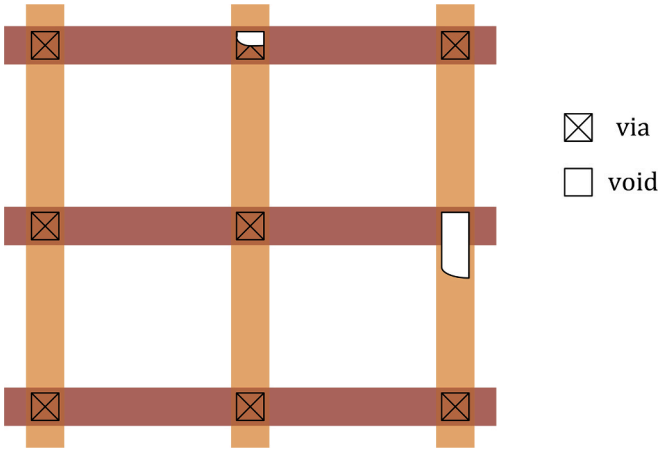

Fig. 4. Void formation of a power supply network.

is time-varying due to the fact that wire resistance changes with EM failure effects. **P** is a $b \times p$ input matrix, where p is the number of inputs, i.e., the size of current sources $I(t)$. $u(t)$ represents the nodal voltages of the network and $I(t)$ is the current sources from the function blocks of the chips. **C**, **A** are $n \times n$ matrices. And n is the number of nodes. Note that $\sigma(0)$ denotes the initial stress at $t = 0$. For each new simulation step, the stress from previous simulation step is used as the initial condition, iteratively.

The above equations in Eq. (5) are coupled and must be solved together. Linear network IR drop solver passes time-dependent current densities and P/G layout information to the FDTD EM solver. Once the voids are formed, IR drops in the power grid will change and the current at each time step will become different. The FDTD EM solver provides the IR drop solver with new resistance information, particularly, wires with voids. Since these two simulations are coupled together, wire current and resistance on each mortal wire are dependent on each other. As a consequence, it can tell the resulted IR drop and EM failure hotspots at the target lifetime.

3. New EM immortality constrained optimization for multi-segment interconnects

In this section, we propose a new EM immortality constrained power grid wire sizing method for multi-segment interconnect wires. Compared to recent work [15], the new EM constraint is less conservative and can optimize more hard-to optimize problems while ensuring all the wires are EM immortal. We first introduce the power grid models in our work, then present a few new EM immortality definitions, finally we formulate the new EM immortality constrained optimization problem.

3.1. Power gird models

In this optimization, the P/G network is composed of an orthogonal mesh of multi-segment wires. Only DC issues are considered, i.e., we focus on the resistance of the network. In addition, we do not size vias as it cannot be sized with most of the design rules. The void typically forms in the wire segment rather than the via unless it is due to initial thermomechanical stress from the fabrication process. Furthermore, the via resistance is quite small compared to the wire resistance, thus it is ignored in our model. To obtain the initial nodal voltages and branch currents of the P/G network, equation $G \times V = I$ must be solved first.

3.2. New EM immortality criteria

In general, the EM failure process is divided into nucleation phase, incubation phase and growth phase. In the nucleation phase, the stress at the cathode increases, when it reaches a critical level, a void will be nucleated. After the nucleation phase, the void starts to grow and eventually leads to wire failure after a period of time.

3.2.1. EM conditions for multi-segment wires

Fig. 4 shows the void formation in a power grid network. We consider the following three cases.

Case 1. In the left vertical wire, no void is formed, which means the stress at the cathode does not exceed the critical stress in the nucleation phase, thus the wire is EM immortal. We call it *EM nucleation phase immortal.*

Case 2. In the middle vertical wire, a void is nucleated, but it does not fully cover the via, EM failure process ends at the incubation phase in which no meaningful wire resistance is observed. Note that the via resistance may change due to void formation, but we do not take via resistance into consideration here. In conclusion, the void is saturated before reaching the critical volume and the wire is still considered EM immortal. We call it *EM incubation phase immortal.*

Case 3. In the right vertical wire, a void is nucleated at the cathode, after the incubation phase, it fully covers the via, initiating the true growth phase. In this phase, the resistance starts increasing as current starts to flow through the more resistive barriers of the copper wire. When it increases to the critical level , such as 10% or other defined thresholds, the wire can be considered to be failed. We deem this kind of wire *EM mortal.*

3.2.2. New EM immortality check

In [27], an EM immortality check criteria has been proposed for general multi-segment interconnects. This method, called voltage-based EM or *VBEM* method, in contrast to the traditional current density based method, formulated the new criteria in terms of nodal voltages. Specifically, this EM immortality condition of a multi-segment interconnect is described as

$$V_E < V_{crit,EM} \tag{6}$$

where *critical EM voltage* $V_{crit,EM}$ is defined by

$$V_{crit,EM} = \frac{1}{\beta}(\sigma_{crit} - \sigma_{init}) \tag{7}$$

where σ_{init} is the initial stress. V_E is the *EM voltage* which is proportional to stress at the ground node g and can be calculated as

$$V_E = \frac{1}{2A}\sum_{k \neq g} a_k V_k \tag{8}$$

where V_k is the normal nodal voltage with respect to the cathode node *cat* at node k and a_k is the total area of branches connected to node k. With voltage of node i (V_i), the steady-state stress at that node is calculated as $\sigma_i = \beta(V_E - V_i)$, where $\beta = \frac{eZ}{\Omega}$, e is elementary charge, Z is effective charge number and Ω is the atomic lattice volume.

However, this condition only checks void nucleation (Case 1). It fails to consider the case where a void is nucleated in a wire but the saturation void volume is less than the critical volume (Case 2).

Given a multi-segment wire m, the new EM immortality criteria first checks *VBEM*. If it passes, then the wire is immortal. Otherwise, we compute the saturation void volume $\mathcal{V}_{sat}$ from Eq. (1) and perform saturation volume check using Eq. (4). If Eq. (4) satisfies, the wire is still considered to be immortal. Otherwise, it is mortal, more complicated analysis of transient hydrostatic stress evolution is needed to evaluate the time to failure.

Note that EM nucleation phase immortal indicates that the stress will not reach the critical level. No void is formed does not mean that the saturation volume is zero, however, saturation volume makes sense only after a void is nucleated.

We remark that the EM models applied in our work are for general

cases, we will consider process variation with Monte Carlo method in the future.

3.3. Problem formulation

Let $G = \{N, B\}$ be a P/G network with n nodes $N = \{1, \ldots, n\}$ and b branches $B = \{1, \ldots, b\}$. Each branch i in B connects two nodes i_1 and i_2 with current flowing from i_1 to i_2. l_i and w_i are the length and width of branch i, respectively. ρ is the sheet resistivity. The resistance r_i of branch i is

$$r_i = \frac{V_{i_1} - V_{i_2}}{I_i} = \rho \frac{l_i}{w_i} \tag{9}$$

3.3.1. Objective function

We can express the total routing area of a power grid network in terms of nodal voltages, branch currents and branch lengths as follows

$$f(V, I) = \sum_{i \in B} l_i w_i = \sum_{i \in B} \frac{\rho I_i l_i^2}{V_{i1} - V_{i2}} \tag{10}$$

3.3.2. Constraints

The constraints that need to be satisfied for a reliable power grid network are shown as follows.

1. Tree-related constraints

   Equal width constraints. For typical chip layout designs, branches within an interconnect tree should have the same width, i.e., $w_i = w_k$.

   $$\frac{V_{i1} - V_{i2}}{l_i I_i} = \frac{V_{k1} - V_{k2}}{l_k I_k} \tag{11}$$

   Note that typically an interconnect tree is just a P/G stripe and equal width is a common assumption for general power grid networks.

   New EM immortality constraints for multi-segment interconnects. As described before, for a multi-segment interconnect m, we consider two EM immortality constraints: the EM nucleation immortal constraint (6) and EM incubation phase immortal constraint (4). We will select one of them based on the stress conditions.

   We remark that in constraints (6) and (4), both the *EM voltage* $V_{E,m}$ and the saturation volume $\mathcal{V}_{sat,m}$ are linear functions of the nodal voltages of the interconnect wires, supposing that each branch has the same width. As a result, the constraints are still linear in terms of nodal voltages, which is a requirement for the sequence of linear programming method.
2. Other constraints

   Voltage IR drop constraints. A threshold voltage is required to guarantee proper logic operation

   $$V_j > V_{min} \text{ for power network} \tag{12}$$

   Minimum width constraints. Usually different layers have different requirements for the width of the wire segments

   $$w_i = \rho \frac{l_i I_i}{V_{i1} - V_{i2}} \geq w_{i,min} \tag{13}$$

   Kirchoff's current law (KCL). For each node j, we have

   $$\sum_{k \in B(j)} I_k = 0 \tag{14}$$

   where $B(j)$ is the set of branches incident on node j.

3.4. Relaxed two-step sequence of linear programming solution

The power grids optimization aims to minimize objective function (10) subject to constraints (6), (4), (12)-(14). It will be referred as problem P. Problem P is a constrained nonlinear optimization problem.

Note that $V_{E,m}$, which is defined in Eq. (8), is a function of both nodal voltage and area of a wire. According to objective function (10), the area of a wire segment is a function of nodal voltages and branch current, therefore, $V_{E,m}$ is a nonlinear function. Take a three-segment wire similar to Fig. 3(a) as an example,

$$\begin{aligned} V_{E,m} = & \frac{a_1(V_0 - V_{cat,m}) + (a_1 + a_2)(V_1 - V_{cat,m})}{2(a_1 + a_2 + a_3)} \\ & + \frac{(a_2 + a_3)(V_2 - V_{cat,m}) + a_3(V_3 - V_{cat,m})}{2(a_1 + a_2 + a_3)} \\ = & \frac{l_1 w_1 V_0 + (l_1 w_1 + l_2 w_2) V_1 + (l_2 w_2 + l_3 w_3) V_2 + l_3 w_3 V_3}{2(l_1 w_1 + l_2 w_2 + l_3 w_3)} \\ & - V_{cat,m} \end{aligned} \tag{15}$$

where $V_{cat,m}$ is the cathode node voltage of the mth wire. If we have the equal width constraint (11), which indicates $w_1 = w_2 = w_3$, then the EM nucleation phase immortal constraint (6) actually becomes a linear function of nodal voltage again.

$$V_{E,m} = \frac{l_1 V_0 + (l_1 + l_2) V_1 + (l_2 + l_3) V_2 + l_3 V_3}{2(l_1 + l_2 + l_3)} - V_{cat,m} \tag{16}$$

For $\mathcal{V}_{sat,m}$, it is also nonlinear in terms of nodal voltages, assume V_0 is the cathode node voltage,

$$\begin{aligned} \mathcal{V}_{sat,m} = & h \times \left[\left(-2\sigma_0 + \frac{(V_1 - V_0) eZ}{\Omega} \right) \frac{l_1 w_1}{2B} + \left(-2\sigma_1 \right. \right. \\ & \left. \left. + \frac{(V_2 - V_1) eZ}{\Omega} \right) \frac{l_2 w_2}{2B} + \left(-2\sigma_2 + \frac{(V_3 - V_2) eZ}{\Omega} \right) \frac{l_3 w_3}{2B} \right] \\ = & h \times \frac{eZ}{2B\Omega} [(V_1 - V_0) l_1 w_1 + (V_1 + V_2 - 2V_0) l_2 w_2 \\ & + (V_2 + V_3 - 2V_0) l_3 w_3] \end{aligned} \tag{17}$$

However, considering $\mathcal{V}_{crit,m}$ is proportional to w^2, EM incubation phase immortality condition can be simplified as

$$\frac{eZ}{2B\Omega} [(V_1 - V_0) l_1 + (V_1 + V_2 - 2V_0) l_2 + (V_2 + V_3 - 2V_0) l_3] < w \tag{18}$$

With all these linear constraints, we can follow the relaxed two-phase iterative optimization process [10,12] and apply the sequence of linear programming technique [15] to solve the relaxed problem in each phase.

Note that the equal width constraint aims for the optimization flow only, the segments of an interconnect can have different width due to reservoir insertion [26]. Besides, sensitivity-based IR drop fix methods, which will be discussed in Section 5, can also lead to distinct segment width.

Specifically, we have a voltage solving phase when all branch currents are assumed to be fixed and a current solving phase when all nodal voltages are fixed. Because the objective function in the voltage solving phase is nonlinear, we take the first-order Taylor's expansion around the initial solution V^0 to get the linearized objective function

$$g(V) = \sum_{i \in B} \frac{2\rho I_i l_i^2}{V_{i1}^0 - V_{i2}^0} - \sum_{i \in B} \frac{\rho I_i l_i^2}{(V_{i1}^0 - V_{i2}^0)^2} (V_{i1} - V_{i2}) \tag{19}$$

Since I_i is a constant, an additional constraint is added [12].

$$\xi sign(I_i)(V_{i1}^0 - V_{i2}^0) \leq sign(I_i)(V_{i1} - V_{i2}) \tag{20}$$

where $\xi \in (0, 1)$ is a restriction factor, which will be selected by some trials and experiences and $sign(x)$ is the sign function.

4. Comprehensive power grid optimization strategies

In this section, we propose several EM constrained power grid

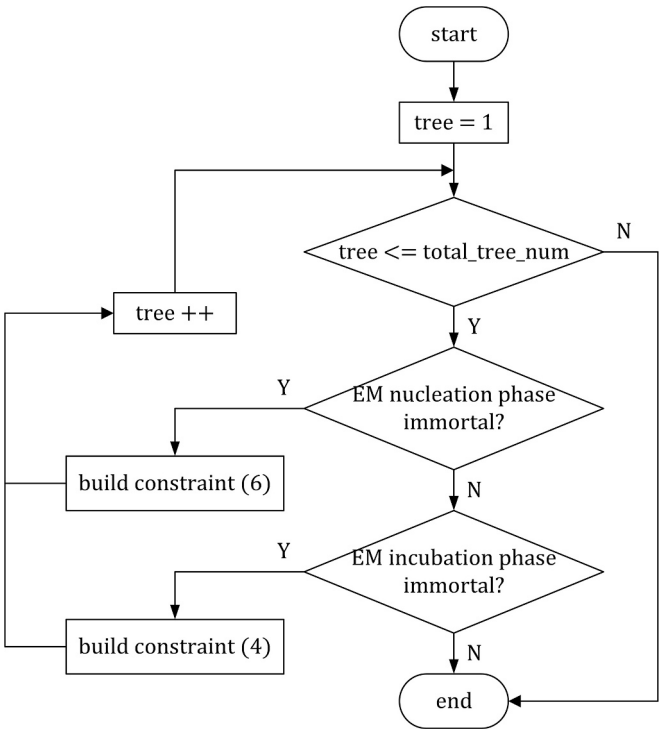

Fig. 5. Saturation volume based EM immortality check for a P/G network.

optimization strategies for multi-segment interconnect wires.

4.1. New EM immortality constrained P/G optimization

In the aforementioned optimization problem, the new EM immortality constrained P/G optimization starts with an initial feasible solution obtained from Section 3.1. Then we iteratively go through the voltage solving phase and current solving phase. The entire EM immortality constrained power grid network optimization procedure is summarized as Algorithm 1.

Algorithm 1
New EM immortality constrained P/G wire sizing algorithm

Input: Spice netlist G_I containing a P/G network.
Output: Optimized P/G network parameters.
1:/*Problem Setup*/
2: $k := 0$.
3: Compute the initial V^k, I^k from G_I.
4: **repeat**
5: /*P–V Phase*/
6: Perform new saturation volume based EM immortality check flow, construct equal width constraints (11) and EM nucleation phase immortal constraints (6) or EM incubation phase immortal constraints (4).
7: Construct minimum width constraints (13) and linear companion constraints (20) with I^k.
8: $m := 1$.
9: Compute $V_m^k := \arg\min g(V^k)$ subject to constraints (12), (13), (6), (4), (11), and (20) by sequence of linear programmings.
10: **while** $f(V_m^k) > f(V_{m-1}^k)$ **do**
11: Determine the search direction $d_m := V_{m-1}^k - V_m^k$.
12: Choose step size α for line search.
13: $V_{m+1}^k := V_m^k + \alpha d_m$.
14: $m := m + 1$.
15: **end while**
16: $V^{k+1} := V_m^k$.
17: /*P–I Phase*/
18: Construct equal width constraints (11) and minimum width constraints (13) with V^{k+1}.

(*continued on next column*)

Algorithm 1 (*continued*)

19: Compute $I^{k+1} := \arg\min f(I^k)$ subject to constraints (13), (11) and (14).
20: $k := k + 1$.
21: **until** $|f(V^k, I^k) - f(V^{k-1}, I^{k-1})| < \epsilon$

At the beginning of each voltage solving phase (line 6), we check the EM immortality for all the interconnect trees. If there exists a wire, which is neither EM nucleation phase immortal nor EM incubation phase immortal, we consider the power grid cannot be optimized. Otherwise, one EM constraint is built for each wire for later optimization. Note that the length and width of a certain branch used in each iteration may differ, thus the constant part of the EM constraints may change. The new saturation volume based EM immortality check flow is shown in Fig. 5.

4.2. New EM immortality constrained P/G optimization with pre-wire-sizing

EM immortality requirement for all the interconnects at the initial stage sometimes can be too strict. This happens when the initially designed power grids do not meet the EM requirement. As discussed earlier, we check the EM immortality conditions at the beginning of the voltage solving phase and consider the power grid network cannot be optimized if neither immortality condition is satisfied, which will greatly reduce the optimization space.

To mitigate this problem, we propose a pre-wire-sizing strategy, which can be seen as a preprocessing stage before the P/G optimization. In other words, in order to enable the optimization, we keep the original topology but adjust the resistance/width of power grid stripes.

When a wire fails the immortality criteria, one idea is to size the width up to make the wire immortal subject to the design rules. When we increase the width of the wire segments or the interconnect tree (for all of its segments), we will increase the critical void volume, which is increased quadratically with width w as defined in Eq. (3). As a result, the wire may become incubation phase immoral based on Eq. (4). Besides, width increase will also reduce the current density and branch voltages, therefore, it may make the wire nucleation phase immortal based on Eqs. (6) and (8). In our approach, we size up the failed wires so that one of the immortal conditions is met. The wire is sized by recomputing the branch voltages assuming that it will not affect other connected interconnect trees as a first order approximation until one of immortality conditions is met.

If the number of the wire segments need to be sized up is large, it indicates that the power grid network is not well designed in terms of EM in the first place and some structure change (e.g., adding more P/G strips) is probably needed first. Sizing up wire segments is trivial as long as design rules are allowed, which is an efficient way of preprocessing.

5. IR drop constrained power grid network optimization

For power grid network design, the ultimate design constraint is still the IR drop at the target lifetime (such as 10 years), which means that we can allow some EM failures in the power delivery networks as long as IR drop constraints are met. In this section, we present two strategies to optimize the power delivery networks to meet IR drop constraints with relaxed EM constraints.

5.1. EM lifetime constrained power grids optimization

Previous methods use EM immortal constraints to ensure that none of the interconnect trees fail. However, such constraints may be conservative because some wires can have EM failures as long as the power grid networks still work in the target lifetime and it fails to consider aging effect. Therefore, an EM aging-aware P/G wire sizing optimization method is applied in which some segments of interconnects will be allowed to fail or to increase resistance.

After performing EM immortality check, if neither of the EM constraints is met for a certain interconnect tree, then the lifetime of the wire will be computed based on the fast EM lifetime estimation method [31]. If the calculated lifetime is smaller than the target lifetime, the interconnect will be marked as failed and its EM constraint will not be considered any more. Furthermore, if void is formed in via-above interconnect, the via will be treated as disconnected, otherwise (via--below case), the increase in resistance of the segment will be computed [26].

On the other hand, if the calculated lifetime meets or exceeds the target lifetime, the saturation volume obtained from the previous optimization $\mathcal{V}_{sat,m,prev}$ for mth interconnect will become the new critical void saturation volume for next optimization iteration, i.e., Eq. (4) becomes

$$\mathcal{V}_{sat,m,prev} > \mathcal{V}_{sat,m} \tag{21}$$

The rationale behind this is that we relax the incubation phase immortality constraint as it still leads to satisfactory lifetime for this wire in previous optimization. By adding this constraint, we expect that its lifetime will not change too much and still achieve the given lifetime goal after the follow-up optimizations. After either *resistance change*, or *wire disconnection*, or *constraint relaxation*, a new round of SLP optimization is carried out until the optimized chip meets the EM lifetime target. Compared with [26], there will be more sizing space with the saturation volume based constraint and it will provide better optimization results.

5.2. Sensitivity-based localized power grids fixing

In this section, we present a large change sensitivity-based IR drop fixing method, which aims at enhancing EM reliability at late power grid network design stage, i.e., sign-off or electrical engineering order stages. As we know, both early failure and late failure contribute to the voltage change. When an early failure occurs, the interconnect is disconnected from another one, which can be seen as an open circuit. In contrast, the resistance of late failure trees increases gradually and finally stops when the voids reach the saturation volume. As a result, the wire resistance can experience large changes (from zero to infinity) during the target lifetime. Note that the definition of power grids lifetime is different from wire lifetime. It refers to the time at which an EM-induced voltage failure is expected to happen.

Algorithm 2 presents the large change sensitivity-based fixing algorithm as.

Algorithm 2
Large change sensitivity-based P/G fixing algorithm

Input: Spice netlist G_I containing a vulnerable power grid network.
Output: Robust power grid network spice netlist G_O.

1: Perform IR drop simulation and obtain $\mathbf{G}^k(t_0)$ and $\mathbf{v}^k(t_0)$ for the power grid network at initial time t_0.
2: Perform EM-IR co-simulation and obtain $\mathbf{G}^k(t_{\text{target}})$ and $\mathbf{v}^k(t_{\text{target}})$ at time point t_{target}.
3:**while** $\mathbf{v}^k(t_{\text{target}}) \le V_{\text{threshold}}$ **do**
4: Calculate the difference of m resistor widths $\Delta\mathbf{w}^k$ using Eq. (26) and determine the sensitivity matrix $\mathbf{S}^k_{n\times m}$.
5: Obtain the error vector $\boldsymbol{\varepsilon}^k$ based on the threshold voltage $V_{\text{threshold}}$ and $\mathbf{v}^k(t_{\text{target}})$.
6: Use gradient descent method Eq. (36) to update the width $\mathbf{w}^k(t_0)$ and widen the branch i with $w_i^{k+1}(t_0)$ which satisfies $w_i^{k+1}(t_0) > w_i^k(t_0)$.
7: **if** the updated branch width does not meet the design rules **then**
8: Set the branch width to the maximum allowable value and mark it as unadjustable.
9: **end if**
10: Perform IR drop simulation and obtain $\mathbf{G}^k(t_0)$ and $\mathbf{v}^k(t_0)$ for the power grid network at initial time t_0.
11: Perform EM-IR co-simulation and obtain $\mathbf{G}^k(t_{\text{target}})$ and $\mathbf{v}^k(t_{\text{target}})$ at time point t_{target}.
12: **end while**

If there exists mortal wire after performing EM immortality check, we deem the power grid network is a mortal one. For mortal power grids at design time, we first perform the IR drop simulation. The modified nodal analysis (MNA) equations for the P/G network at t_0 is represented as

$$\mathbf{G}(t_0)\mathbf{v}(t_0) = \mathbf{i} \tag{22}$$

where $\mathbf{G}$ is the admittance matrix of the network, $\mathbf{v} = [V_1, \ldots, V_n]^T$ is the vector of resulted node voltages and $\mathbf{i}$ is the attached current sources. The conductance of branch i is

$$g_i = \frac{w_i}{\rho l_i} \tag{23}$$

Therefore, the elements of $\mathbf{G}$ can be expressed as

$$G_{ij} = \begin{cases} -\sum_{k=1}^{N} g_k, & i = j \text{ and } (k_1 = i \text{ or } k_2 = i) \\ g_k, & i \neq j \text{ and } (k_1 = j \text{ or } k_2 = j) \\ 0, & i \neq j \text{ and } k_1 \neq j \text{ and } k_2 \neq j \end{cases} \tag{24}$$

Second, the coupled EM-IR drop analysis for the power supply network is performed through *EMspice* [24,32]. The new MNA equations at the target lifetime t_{target} can be expressed as

$$\mathbf{G}(t_{\text{target}})\mathbf{v}(t_{\text{target}}) = \mathbf{i} \tag{25}$$

Assume that m resistor (g_1, g_2, …, g_m) values would change due to void formed at the cathode. Then the difference of the corresponding effective width $\Delta\mathbf{w} = [\Delta w_1, \Delta w_2, \ldots, \Delta w_m]^T$ between t_0 and t_{target} time points are given by

$$\Delta w_i = \Delta g_i \rho l_i = [g_i(t_{\text{target}}) - g_i(t_0)]\rho l_i \tag{26}$$

Finally, we only change the i-th width with increment Δw_i at one time to calculate the voltage increments $\Delta\mathbf{v} = [\Delta v_1, \Delta v_2, \ldots, \Delta v_n]$ compared to the original network. When changing the i-th resistor, the $\mathbf{G}(t_0)$ matrix is modified by adding the perturbation matrix $\Delta g_i \mathbf{p}_i \mathbf{q}_i^T$, which is expressed as

$$\mathbf{G}\mathbf{v} = \left(\mathbf{G}(t_0) + \Delta g_i \mathbf{p}_i \mathbf{q}_i^T\right)\left(\mathbf{v}(t_0) + \Delta\mathbf{v}\right) = \mathbf{i} \tag{27}$$

where $\mathbf{p}_i$ and $\mathbf{q}_i$ are $n \times 1$ vectors. Their elements are given by

$$[\mathbf{p}_i]_k = \begin{cases} 1, k = i_1 \quad -1, k = i_2 \\ 0, \text{otherwise} \end{cases} \quad [\mathbf{q}_i]_k = \begin{cases} -1, k = i_1 \\ 1, k = i_2 \\ 0, \text{otherwise} \end{cases} \tag{28}$$

Based on Eq. (27), the increments of voltage can be determined by

$$\Delta\mathbf{v} = -(\mathbf{G}(t_0) + \Delta g_i \mathbf{p}_i \mathbf{q}_i^T)^{-1} \Delta g_i \mathbf{p}_i \mathbf{q}_i^T \mathbf{v}(t_0) \tag{29}$$

This equation involves the inverse of an $n \times n$ matrix and can be rewritten as [33].

$$\Delta\mathbf{v} = -\mathbf{G}(t_0)^{-1}\mathbf{p}_i(\Delta g_i^{-1} + \mathbf{q}_i^T \mathbf{G}(t_0)^{-1}\mathbf{p}_i)^{-1}\mathbf{q}_i^T\mathbf{v}(t_0) \tag{30}$$

Therefore, we only need to calculate the inverse of $\mathbf{G}(t_0)$ once to obtain the sensitivity $[\frac{\Delta v_1}{\Delta w_i}, \frac{\Delta v_2}{\Delta w_i}, \ldots, \frac{\Delta v_n}{\Delta w_i}]^T$. By repeating above procedure m times, we can compute the sensitivity matrix $\mathbf{S}_{n\times m}$ as

$$\mathbf{S}_{n\times m} = \begin{bmatrix} \frac{\Delta v_1}{\Delta w_1} & \frac{\Delta v_1}{\Delta w_2} & \cdots & \frac{\Delta v_1}{\Delta w_m} \\ \frac{\Delta v_2}{\Delta w_1} & \frac{\Delta v_2}{\Delta w_2} & \cdots & \frac{\Delta v_2}{\Delta w_m} \\ \vdots & \vdots & \ddots & \vdots \\ \frac{\Delta v_n}{\Delta w_1} & \frac{\Delta v_n}{\Delta w_2} & \cdots & \frac{\Delta v_n}{\Delta w_m} \end{bmatrix} \tag{31}$$

Therefore, the relationship between $\Delta\mathbf{v}$ and $\Delta\mathbf{w}$ can be described by

Table 1
Parameters used in the optimization process.

Parameters	Value	Parameters	Value
σ_{crit}	500 MPa	Ω	1.182×10^{-29}m^3
V_{crit}	3.69×10^{-3}V	E_a	0.8eV
T	323 K	D_0	5.55×10^{-8} m^2/s
B	140 GPa	ρ_{Cu}	$1.9 \times 10^{-8}\Omega \cdot$m
Z	10	ρ_{Ta}	$1.35 \times 10^{-7}\Omega \cdot$m

$$\Delta \mathbf{v} = \mathbf{S} \times \Delta \mathbf{w} \tag{32}$$

To solve for $\Delta \mathbf{w}$, we have

$$\begin{aligned} \mathbf{S}^T \Delta \mathbf{v} &= \mathbf{S}^T \mathbf{S} \times \Delta \mathbf{w} \\ \Delta \mathbf{w} &= (\mathbf{S}^T \mathbf{S})^{-1} \mathbf{S}^T \Delta \mathbf{v} \end{aligned} \tag{33}$$

Similar to constraint (12), to meet the operating requirements of the VLSI circuit, the voltages at all nodes should be no less than the threshold voltage $V_{\text{threshold}}$ within certain lifetime. Therefore, our destination is to minimize the error vector

$$\boldsymbol{\varepsilon} = [\varepsilon_1, \varepsilon_2, \ldots, \varepsilon_n]^T \tag{34}$$

where

$$\varepsilon_i = \begin{cases} 0, & V_i(t_{\text{target}}) \geq V_{\text{threshold}} \\ V_{\text{threshold}} - V_i(t_{\text{target}}), & V_i(t_{\text{target}}) < V_{\text{threshold}} \end{cases} \tag{35}$$

Then we can optimize the problem using gradient descent method

$$\mathbf{w}^{k+1}(t_0) = \mathbf{w}^k(t_0) + \alpha(\mathbf{S}^T \mathbf{S})^{-1} \mathbf{S}^T \boldsymbol{\varepsilon} \tag{36}$$

where α is the step size and can be selected by some trials. Note that the required width $\mathbf{w}$ to be changed may be also subject to the design rules as there is a upper bound for the widths.

6. Experimental results and discussion

6.1. Experiment setup

The proposed EM-aware constrained power grid optimization is implemented in C/C++. IBM power grid benchmarks [34] are used to test our work, and we also have a few synthesized IBM-format power grid networks so that different kinds of EM immortality constraints can be tested and verified. Node location and layer information are provided, therefore, the geometric structure of a certain benchmark is known. Current source, voltage source and resistance values can also be obtained easily. Since there is no wire length and width information, we made reasonable assumptions on wire length and layer height for the experiments. The maximum allowable IR drop is assumed to be 10% V_{dd} and the minimum allowable width is 0.1 μm. Some important parameters used in our experiments are listed in Table 1.

6.2. EM immortality constrained power supply optimization results

Table 2 compares the results of the new optimization method considering saturation volume with the results of the existing P/G optimization method checking EM nucleation phase immortality only [15].

In the optimization process, we assume that all the branches have the same width in one tree but different trees can have different widths. For fair comparison, we only allow the difference in the EM constraints. In Table 2, column 1 to 5 list the P/G network benchmarks (*circuit*), the number of interconnect trees (# tree), the number of nucleated wires at the beginning (# nuc-wires (b)), the number of nucleated wires at the end (# nuc-wires (e)), and the original area (*area (mm^2)*). Column 6 and 7 report the reduced chip area ratio (*area reduced (%)*) with respect to the original area for the two methods with EM nucleation phase immortal only constraint (*w/o saturation volume*) and the new EM immortality criteria (*with saturation volume*) respectively. Note that for the two methods, all the wires are EM immortal after optimization.

Table 2
Results of EM immortality and lifetime constrained P/G optimization considering void saturation volume.

circuit	# tree	# nuc-wires (b)	# nuc-wires (e)	area (mm^2)	w/o saturation volume [15]	with saturation volume
					area reduced (%)	area reduced (%)
ibmpg2	462	0	0	60.38	77.55	77.55
PG1	128	0	0	40.21	34.34	34.34
PG2	38	0	9	0.50	28.78	38.33
PG3	9	1	3	0.031	can't finish (with mortal wires (II))	53.26
PG4	12	1	1	0.030	can't finish (with mortal wires)	25.21
PG5	20	10	10	0.017	can't finish (with mortal wires)	14.84
PG6	20	2	2	0.23	27.39	28.41
PG7	80	11	11	1.28	26.68	29.76

As we can see, for *ibmpg2* example, which has 462 immortal trees at the beginning, the original area is 60.38 mm^2. After 2 iterations, the area can have 77.55% reduction without any EM violation. For *PG2*, all the wires are EM nucleation phase immortal at first, after 2 iterations, although it has 9 nucleated wires, all of them are EM incubation phase immortal. Compared with the previous work [15] which has about 28.78% reduction, the new method has better performance in terms of area reduction, while still ensuring EM immortality. Previous work cannot size *PG3* because it has nucleated wires in the beginning. Since the nucleated wires can still pass the saturation volume check (it is incubation immortal (II)), the P/G network can be sized properly with the new method. Note that the area improvement strongly depends on the original layouts, thus the absolute values of reduced area are not that important.

We further observe that the new method typically leads to more area reduction compared to the previous method. The reason is that the new EM immortality criteria is less conservative and thus it effectively allows the *EM voltage* to exceed the *critical EM voltage* by using the *EM incubation phase immortal* constraint. In other words, larger current density which can nucleate a void is allowed in the new method while ensuring wire resistance is not affected. As a result, we can conclude that the new method successfully enables the optimization of power grids, which would have been impossible in the previous method due to the conservative immortality constraint, in addition to leading to further area reduction in power grids compared to the previous method.

6.3. EM immortality constrained power supply optimization results with pre-wire-sizing

The result of the EM immortality constrained power supply optimization with sizing up are also shown in Table 2. There exist some benchmarks which do not satisfy the EM requirement in the initial situation, in this way, we check if the interconnects can be sized up to become incubation phase immortal. In *PG4* example, we find that there is one nucleated wire which fails both immortality constraints in the beginning. As discussed in subsection 4.2, after width adjustment, it becomes incubation phase immortal. For *PG5*, half of the interconnects are mortal at first, and they all become nucleation phase immortal after pre-wire-sizing. In this way, the optimization process can finish successfully.

Table 3
Results of sensitivity-based localized fixing.

circuit	# tree	# mortal wires (b)	# violations at t_{target}	# mortal wires (e)	# modified branches	area increased (%)	total time (s)
ARM-PG1	64	3	11	3	2	0.0438	150.27
ARM-PG2	64	5	32	5	3	0.0352	171.65
ARM-PG3	64	4	87	4	2	0.0614	377.18
ARM-PG4	128	7	21	6	4	0.0348	522.83

6.4. EM lifetime constrained power supply optimization results

PG6 and *PG7* in Table 2 demonstrated the lifetime constrained optimization case. In *PG6* example, the lifetime of the nucleated wires are longer than 100 years, thus the difference between the previous method and the new method is the relaxed constraint. In *PG7* example, before optimization, the shortest lifetime among the 11 nucleated wires is 5.53 years, which violates the lifetime constraint. After the optimization, the lifetime was improved to 17.02 years. As we can see from this example, lifetime can be extended while area can still be saved. The reason is that the open circuit or resistance change of the short-lived wires will be compensated by properly sizing the other wires to meet the lifetime requirement due to redundant structure design of P/G networks. It may lead to wider width, but the overall area of all the wires can be reduced. This further demonstrates the superior advantage of the lifetime constrained method over the immortality constrained method. For the cases with very long lifetime wires, even though they may have a few nucleated wires, after optimization, this is still the case. Besides, compared with previous method, the void saturation volume based method can lead to more area reduction.

6.5. Sensitivity-based localized power grids fixing results

The sensitivity-based localized power grids fixing results are demonstrated in Table 3. The PG designs for this subsection come from the power grids of the Cortex-M0 DesignStart processor, which is a 32-bit processor that implements the ARMv6-M architecture. The processor is synthesized using Synopsys Design Compiler and we simply modified some of the interconnects for our experiments.

We assume that the widths of the original power grids have already been set to their minimums and thus cannot be reduced. Column 1 to 4 list the P/G network benchmarks (*circuit*), the number of interconnect trees (# tree), the number of mortal wires at the beginning (# mortal wires (b)), and the number of IR drop violations at the target lifetime (# violations at t_{target}). Column 5 to 8 report the number of mortal wires at the end (# mortal wires (e)), the number of modified branches (# modified branches), the increased chip area ratio (*area increased (%)*) with respect to the original area, and the total simulation time (*total time (s)*).

With the localized fixing method, we are able to meet the power grid lifetime by only widening a few branches. In *ARM-PG1* example, the lifetime of the whole power grids is 8 years and the maximum voltage at t_{target} is $10.022\%V_{dd}$. There are 3 mortal wires and all of them have lifetime less than 10 years, in other words, there are 3 branch resistance changes at t_{target}. Note that the lifetime definitions of wire and power grid network are different. After performing the sensitivity analysis, we get the information that one of the wires need to modify. The power grid meets the lifetime target with only one iteration. The largest resistance change does not mean it contributes the most to voltage violations. For *ARM-PG3* who have 87 violations, the largest resistance change occurs at tree 33. However, according to Eq. (33) tree 1 and 31 should be modified, and tree 1 has the smallest resistance among the 4 mortal wires. In addition, *ARM-PG4* illustrates that the number of mortal wires can be reduced after the fixing process, where the mortal wires is one less at the end than at the beginning. The total fixing time mainly depends on the iteration number and the simulation time from initial to 10 years to get the EM-induced IR drop.

The sensitivity-based localized power grid fixing method is better performed at the later design stages, we suppose that the power grid is well designed and meets the IR drop requirement in the start. Usually, the grid can be easily fixed with 7 years or above lifetime. If the lifetime is too short, then there will be much more violations at 10 years, and may be difficult to fix with widening only a small set of branches. In this case, the interconnect widening method will be applied first.

7. Conclusion

In this paper, we presented a number of power grid network design and optimization techniques to consider the electromigration effects for multi-segment interconnect wires. First, we considered a new EM immortality constraint due to EM void saturation volume for multi-segment interconnects, which will reduce conservativeness in the EM-aware on-chip power grid design. We showed that the new EM immortality constraint can be integrated into the existing programming based power grid optimization framework. Second, to further mitigate the excessive conservativeness of the immortality constrained optimization methods, we explored three strategies: we first sized up failed wires to meet one of the $^{\text{immorality}}$ conditions subject to the design rules; second, we considered the EM-induced aging effects on power supply networks for a target lifetime, which allows some short-lived wires to fail and optimizes the rest of the wires; third, we proposed a large change sensitivity-based optimization scheme to perform localized fixing based on recently proposed coupled EM-IR drop analysis method for power grid networks. Numerical results on a number of IBM-format power grid networks demonstrated that the new method can reduce more power grid area compared to the existing EM immortality constrained optimizations. Furthermore, the new method is able to optimize power grids with nucleated wires for the first time. Results also showed the sensitivity-based localized power girds fixing can fix EM-induced IR drop violations in a few minutes for synthesized power grid networks from ARM core designs.

CRediT authorship contribution statement

Han Zhou: Conceptualization, Methodology, Software, Formal analysis, Investigation, Writing - original draft. **Liang Chen:** Methodology, Validation, Formal analysis, Investigation, Writing - review & editing. **Sheldon X.-D. Tan:** Conceptualization, Methodology, Formal analysis, Writing - review & editing, Supervision, Funding acquisition.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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