EMI-Regulated GaN-Based Switching Power Converter With Markov Continuous Random Spread-Spectrum Modulation and One-Cycle ON-Time Rebalancing

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***Abstract*— To meet stringent electromagnetic interference (EMI) requirements in modern integrated systems, this article presents a gallium nitride (GaN)-based switching power converter operating at 8.3 MHz. It employs a Markov continuous random spread-spectrum modulation (RSSM) technique to spread EMI spectra almost uniformly, and thus attenuate EMI level effectively. On the other hand, a one-cycle ON-time rebalancing scheme is designed to stabilize the duty-ratio of the converter even if the switching frequency changes randomly, suppressing the output voltage jittering without influencing the EMI reduction by RSSM. A prototype was designed and fabricated using a 0.18-μm HV CMOS process. With ±10% modulation range of a nominal switching frequency of 8.3 MHz, peak EMI is reduced from 66 to 35 dBμV at the fundamental frequency and from 62 to 27 dBμV at the third-order harmonic. In the meantime, the RSSM-induced output voltage jittering is suppressed from 240 to below 10 mV. The converter achieves above 60% efficiency over 96.6% of 7.5-W full power range, with a peak efficiency of 86.8% at 6.25 W.**

***Index Terms*— Electromagnetic interference (EMI) regulation, gallium nitride (GaN) power converter, Markov continuous random spread-spectrum modulation (RSSM), one-cycle ON-time rebalancing.**

I. Introduction

GALLIUM nitride (GaN) power devices, owing to their superior figure of merits, have gained fast-growing popularity in high-performance power electronics. With an equivalent dynamic ON-resistance R_{DSON}, a GaN high-electron-mobility transistor (HEMT) requires much less gate charge to switch. This attribute offers valuable potentials for GaN-based switching power converters to operate at much higher switching frequency than conventional silicon counterparts while retaining comparable if not better efficiency [1], [2]. High switching frequency operation facilitates fast transient performance and allows for the use of smaller power inductors and capacitors, leading to significant benefits on power density, cost, and system volume [3]–[7]. However, as a tradeoff, circuit operation at high switching frequency demands much shorter switching transition periods. This causes drastic increases on the slew rates of switching voltages and currents, which contribute directly to electromagnetic interference (EMI) generation [8]–[11]. As the EMI level elevates in interested frequency bands, circuit reliability for both signal and power processing deteriorates substantially. To regulate the EMI emission and avoid safety problems, EMI standards such as CISPR Compliance One specify stringent limits on the maximum allowed EMI levels [12]. Any single frequency violating such limits would fail the compliance tests. Hence, the EMI issue has become a tremendous hindrance in developing high-frequency GaN-based power circuits.

To regulate EMI noise in interested frequency bands effectively, spread-spectrum modulation (SSM) techniques have been reported [13]–[18]. If a switching circuit operates at a fixed frequency, the switching noise concentrates at the fundamental frequency and its harmonics. For reducing the peak EMI, the SSM techniques redistribute the energy at the switching frequency and its harmonics into a broader frequency range through frequency modulation. According to Carson's rule [19], the total energy before and after such a frequency modulation remains unchanged. This lays the foundation to remove or attenuate EMI from the critical frequency bands. In [13] and [14], periodic SSM (PSSM) techniques were developed. As shown in Fig. 1(a), a circuit's switching frequency f_{SW} varies following a periodic pattern, such as a triangular, a sinusoidal, or an exponential function. The quality of such a PSSM can be measured by its modulation index m_f, which is defined as follows:

$$m_f = \Delta f / f_m, \tag{1}$$

where Δf represents the switching frequency spread range and f_m is the modulation frequency. Theoretically, the EMI level decreases as m_f increases, which can be achieved by either reducing f_m, or increasing Δf, or both. However,

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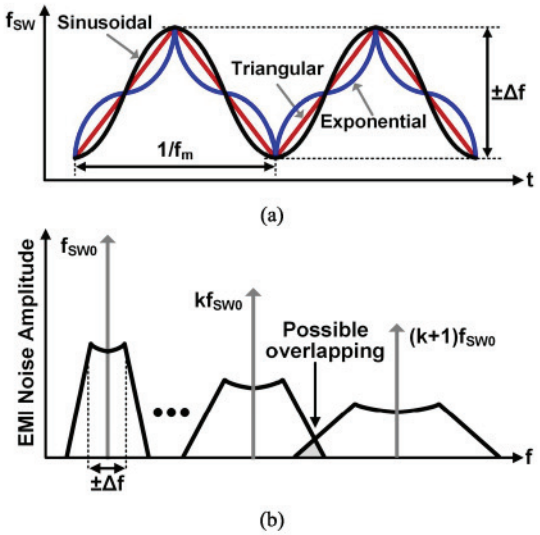

Fig. 1. Illustration of PSSM techniques in (a) time domain and (b) frequency domain.

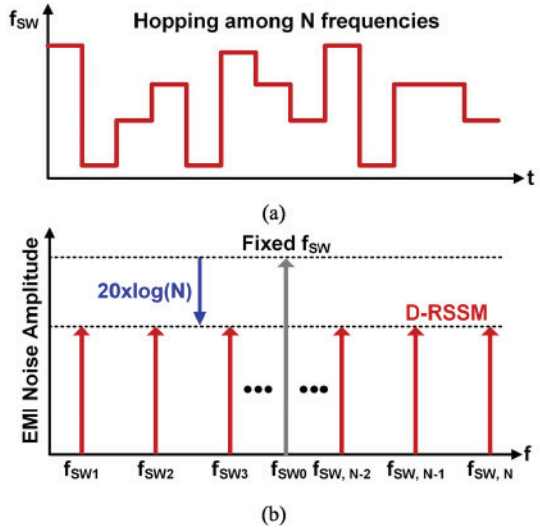

Fig. 2. Illustration of a D-RSSM technique with a finite hopping frequency of N in (a) time domain and (b) frequency domain.

in practice, a few constraints exist. First, f_m should be selected higher than the resolution bandwidth (RBW) of measurement instruments to meet the requirement of the peak detector value reading in EMI standards [20], [21]. Second, it should also be higher than 20 kHz to avoid audible noise. Third, Δf is confined by a switching power circuit itself when considering its loop stability. At last, extending Δf may cause overlaps across lower harmonics, as illustrated in Fig. 1(b), causing countereffects on the PSSM. Hence, historically, the effectiveness of the PSSM techniques are limited.

Random SSM (RSSM) techniques can be utilized to overcome the drawbacks of the PSSM techniques. With an RSSM, the switching frequency of a circuit is modulated randomly, and the EMI noise can thus be distributed almost uniformly within the modulated frequency range, leading to much lower EMI than in PSSM techniques [13]. The most straightforward way to randomize the switching frequency is to employ a random clock generator. Usually, such a clock generator is implemented digitally [15], [16]. The corresponding RSSM is thus a discrete RSSM (D-RSSM). With a clock generator that covers N discrete achievable modulation frequencies, the circuit hops randomly from f_{SW1} to f_{SWN}, as shown in Fig. 2(a). Theoretically, in this situation, the EMI reduction can be calculated as follows:

$$\Delta_{\mathrm{EMI}} = 20 \times \log N(\mathrm{dB}). \tag{2}$$

To achieve a large EMI reduction, a large N is highly desirable. However, as N increases, circuit complexity, chip area, and power consumption rise substantially. To overcome this, a thermal noise random clock generator was reported [17]. The technique provides continuous RSSM (C-RSSM) using an analog thermal noise generator circuit to modulate the switching frequency. It successfully achieves almost uniform noise distribution without the use of a large scale of digital blocks. Unfortunately, thermal noise is very sensitive to temperature and is difficult to control. In practice, it requires dedicated

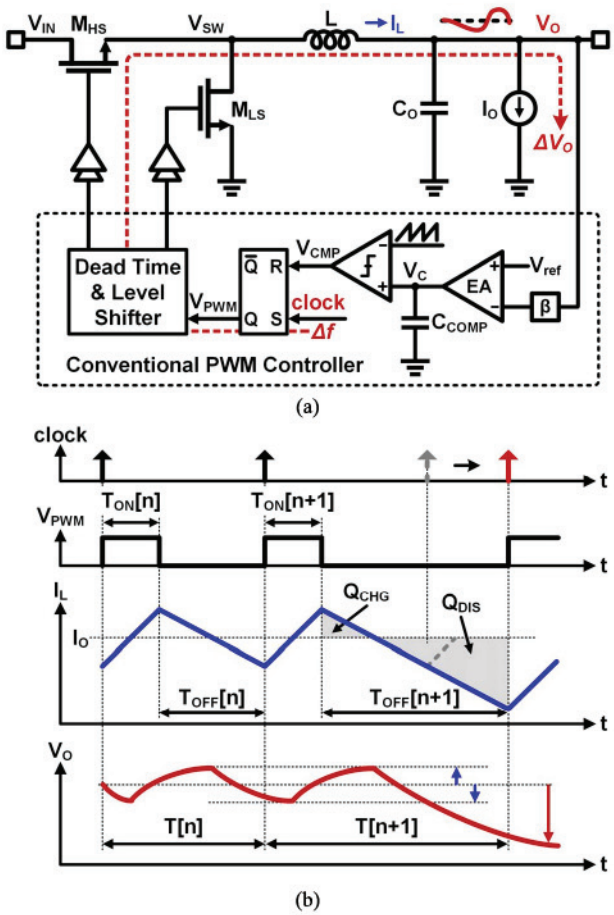

Fig. 3. (a) Schematic of a PWM buck converter with (b) illustration of V_O jittering effect induced by an RSSM.

design effort and hardware to confine the range of randomization, which counters the initial purpose of the RSSM.

On the other hand, although the RSSM techniques reduce EMI level effectively, they deteriorate the quality of voltage regulation [15], [16]. Use a classic pulsewidth modulation (PWM) buck switching converter in Fig. 3(a) as an example.

Due to the RSSM technique, the switching period varies from $T[n]$ to $T[n+1]$ randomly on a cycle-by-cycle basis. Here, n and $n+1$ represent the nth and the $(n+1)$th switching cycle, respectively. For stability and noise concerns, the loop gain bandwidth of the converter is usually designed lower than the switching frequency. Hence, the random T change cannot be immediately detected by the feedback controller. As a result, when the switching cycle alters from $T[n]$ to $T[n+1]$ randomly, $T_{\text{ON}}[n+1]$ remains unchanged from $T_{\text{ON}}[n]$. The inductor L is thus charged for the same period of time. However, as $T[n+1]$ is extended from $T[n]$ due to the RSSM [Fig. 3(b)], the inductor L is discharged for a longer period of time. Consequently, extra charge is withdrawn by the load, causing the output voltage V_O of the converter to drop from the nominal value. On the other hand, if $T[n+1]$ decreases from $T[n]$, the discharge time will be reduced, causing V_O to increase. Because the switching period under an RSSM varies continuously on a random pattern, the corresponding V_O jitters randomly around the nominal V_O value. This degrades the voltage regulation performance significantly. Increasing the output capacitor C_O can alleviate the issue. However, this would further reduce the loop gain bandwidth, making the transient response of the converter sluggish. On the other hand, this also increases PCB area and cost, contradicting the purpose of high-frequency GaN-based power converters addressed earlier. Alternatively, a ramp compensation scheme was reported to reduce similar V_O jittering [18], but the improvement is very limited, and the scheme only works for voltage mode power converters.

In addressing the aforementioned issues, this paper proposes a Markov C-RSSM technique to spread the EMI spectrum continuously in an almost uniform spectra distribution. For facilitating the C-RSSM, a Markov-chain-based random clock generator is proposed to modulate the switching frequency in an analog way. With an infinite number of random switching frequencies, it achieves better spread-spectrum than its digital counterpart. The proposed Markov C-RSSM is then applied to a GaN-based dc–dc buck converter, reducing the peak EMI effectively without elevating the noise floor significantly. In the meantime, a one-cycle ON-time (T_{ON}) rebalancing scheme is designed to stabilize the duty-ratio cycle-by-cycle even though the switching frequency is modulated randomly, removing the RSSM-induced V_O jittering effect. The remainder of this paper is organized as follows. Section II introduces the proposed Markov C-RSSM technique. The operation principle and circuit implementation of the one-cycle ON-time rebalancing scheme are elaborated in Section III. Then the implemented system is explained in Section IV, followed by the experimental results in Section V. Finally, this paper is summarized in Section VI.

II. Markov Continuous RSSM

A. Mathematical Principle

As addressed in Section I, the C-RSSM is highly desirable to overcome the finite frequency resolution issue encountered in D-RSSMs. The challenge here is the design of an effective analog random clock generator. For mitigating the issue, a Markov-chain-based random clock generator is designed on the ground of a chaotic piecewise-linear 1-D (PL1D) map [22] described as follows:

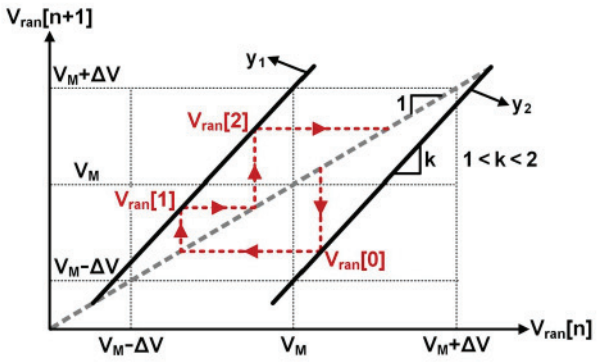

Fig. 4. PL1D map of the Markov random voltage source.

$$V_{\text{ran}}[n+1] = \begin{cases} kV_{\text{ran}}[n] + [(1-k)V_M + \Delta V], & V_{\text{ran}}[n] < V_M \\ kV_{\text{ran}}[n] + [(1-k)V_M - \Delta V], & V_{\text{ran}}[n] \geq V_M. \end{cases} \tag{3}$$

Here, V_{ran} is the random output, V_M and ΔV represent the center reference and the variation range, respectively and k is the common slope of the two lines. This chaotic map is illustrated further in Fig. 4. In addition to defining the nominal level, V_M also divides the state space into two regions, which is known as Markov partition. The ΔV defines the randomization boundary. The value of k determines the stochastic property of the system. On the one hand, to avoid the convergence issue, k should be selected among the range from 1 to 2 [22]. This ensures that the random sequence of V_{ran} is attracted to $[V_M - \Delta V,\ V_M + \Delta V]$. On the other hand, to acquire an almost uniformly distributed V_{ran}, k should be close to 2. As shown in the waveforms, after initiating an arbitrary state $V_{\text{ran}}[0]$ among the range of $[V_M - \Delta V,\ V_M + \Delta V]$, a random sequence $\{V_{\text{ran}}[n]\}$ is triggered, performing as an information source.

Mathematically, it can be proved that the state transitions of the sequence $\{V_{\text{ran}}[n]\}$ satisfy the Markov character, providing a complex and unpredictive behavior. Moreover, according to (3), the state transition from $V_{\text{ran}}[n]$ to $V_{\text{ran}}[n+1]$ is in an analog manner. It means that the value set of V_{ran} is continuous in the defined state space. Hence, the thus designed Markov-chain-based random clock generator is able to produce an infinite number of states, fundamentally removing the resolution issue in its digital counterpart. In addition, the range of the state space is clearly defined by $V_M - \Delta V$ and $V_M + \Delta V$. It is completely independent of the state transition. Therefore, the randomization range can be confined precisely by choosing V_M and ΔV, without influencing the random behavior. As a result, it eliminates the necessity of additional signal processing, which is required in the thermal-noise-based random clock generator. This facilitates the efficient implementation of an on-chip random clock generator.

B. Design Consideration

From the design point of view, because the chaotic PL1D map is linear within the Markov partition, it can

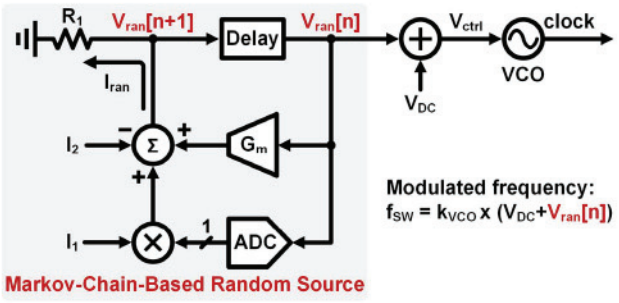

Fig. 5. Block diagram of continuous random frequency modulation using the Markov-chain-based random clock generator.

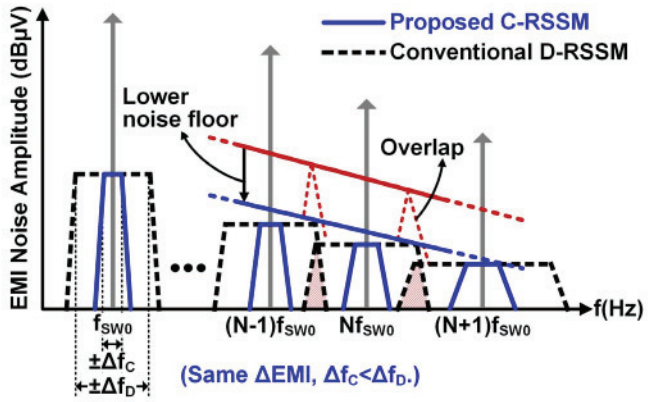

Fig. 6. Spectrum comparison of the proposed C-RSSM with the conventional D-RSSM.

be conveniently implemented on a standard CMOS process. As shown in the block diagram of Fig. 5, five basic analog blocks are employed to realize the state transition illustrated in (3). An analog-to-digital converter (ADC) is utilized to adjust the region of the random output $V_{\text{ran}}[n]$. Then, a binary multiplier quantizes the ADC's output to a current signal with respect to a reference current I_1, implementing the Markov partition. Further, assisted by a G_m-cell, a current adder completes the summing operation in the current domain. A constant current I_2 is used here to help define the parameter ΔV in (3). Accordingly, the intercepts of both lines in (3) can be determined. Then, the resultant current I_{ran} flows through a resistor R_1, generating the new random state $V_{\text{ran}}[n+1]$. Finally, a delay-cell is applied to update the random state, producing the random voltage sequence $\{V_{\text{ran}}[n]\}$. Based on the signal processing procedure, the relations between the design parameters (i.e., I_1, I_2, G_m, and R_1) and the system characteristics (i.e., V_M, ΔV, and k) can be derived as follows:

$$\begin{cases} I_1 = [(k-1) \times V_M + \Delta V]/R_1 \\ I_2 = 2 \times \Delta V / R_1 \\ k = G_m \times R_1. \end{cases} \tag{4}$$

Based on (4), the design parameters I_1, I_2, and R_1 can be determined according to the required nominal level V_M and randomization range ΔV. Meanwhile, G_m can be chosen to achieve an optimum stochastic property by controlling the slope k. In this way, both the range and randomness of the output V_{ran} can be well designed practically. The thus generated V_{ran} is then delivered to the input of a voltage-controlled-oscillator (VCO), modulating the clock frequency accordingly. Hence, it conducts SSM continuously and spreads the spurious noise at the fundamental frequency and its harmonics uniformly, achieving the desirable C-RSSM. As illustrated in the spectrum plot in Fig. 6, compared to the conventional D-RSSM, the proposed Markov C-RSSM is able to achieve a similar peak EMI reduction with narrower modulation range ($\Delta f_C < \Delta f_D$), avoiding the significant elevation of noise floor due to spectral overlap. As a result, in the proposed design, the peak EMI level is reduced effectively at the minimal cost of noise floor elevation and die area overhead.

C. Circuit Implementation

The core of the proposed C-RSSM technique is the Markov-chain-based random clock generator. Its circuit implementation

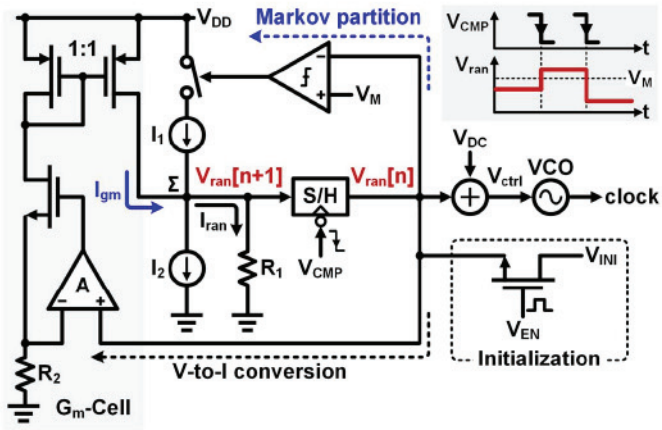

Fig. 7. Schematic of the Markov-chain-based random clock generator.

is shown in Fig. 7. The present state $V_{\text{ran}}[n]$ is converted into current I_{gm} by the G_m-cell to compute the next random state $V_{\text{ran}}[n+1]$. The transconductance G_m is determined as the reciprocal of the resistance R_2. The converted I_{gm} is then driven into a summation node Σ. Meanwhile, $V_{\text{ran}}[n]$ is compared to V_M. The comparison result multiplies the current I_1 in binary to implement the Markov partition. Finally, a fixed current I_2 is subtracted from the node Σ to generate the random current I_{ran}, leading to $V_{\text{ran}}[n+1]$, which is equal to $I_{\text{ran}} \times R_1$. It is derived that the ratio of R_1/R_2 determines the slope k in (3). By layout matching these two resistors, k could be well defined, ensuring the convergence of the Markov transitions. Triggered by the trailing edge of V_{CMP} from the feedback link, $V_{\text{ran}}[n+1]$ is sampled and added to V_{dc}, adjusting the VCO input V_{ctrl}, and hence, the clock frequency. Thanks to the Markov state transitions, V_{ctrl} varies randomly within $\pm\Delta V$ centered at $(V_{\text{dc}} + V_M)$, and the switching frequency is modulated accordingly. It should be noted that the random output V_{ran} would remain at zero without any random behaviors when the circuit is activated. In avoiding this "start-up" problem, $V_{\text{ran}}[n]$ is initiated to a voltage level V_{INI} by a short pulse signal of V_{EN} during the power-ON period. Based on the previous discussion, V_{INI} is selected within the desirable randomization range $[V_M - \Delta V, V_M + \Delta V]$.

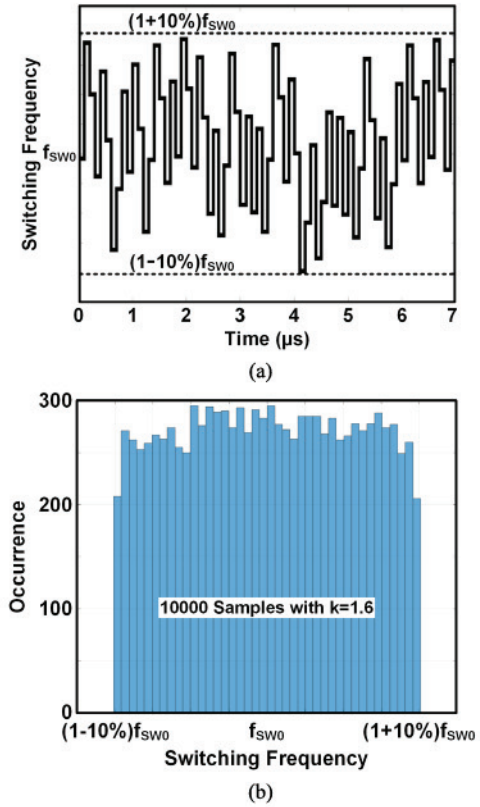

Fig. 8. (a) Simulated switching frequency modulation pattern and (b) switching frequency distribution of the proposed Markov-chain-based random clock generator.

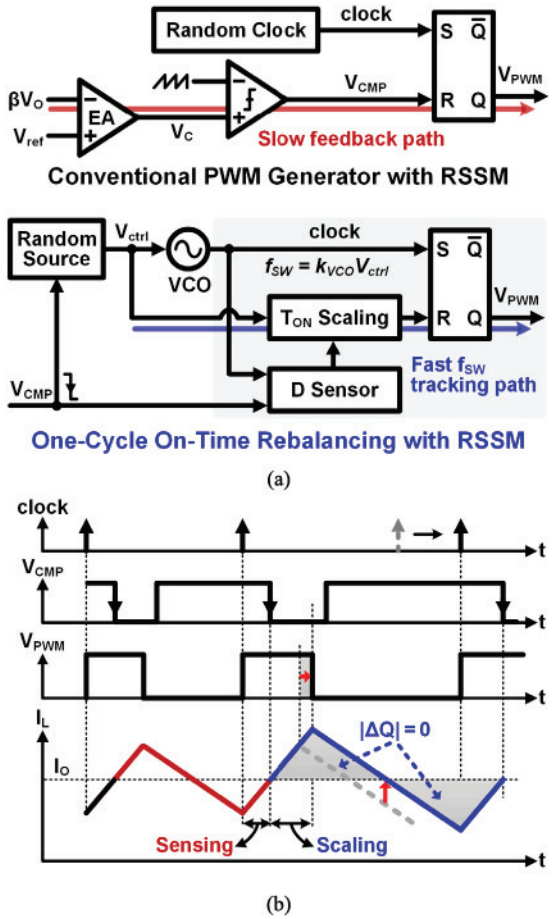

Fig. 9. Proposed one-cycle ON-time rebalancing scheme: (a) structure comparison with the conventional PWM generator and (b) operation principle with RSSM.

From the simulated switching frequency modulation, as shown in Fig. 8(a), the switching frequency traverses arbitrarily within the sideband of $\pm\Delta f_C$, creating a continuously and randomly distributed modulation pattern. Practically, to minimize the risk of V_{ran} being attracted to either zero or power supply V_{DD} due to the variations of the process, voltage, and temperature (PVT), k is designed as 1.6 here. The simulated switching frequency occurrences of 10 000 samples are shown in Fig. 8(b), illustrating almost uniform distribution.

III. One-Cycle On-Time Rebalancing

A. Design Principle

As addressed in Section I, although the conventional PWM control works well with fixed frequency switching for tight V_O regulation, it fundamentally suffers from V_O jittering issue when RSSM is applied, which is due to two reasons. First, the regulation loop is not able to predict the error on duty-ratio D induced by the switching frequency modulation. Thus, it cannot correct the ON-time T_{ON} in real-time to remain a constant duty-ratio. Second, the loop response is much slower than the switching frequency modulation, further deteriorating the situation. Based on this analysis, a one-cycle ON-time rebalancing scheme is proposed to eliminate the V_O jittering issue without influencing EMI attenuation by RSSM. As shown in Fig. 9(a), to compensate for the slow feedback loop in the conventional PWM generator, an additional fast switching frequency (f_{SW}) tracking path is created to modulate the ON-time synchronously with switching frequency modulation. For this, the one-cycle ON-time rebalancing module performs a two-step operation in each charging phase. As shown in the waveforms in Fig. 9(b), during the sensing phase, the duty-ratio D sensor detects the instant duty-ratio D, determined by the converter's PWM controller. By this, the loop regulation is assured. Then, during the scaling phase, by analyzing the sensed information of duty-ratio and the instant switching frequency from the output of Markov-chain-based random clock generator, the ON-time T_{ON} scaling block adaptively adjusts the length of ON-time proportionally to the VCO input V_{ctrl}. Hence, the ON-time, and thus, the duty-ratio of the converter are dynamically rebalanced to the instantly modulated switching frequency within one cycle, preventing V_O from jittering.

B. Circuit Implementation

Fig. 10(a) shows the schematic of the proposed one-cycle ON-time rebalancing circuit. A phase detector is applied to sense the duty-ratio D determined by the phase difference between the leading edge of the clock and trailing edge of V_{CMP}. The sensed duty-ratio is then memorized in the capacitor C_{cp} as voltage V_{cp} through time to voltage conversion by a charge pump. Controlled by the VCO input V_{ctrl}, the ON-time T_{ON} is thus dynamically scaled by converting

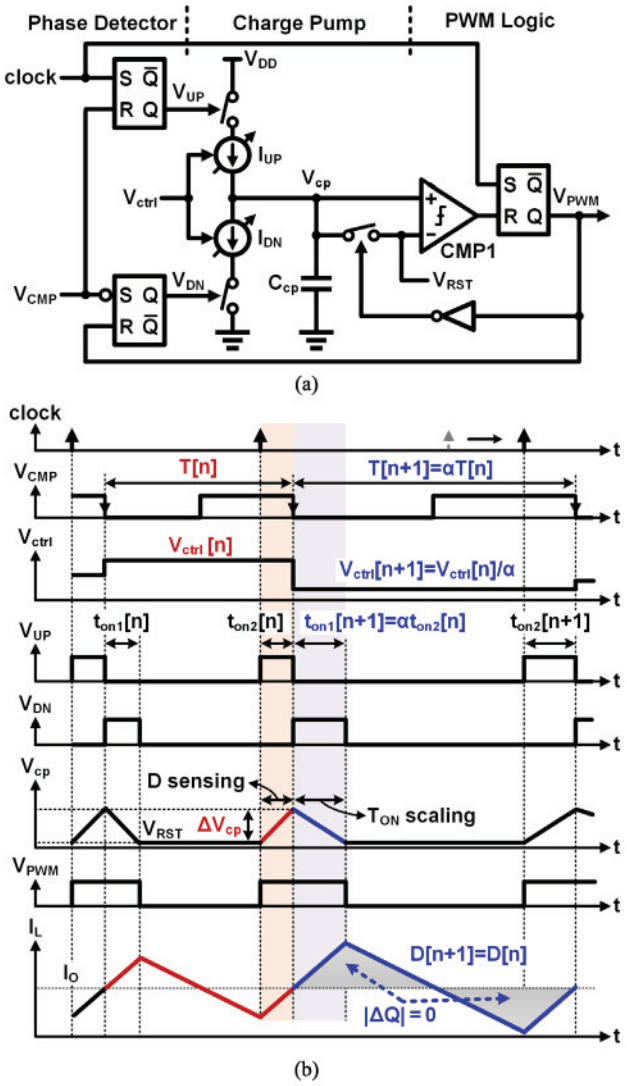

Fig. 10. (a) Circuit schematic and (b) operation waveforms of the one-cycle ON-time rebalancing scheme.

V_{cp} to time proportionally to the switching frequency. The operation is detailed in Fig. 10(b). As the trailing edge of V_{CMP} triggers switching frequency transition, instant switching cycle of the converter is defined between two adjacent trailing edges of V_{CMP}. Two cycles, $T[n]$ and $T[n+1]$ are shown in the waveforms. The relation between them is defined by a proportional coefficient α as follows:

$$T[n+1] = \alpha \times T[n]. \tag{5}$$

In steady-state, the ON-time T_{ON} in each cycle is split equally into t_{ON1} and t_{ON2} as follows:

$$t_{ON1} = t_{ON2}. \tag{6}$$

The operation could be explained by focusing on $t_{ON2}[n]$ and $t_{ON1}[n+1]$. The leading edge of the clock initiates the duty signal V_{PWM} and $t_{ON2}[n]$. The inductor current I_L then ramps up. Meanwhile, the phase detector sets V_{UP} to high, starting to charge C_{cp} with the current I_{UP}. Controlled by the VCO input $V_{ctrl}[n]$, I_{UP} is inversely proportional to $T[n]$. The $t_{ON2}[n]$ is terminated until V_{CMP} triggers low by the feedback loop and then V_{UP} is reset to stop charging C_{cp}. Thus, the induced capacitor voltage change ΔV_{cp} is derived as follows:

$$\Delta V_{cp} = (\gamma / C_{cp}) \times (t_{ON2}[n]/T[n]). \tag{7}$$

Here, γ is the inverse proportionality constant of the charge current I_{UP} to the switching period $T[n]$. Moreover, with (6), the duty ratio in the nth cycle, $D[n]$, is calculated as follows:

$$D[n] = 2 \times t_{ON2}[n]/T[n]. \tag{8}$$

Combining (7) and (8), ΔV_{cp} is proportional to half $D[n]$ as follows:

$$\Delta V_{cp} = (\gamma / C_{cp}) \times (0.5 \times D[n]). \tag{9}$$

Equation (9) implies that $D[n]$ is converted into the ΔV_{cp}, completing duty-ratio sensing. The $(n+1)$th cycle $T[n+1]$ begins after V_{CMP} flips to low. I_L continues to rise as V_{PWM} remains high. I_{DN} is enabled by the trailing edge of V_{CMP} to discharge C_{cp}. As the trailing edge of V_{CMP} updates the VCO input from $V_{ctrl}[n]$ to $V_{ctrl}[n+1]$, I_{DN} is inversely proportional to $T[n+1]$. When V_{cp} hits V_{RST}, the comparator CMP1 triggers to terminate $t_{ON1}[n+1]$ by resetting V_{PWM}. The charge conservation of C_{cp} makes

$$t_{ON1}[n+1] = \alpha \times t_{ON2}[n]. \tag{10}$$

Note that the duty-ratio in the $(n+1)$th cycle is calculated as follows:

$$D[n+1] = 2 \times t_{ON1}[n+1]/T[n+1]. \tag{11}$$

By inserting (5), (8) and (10) into (11), it is derived that

$$D[n+1] = D[n]. \tag{12}$$

Equation (12) implies that the duty-ratio D is stabilized cycle-by-cycle, rebalancing the inductor charge, and hence, eliminating the V_O jittering effect.

IV. System Implementation

The system is designed, as shown in Fig. 11. The Markov-chain-based random clock generator implements analog switching frequency modulation within a range of $\pm\Delta f_C$ centered at f_{SW0}, achieving a C-RSSM to spread the EMI noise uniformly. On the other hand, the one-cycle ON-time rebalancing module prevents the V_O from jittering induced by RSSM, balancing the EMI and voltage regulation performance of the converter. The power stage consists of two enhancement-mode GaN HEMTs as the power switches, M_{HS} and M_{LS}, respectively. Peak current-mode control is used in this design because of its fast transient response compared to the voltage mode control. A direct current resistance (DCR) current sensing strategy is employed here due to its low power and high accuracy. As shown in Fig. 11, an RC filter (R_S and C_S) integrates the voltage drop across the inductor L due to its direct-current resistance R_{DCR}. The voltage difference V_{CS} between C_S is equal to $(I_L \times R_{DCR})$ by designing the time constant as follows:

$$R_S \times C_S = L/R_{DCR}. \tag{13}$$

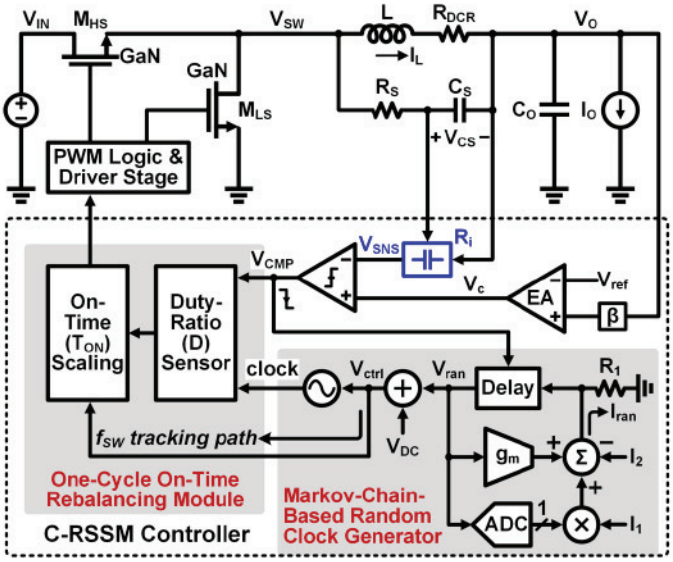

Fig. 11. Schematic of the proposed GaN-based switching power converter.

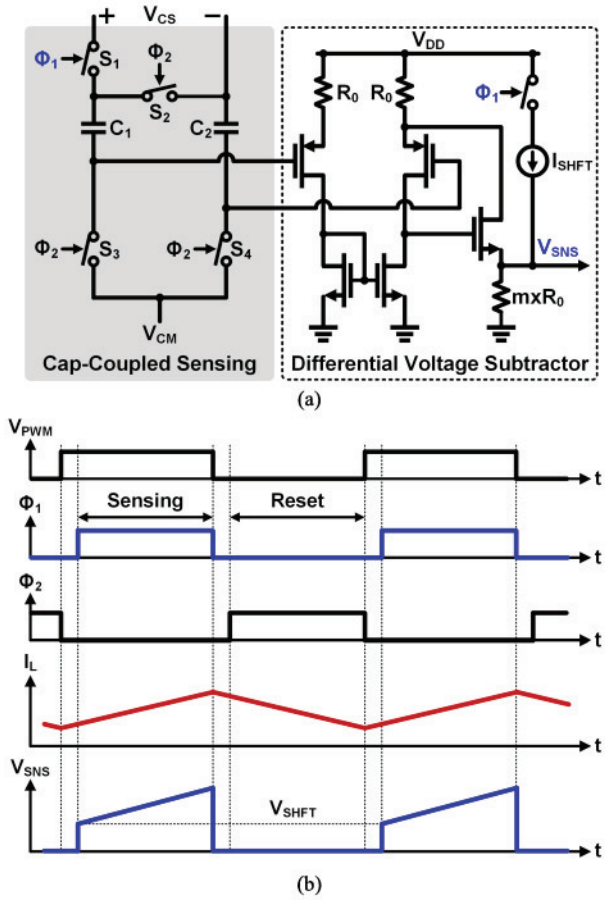

Fig. 12. Capacitive-coupled peak current sensing. (a) Circuit schematic and (b) operation waveforms.

Then a high-speed current sensor R_i is employed to implement the current sensing. Fig. 12 shows the schematic and operation waveforms of the sensor R_i. A capacitive-coupled sensing stage [23] is adopted here to capture V_{CS} through the differential coupling of C_1 and C_2. The sensed differential

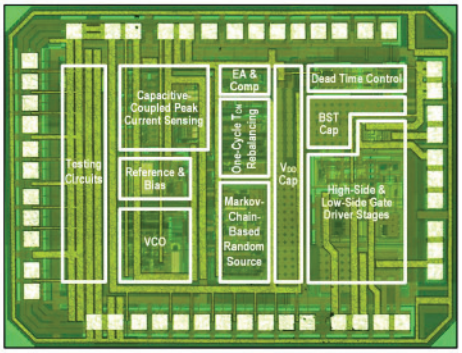

Fig. 13. Chip micrograph.

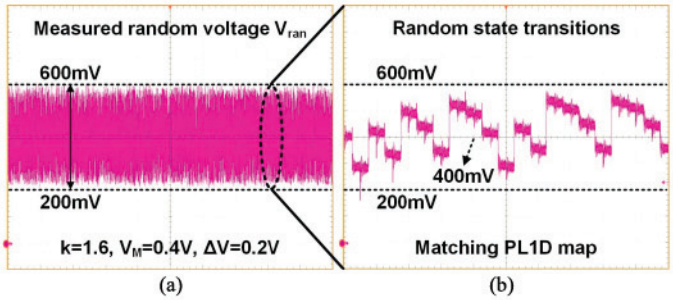

Fig. 14. Measured random voltage V_{ran} generated by the Markov-chain-based random clock generator. (a) Randomization range and (b) state transitions.

voltage is further converted into a single-ended output V_{SNS} by a voltage subtractor. As it is designed with two stages of source follower, the subtractor can operate at high speed. A constant current I_{SHFT} is added to elevate V_{SNS} by a dc level of V_{SHFT}. This dc level-shifting is used to ensure that V_{SNS} satisfies the range of the error amplifier's (EA's) output V_C. This is because V_{SNS} is compared to V_C in the feedback loop for V_O regulation. As to the operation, as shown in the waveforms, the leading edge of V_{PWM} triggers to turn on the high-side power switch M_{HS}. Then, the inductor current I_L begins to ramp up. In this phase, the switch S_1 in the capacitive-coupled sensing stage is closed by the signal Φ_1, whereas S_2, S_3, and S_4 are disconnected, completing the current sensing. When T_{ON} expires, V_{PWM} triggers low to turn off M_{HS}. At the same time, it triggers to disconnect S_1. The switches S_2, S_3, and S_4 are closed by Φ_1's non-overlap signal Φ_2, resetting the sensing circuit. As a result, the top plates of C_1 and C_2 are shorted to V_O, and the bottom plates are reset to a reference V_{CM}. This also sets the common-mode input of the differential voltage subtractor as V_{CM}. As V_{CM} is independent on V_O, the current sensor is able to support wide V_O range.

V. Experimental Verification

An experimental prototype of the design presented in this paper is fabricated in a 0.18-μm HV CMOS process [24]. The chip micrograph is shown in Fig. 13, with an active area of 1.54 mm^2. The Markov-chain-based random clock generator occupies 0.08 mm^2. Two enhancement-mode GaN HEMTs are used as the power switches. The converter delivers a maximum I_O of 1.5 A over an input range of 3 to 40 V.

To validate the design of the Markov-chain-based random generator, Fig. 14 shows the measured random voltage V_{ran}

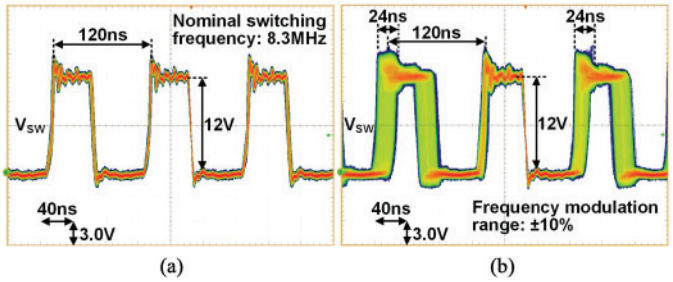

Fig. 15. Measured switching voltage at the switching node V_{SW} (a) without and (b) with Markov C-RSSM.

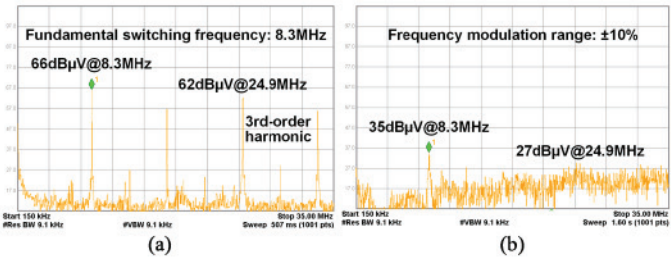

Fig. 16. Measured conducted EMI (from 150 kHz to 30 MHz), (a) without and (b) with Markov C-RSSM.

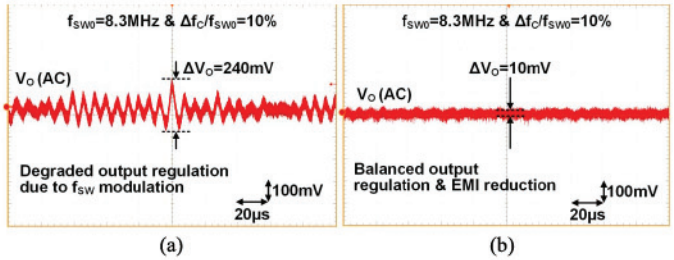

Fig. 17. Measured V_O jittering induced by RSSM with (a) conventional PWM control and (b) proposed one-cycle ON-time rebalancing scheme.

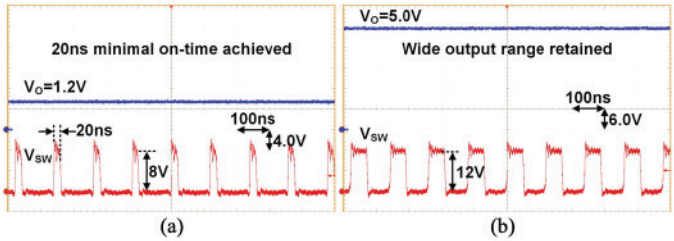

Fig. 18. Measured switching node V_{SW} with reference to the variable output voltage. (a) $V_O = 1.2$ V and (b) $V_O = 5.0$ V.

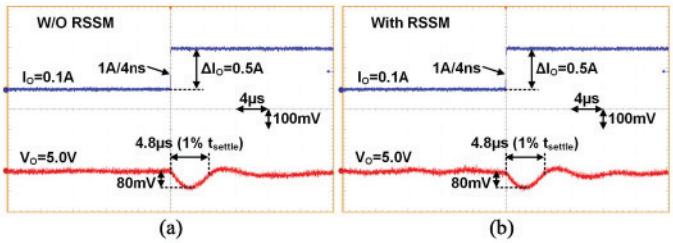

Fig. 19. Measured load step-up transient response. (a) Without and (b) with Markov C-RSSM.

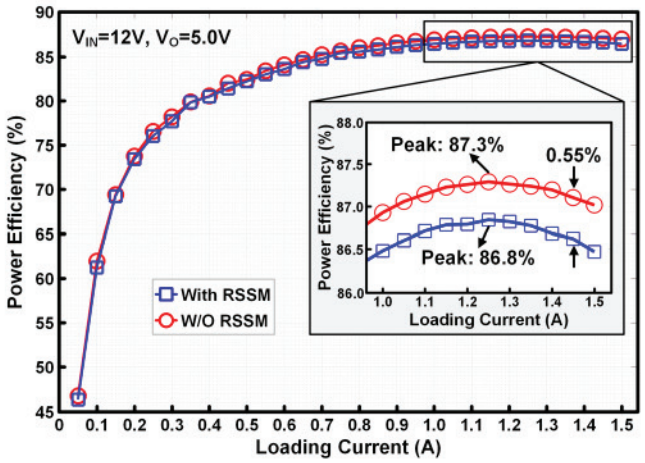

Fig. 20. Measured efficiency.

used for Markov-chain-based random clock generation. In consistence with the prediction, V_{ran} is modulated between 200 and 600 mV. Its transient behavior matches the PL1D map. Fig. 15 shows the measured switching node voltage V_{SW} of the switching converter. The proposed Markov C-RSSM technique modulates the switching frequency at the center frequency of 8.3 MHz with ±10% modulation range. For measuring the conducted EMI, a line impedance stabilization network (LISN) is connected between the input source and power converter. The LISN captures the ac component of the input voltage. It is then delivered to a spectrum analyzer. The measured conducted EMI noise spectra are shown in Fig. 16 when the converter operates with a 12-V input voltage source and delivers 1-A load current at the 5-V output. Compared to conventional PWM fixed-frequency operation, the Markov C-RSSM technique reduces the peak EMI noise by 31 dBμV at the fundamental frequency and 35 dBμV at the third-order harmonic, respectively.

To validate the one-cycle ON-time rebalancing scheme, Fig. 17 shows the measured output voltage V_O waveforms at the same test condition in Fig. 16. With the conventional PWM design, the peak-to-peak V_O jittering is measured up to 240 mV. Thanks to the proposed one-cycle ON-time rebalancing scheme, in this work, the jittering drops below 10 mV.

The measured switching behaviors at different input/output conditions are shown in Fig. 18 to illustrate the load regulation of the converter. Thanks to the fast speed capacitive-coupled current sensor, the design achieves 20-ns minimal ON-time in the proposed peak current mode control. As explained in Section IV, the common-mode input range of the current sensor is independent of V_O, supporting a wide output ranging from 1.2 to 5.0 V.

Fig. 19 shows the load transient responses of the converter to I_O step-up change. In response to 500-mA I_O change, the converter achieves a 1% settling time t_{settle} of 4.8 μs with a peak undershoot voltage of 80 mV. With no obvious difference from the case without the Markov C-RSSM technique, it is proven that the proposed technique does not deteriorate load transient performance significantly. Fig. 20 shows the measured power efficiency. The efficiency of the converter peaks at 86.8% with 1.25-A load current. The power penalty of adding the C-RSSM

TABLE I
PERFORMANCE COMPARISON

Design		ISSCC 2018 [15]	ISSCC 2017 [17]	CICC 2010 [18]	This Work
Process		55nm CMOS	0.35μm HV BCD	0.35μm CMOS	0.18μm HV CMOS
Power Switch		MOSFET	GaN HEMT	MOSFET	GaN HEMT
Control Mode		Hysteresis current mode	PWM voltage mode	PWM voltage mode	PWM current mode
Central Switching Frequency		1MHz	10MHz	1MHz	8.3MHz
Frequency Modulation Way		Discrete RSSM	Triangular modulation	Continuous RSSM	Continuous RSSM
Random Clock Generator Area		$(0.17mm^2)^1$	Not reported	Not reported	$0.08mm^2$
Frequency Modulation Range		-21%/+22%	±9%	±20%	±10%
Peak EMI Attenuation		35dBμV	33dBμV	16dBμV	35dBμV
V_O Jittering Suppression	Amplitude	Not reported	Not reported	18.1dB	>27.6dB
	Method	Pseudo hysteretic window	Not reported	Ramp compensation	One-cycle on-time rebalancing

[1] Estimated through the chip photo

technique and the corresponding circuit modules leads to less than 0.6% efficiency drop.

Finally, Table I compares this work with the prior arts. Thanks to the Markov C-RSSM technique, with the same peak EMI attenuation of 35 dBμV, this work requires 50% narrower frequency modulation range compared to the D-RSSM technique in [15]. Moreover, implemented on a much larger feature-size technology, the Markov-chain-based random clock generator consumes 53% less silicon area than its digital counterpart. On the other hand, compared to the C-RSSM technique in [18], this work achieves 119% higher peak EMI attenuation, and three times higher V_O jittering suppression.

VI. CONCLUSION

A GaN-based power converter with Markov C-RSSM technique and one-cycle ON-time rebalancing scheme is presented. With the use of an analog random switching frequency modulation, the Markov C-RSSM spreads the EMI spectra continuously and uniformly, attenuating the peak EMI without significant noise floor elevation. A one-cycle ON-time rebalancing scheme stabilizes the duty-ratio cycle by cycle, eliminating the RSSM-induced V_O jittering effect, and hence, improving the V_O regulation performance without influencing the EMI reduction. The experimental results successfully verify the effectiveness of the design.

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