A Two-Stage Cascaded Hybrid Switched Capacitor DC-DC Converter With 96.9% Peak Efficiency Tolerating 0.6V/µs Input Slew Rate During Startup

Efficient high-conversion-ratio power delivery is needed for many portable computing applications which require sub-volt supply rails but operate from batteries or USB power sources. Power management requires small volume, area and height while providing fast transient response. Past work has shown favorable performance of hybrid switched-capacitor (SC) converters to reduce the size of needed inductor(s), which can soft-charge high-density SC networks while supporting efficient voltage regulation [1]-[5]. However, challenges with the hybrid approach include flying capacitor voltage balance and achieving safe but fast startup. Rapid supply transients, including startup, can cause voltage stress on power switches if flying capacitors are not quickly regulated. Past approaches include precharge networks [3] or fast balancing control [5], but previously demonstrated startup times are on the order of milliseconds. This paper presents a two-stage cascaded hybrid SC converter that features fast nonlinear control with automatic flying capacitor balancing for low-voltage applications (i.e. 5V:0.4-1.2V from a USB interface). The converter is nearly standalone with all gate drive supplies generated internally. Measured results show peak efficiency of 96.9%, <36mV under/overshoot for 1A/µs load transients, and self-startup time on the order of 10µs (over 100× faster than previous work).

The powertrain and phase-wise equivalent circuits are shown in Fig. 1. The first stage uses a merged-interleaved 2:1 SC architecture, using switches $M_{1\alpha/\beta}$-$M_{4\alpha/\beta}$ to effectively rotate the positions of capacitors C_α-C_β. This provides a first 2:1 step down without charge sharing as $V_{C\alpha}$ and $V_{C\beta}$ always sum to V_{in}; it also helps reduce input bypass capacitance as one of C_α and C_β is always gnd-connected, providing low-impedance to the second stage. By switching at $f_{sw}/4$, losses in the 5V devices are reduced. The second stage operates like a 3-level Buck with 180nm ($1.8V_{nom}$; $1.98V_{max}$) switches at $f_{sw}/2$ except that the top power switch is removed, its function replicated by turning off (high-Z) $M_{2\alpha/\beta}$ and $M_{3\alpha/\beta}$ in phase φ_3. Removing this switch

simplifies gate driving and reduces conduction loss. In phases φ_1 and φ_3 capacitor C_2 is respectively charged and discharged; in phases φ_2 and φ_4 the switching node is gnd-connected to provide regulation. Thus, there are 8 phases in each period, with φ_5~φ_8 being identical to φ_1~φ_4 except that C_α and C_β swap connection.

Fig. 2 shows relevant portions of the gate drive circuit. Importantly, no external supplies are required for gate drivers; all bootstrap capacitors and gate-drive supplies (even for gnd-referenced switches) are integrated on chip. Gate drivers of $M_{3\alpha/\beta}$ are directly supplied from flying capacitors $C_{\alpha/\beta}$. Devices $M_{2\alpha/\beta}$ are bootstrapped from $C_{\alpha/\beta}$ when they are turned on so that only a small (shared to reduce area) capacitor C_{BS} is needed to maintain voltage in their off state. For switches not shown in Fig. 2, M_6 is supplied directly (and M7 bootstrapped) from flying capacitor C_2; $M_{1\alpha/\beta}$ and $M_{4\alpha/\beta}$ are bootstrapped from V_{in} and $C_{\alpha/\beta}$ respectively; M_5 bootstraps from V_{mid}. The level shifter uses a cascode-OTA structure which injects a current pulse by charging the large C_{GS} of a long-channel diode-connected stack; this current pulse is amplified and rectified in the linear OTA. The linear OTA maintains fast and symmetric rise-fall propagation delays while the diode-connected degeneration (reset between phases) provides a small hold-state current. The buffer chain uses skewed delays to reduce cross-conduction in the last (gate drive) stage.

Output voltage regulation and flying capacitor balance are achieved by a variation on modified ripple injection control (MRIC), proposed in [5]. MRIC is similar to hysteretic control (often used for buck converters) where output voltage, added to a representation of inductor current ripple $I_{L,AC}$, is compared to a reference within a hysteresis band. Shown in Fig. 3 the output of comparator *cmp1* represents a conventional ripple-injection control signal that in normal operation provides fast and accurate regulation: $I_{L,AC}$ is estimated by integrating $V_{x,nom} - V_{out}$, which is added to V_{out} with hysteresis and compared to V_{ref} by *cmp1*. A finite state machine is used to control the switching sequence. For fine regulation of flying capacitor voltages, an added feedback loop (*cmp2*) is used to regulate the 4th-order dynamics of the converter with a single sliding mode. The flying capacitor balance information is captured by integrating the switching node V_x compared to its ideal reference

$V_{x,nom}$ (~V_{in}/4); in a balanced state, the output of this integral is zero at the end of the switching state such that it has no effect on regulation. However, if V_x is too low (i.e. a capacitor is discharging with too-low voltage; or charging with too-high voltage), the integral will cause *cmp2* to switch, reducing the state duration such that less charge is drawn from the flying capacitor network, forcing the converter in the direction of balance. Two added features improve the converter dynamics during transients and startup. *Cmp3* compares the switching node to a minimum reference, $V_{x,min}$ to detect an extreme imbalance and stop the switching state early. *Cmp4* is used only during startup. Startup is identified when voltage on C_2 is significantly lower than its nominal voltage, indicated by V_x being above a high threshold ($V_{x,max}$) during φ_1 or φ_5. In startup mode, the finite state machine (FSM) which generates gate drive signals skips φ_3 and φ_7 so that C_2 is only charged but not discharged, accelerating balance. If startup is no longer detected, the converter automatically enters regular mode in the next period.

Fig. 4 shows measured data for load and line transients. Full-range load transients (0A→1A→0A) were applied with rise/fall time ≤1µs; respective under/overshoot were 32mV/36mV. Importantly, capacitor voltage balance is maintained, even in the case when I_{out} = 0A. For the line transient test, the input voltage rises from 4V to 5.2V within 4µs with less than ±10mV variation of $V_{out}-V_{ref}$. Settling time of the flying capacitor voltage is ~10µs. Fig. 5 shows converter startup with V_{in} rising from 0V to 5V in 8µs (0.6V/µs). Different stages in the startup process are seen in the zoom of the V_x waveform. During 0~4µs, V_{in} is rising but no switching event happens as internal nodes and capacitors are charging. In 4~7µs, the converter is in startup mode since no lower pulse of V_x (i.e. φ_3 and φ_7 where C_2 is connected between V_x and GND) is observed; as gate drivers in the second stage wait for C_2 to charge, switches $M_{6/7}$ are subject to body-diode conduction. In 7~12µs, C_2 is charged sufficiently close to nominal voltage and the converter is in regular mode, where the control loop is regulating both output and flying capacitor voltage. The converter enters steady state at 12µs. V_{out} tracks V_{ref} within 6mV (<1.1% SSE) for the entire output voltage range from 0.4V to 1.2V. The overall

peak efficiency of 96.9% is achieved at 150mA with 5V:1.2V step down. The converter maintains up to 85.5% efficiency at 5V:0.4V (VCR = 12.5).

The converter prototype is fabricated in 180nm CMOS with 7.8mm^2 die area, dominated by bootstrap caps and power devices, Fig. 7. Flying capacitors are die-attached using a custom gold-stud/solder process. A 240nH inductor and output cap are on the PCB back side. A 10nF on-die cap is used to filter V_{out} (remove artifacts from bondwire inductance) in the control feedback path. Relative to work with comparable voltage and current, this work achieves higher efficiency at higher conversion ratios with similar power density (summing die + passive comp. area, thus trying to compare fairly by not counting the benefit of die-attached or PCB-backside passives). The major advance here is faster load/line regulation and startup time over 100× faster than the closest prior art.

Acknowledgements:

This work was supported in part by the Power Management Integration Center (PMIC) an NSF I/UCRC, award number IIP 1822140.

References:

[1] W. Liu et al., "A 94.2%-peak-efficiency 1.53A direct-battery-hook-up hybrid Dickson switched-capacitor DC-DC converter with wide continuous conversion ratio in 65nm CMOS," ISSCC, pp. 182-183, Feb. 2017.

[2] L. Chu et al., "A three-level single-inductor triple-output converter with an adjustable flying-capacitor technique for low output ripple and fast transient response," ISSCC, pp. 186-187, Feb. 2017.

[3] C. Schaef et al., "A 93.8% Peak Efficiency, 5V-Input, 10A Max ILOAD Flying Capacitor Multilevel Converter in 22nm CMOS Featuring Wide Output Voltage Range and Flying Capacitor Precharging," ISSCC, pp. 146-148, Feb. 2019.

[4] J. Baek et al., "A Voltage-Tolerant Three-Level Buck-Boost DC-DC Converter with Continuous Transfer Current and Flying Capacitor Soft Charger Achieving 96.8% Power Efficiency and 0.87µs/V DVS Rate," ISSCC, pp. 202-204, Feb. 2020.

[5] J. S. Rentmeister and J. T. Stauth, "A 92.4% Efficient, 5.5V:0.4-1.2V, FCML Converter with Modified Ripple Injection Control for Fast Transient Response and Capacitor Balancing," CICC, pp. 1-4, Mar. 2020.

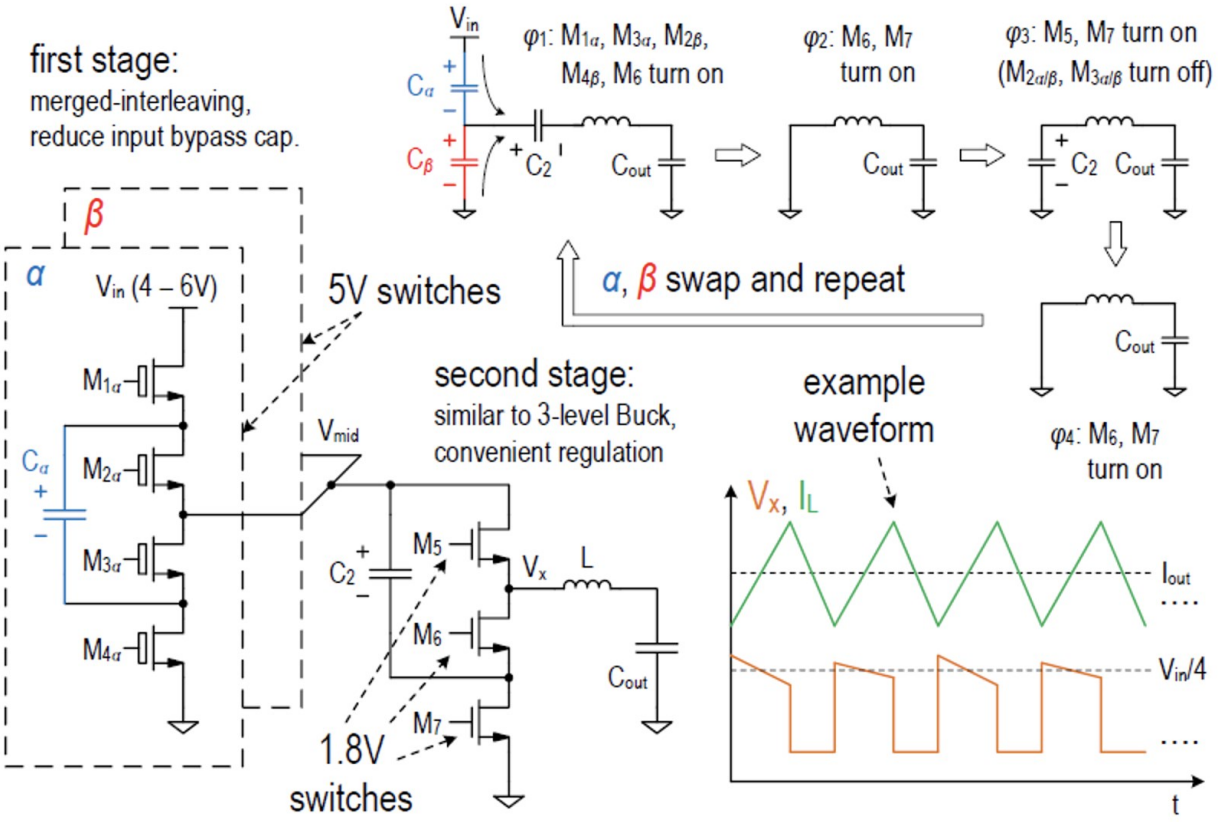


Fig. 1: Schematic, phase-wise equivalent circuits and example waveform of the proposed converter.

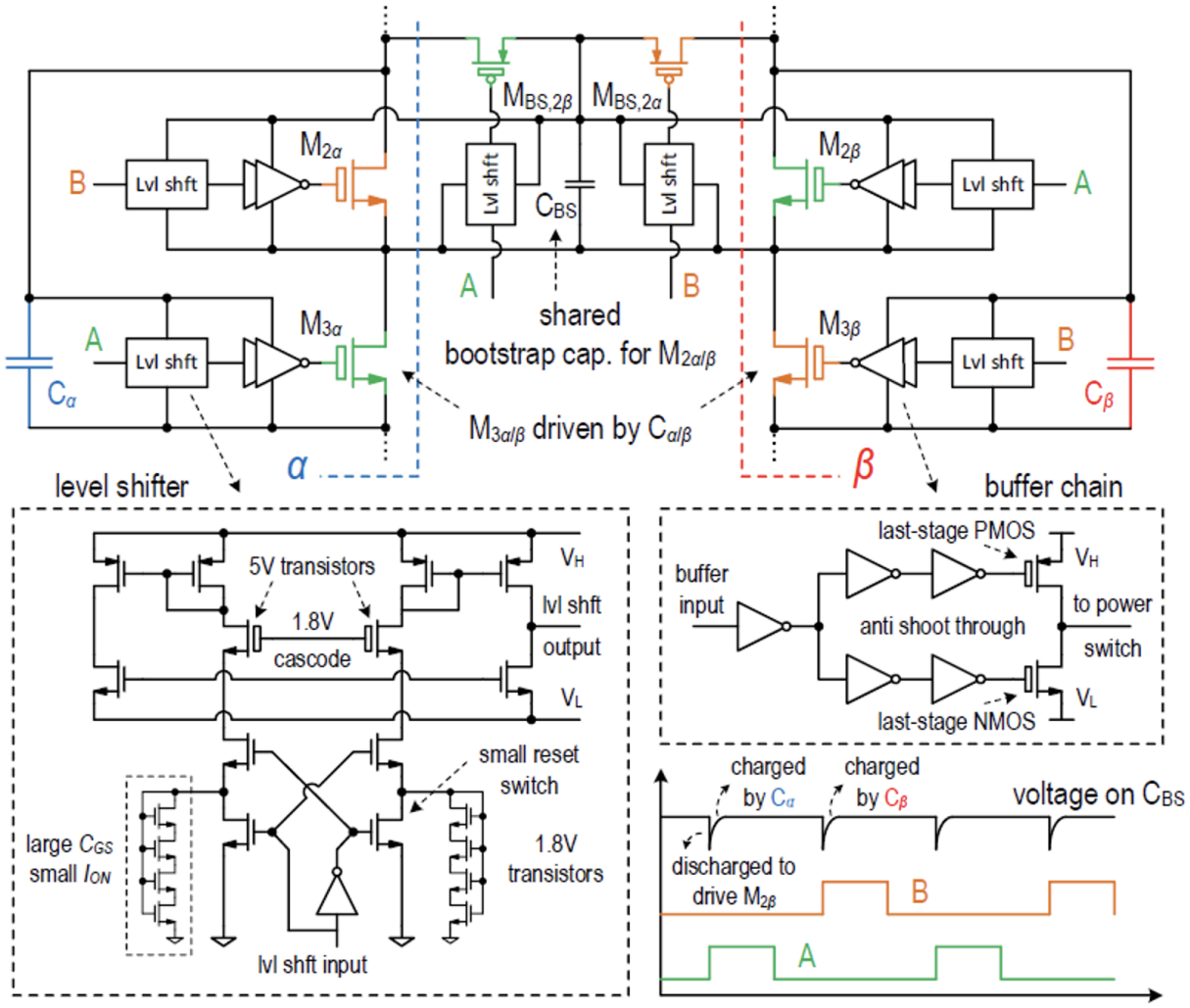


Fig. 2: Illustration of the gate drive strategy with circuit details of the level shifter and buffer chain.

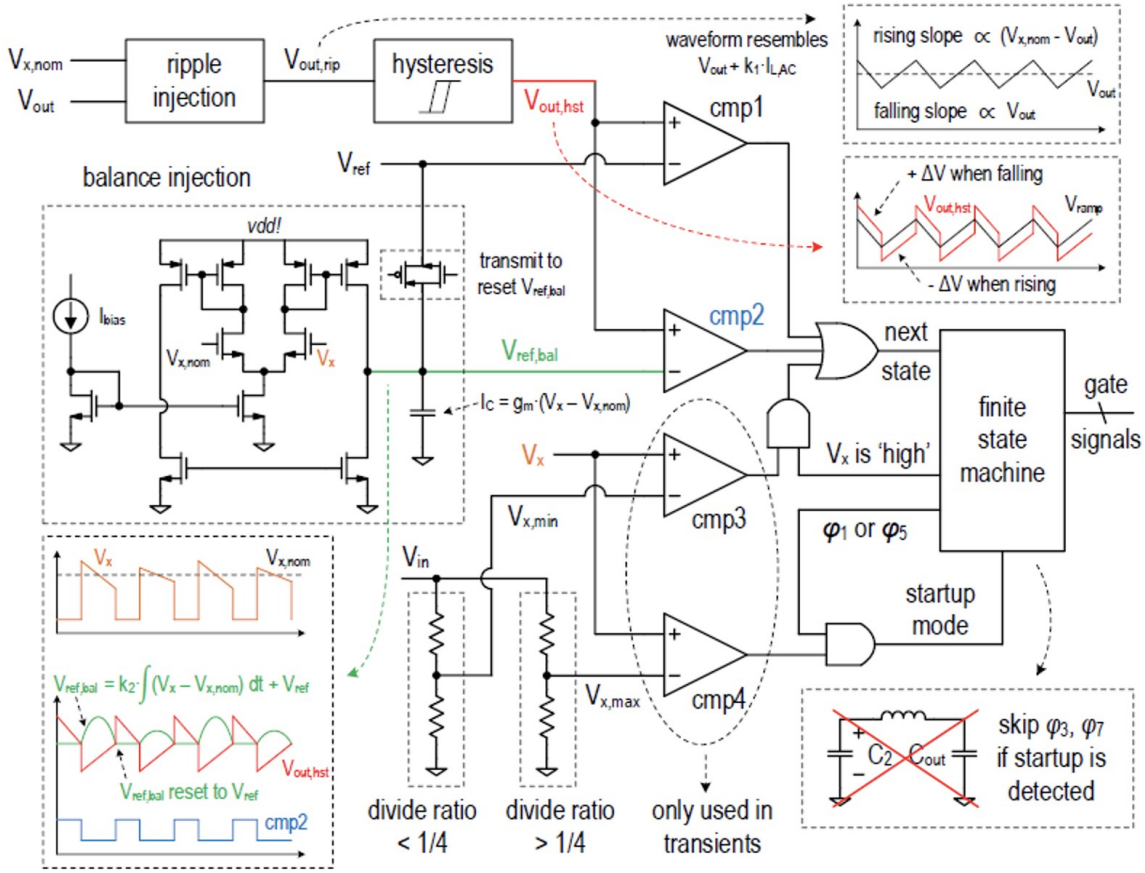


Fig. 3: Simplified block diagram of modified ripple injection control with additional phase skipping technique.

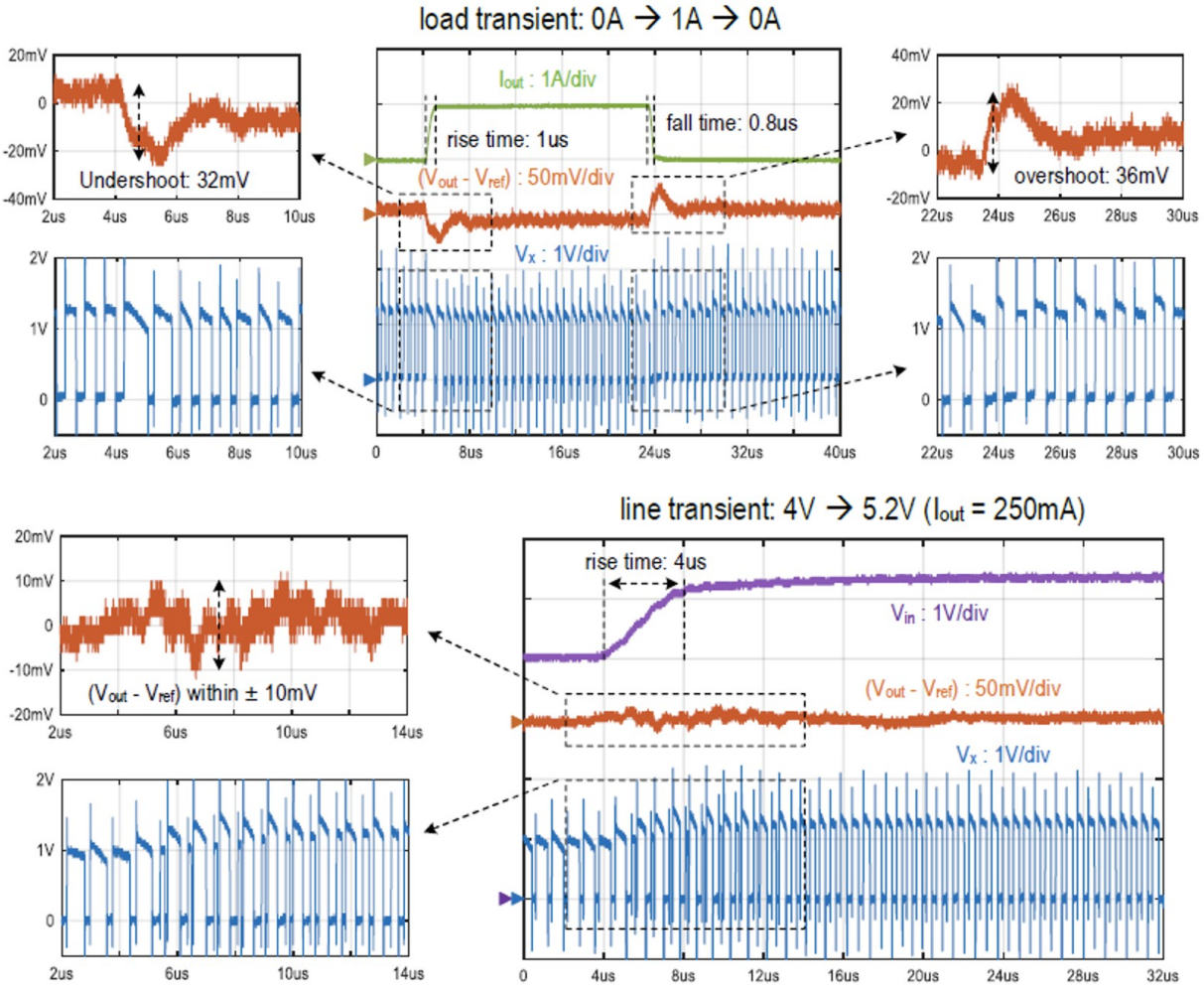


Fig. 4: Measured converter response to rising/falling load transient and rising line transient.

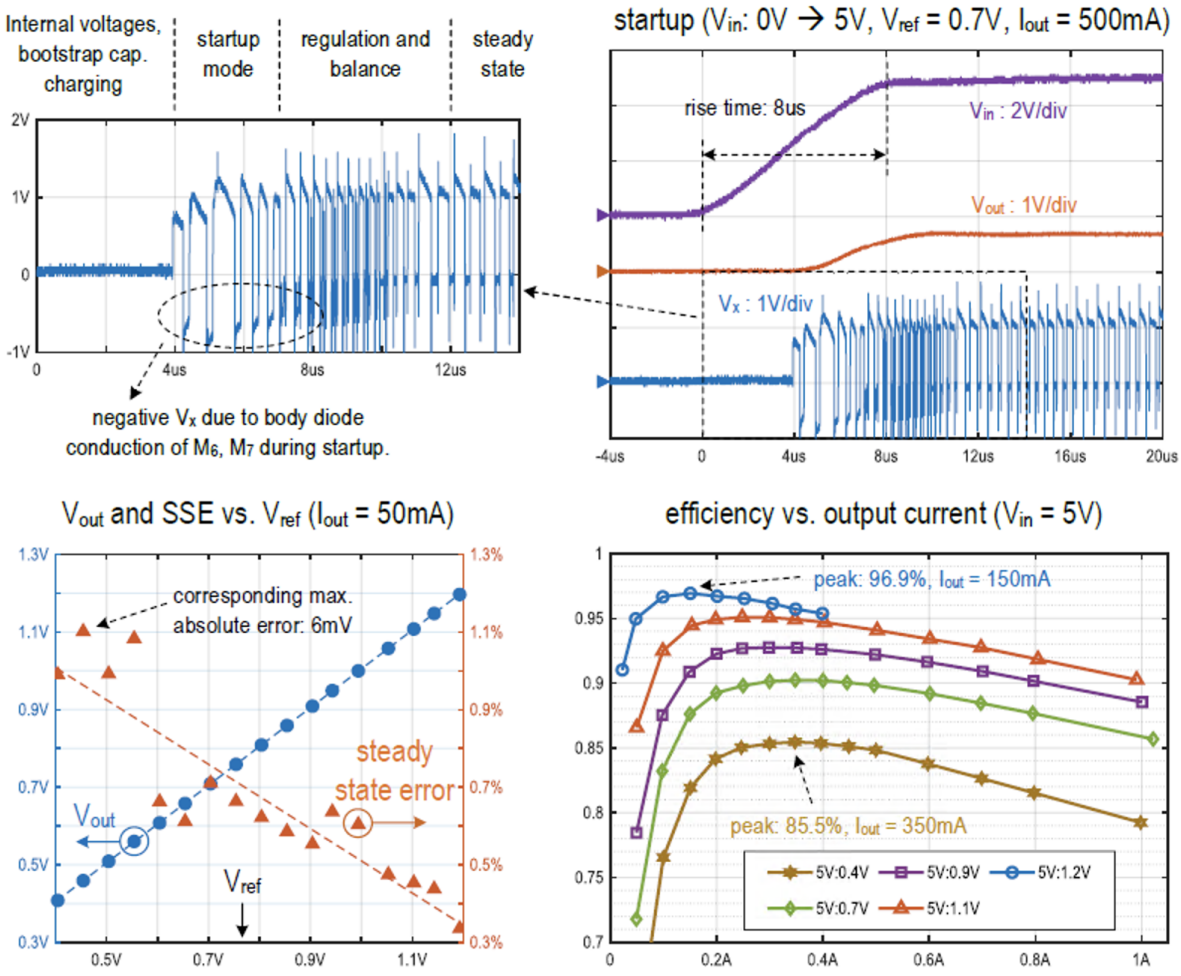
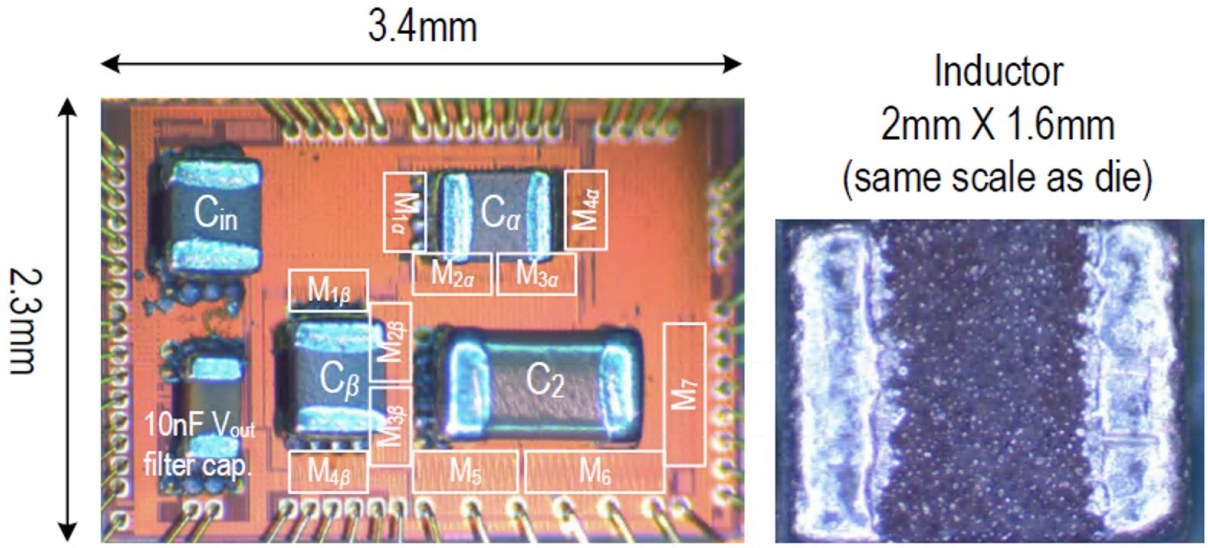


Fig. 5: Measured converter startup waveform, steady-state regulation accuracy and efficiency.

	Liu ISSCC17	Chu ISSCC17	Schaef ISSCC19	Baek ISSCC20	Rentmeister CICC20	This work
Topology	Hybrid Dickson	3-level Buck	4-level FCML	3-level Buck-Boost	5-level FCML	Hybrid Cascaded SC
Technology	65nm	28nm	22nm	90nm	180nm	180nm
Input Voltage	3 – 4.5V	3 – 4.5V	3.7 – 5V	2.5 – 5V	4 – 5.5V	4 – 6V
Output Voltage	0.3 – 1V	0.8 – 1.45V	0.8 – 1.8V	0.4 – 9V	0.4 – 1.2V	0.4 – 1.2V
Max. I_{out} (@ V_{out})	1.05A† (0.95V)	1A (1.15V*)	10A (1.8V)	1A (4.5V)	1.4A (1V)	1A (1.1V)
Control	Integrated	Integrated	Off-chip	Integrated	Integrated	Integrated
Flying Capacitor	3 x 22µF	On-chip	2 x 13.2µF	10µF	3 x 4.7µF	2 x 4.7µF + 10µF
Output Capacitor	22µF	2µF	18µF	4.7µF	10µF	14.1µF
Inductor	470nH	2.2µH	10nH	2.2µH	240nH	240nH
Max. Power Density††	0.10W/mm²	N/A	0.95W/mm²	N/A	0.11W/mm²	0.10W/mm²
Max. Eff. (@ VCR)**	94.2% (4.4)	89.6% (3.8*)	93.8% (2.8)	96.8% (1.2)	92.4% (4.6)	96.9% (4.2)
Max. VCR (@ Eff.)	8.2 (86.5%†)	3.8* (89.6%)	6.3 (85.8%†)	N/A	13.8 (80.2%†)	12.5 (85.5%)
Startup Vin rise time	N/A	N/A	7ms (0 → 5V)	N/A	2ms (0 → 5.5V)	8µs (0 → 5V)

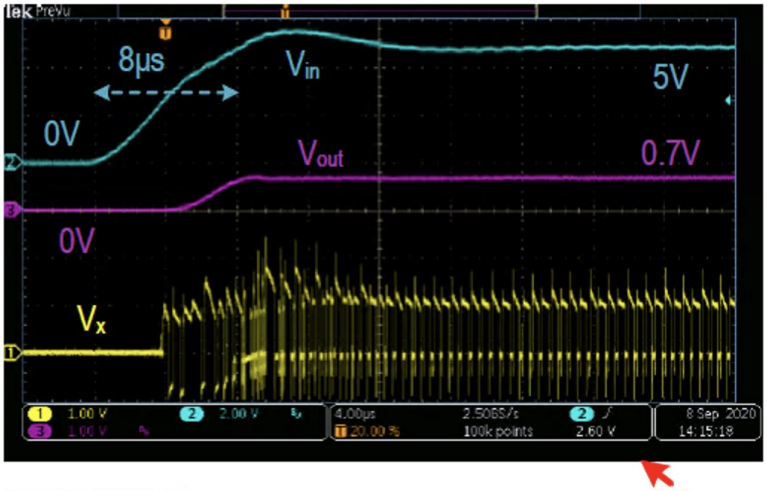
* V_{out} assumed as the average of multiple output.
† Estimated from graph
** Voltage conversion ratio (VCR) = V_{in}/V_{out}
†† Area counts active die, flying capacitor and inductor.

Fig. 6: Performance summary and comparison with prior art.



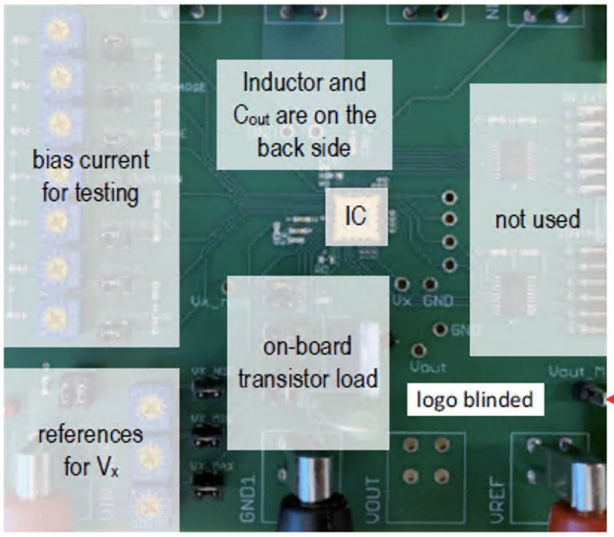
component	C_{in}	C_{α}	C_{β}	C_2	L
footprint	0201	0201	0201	0402	0806
nominal value	4.7µF	4.7µF	4.7µF	10µF	240nH
est. derated value	0.7µF	1.6µF	1.6µF	6.4µF	N/A

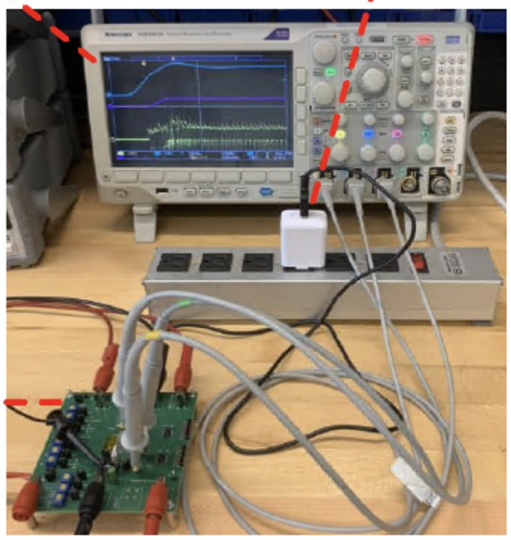
Fig. 7: Annotated die photo with component details.



startup caused by 'hard' connect: V_{in} has an overshoot due to cable inductance; the converter functions normally.

5V USB adapter, cable connected to V_{in}





PCB top view

test setup for direct plug to real USB

Fig. S1: Demonstration of direct plug to real USB supply; annotated PCB and exported waveform.

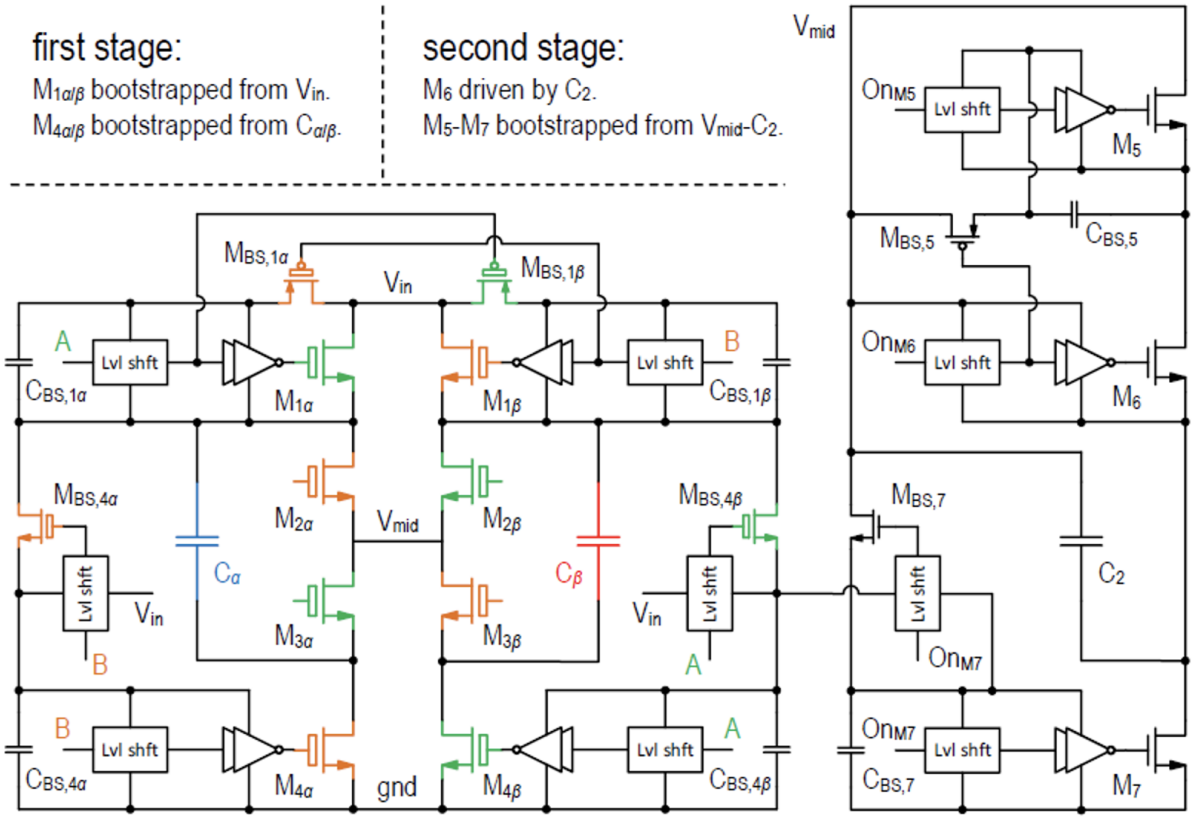


Fig. S2: Gate drive strategy for other power switches.

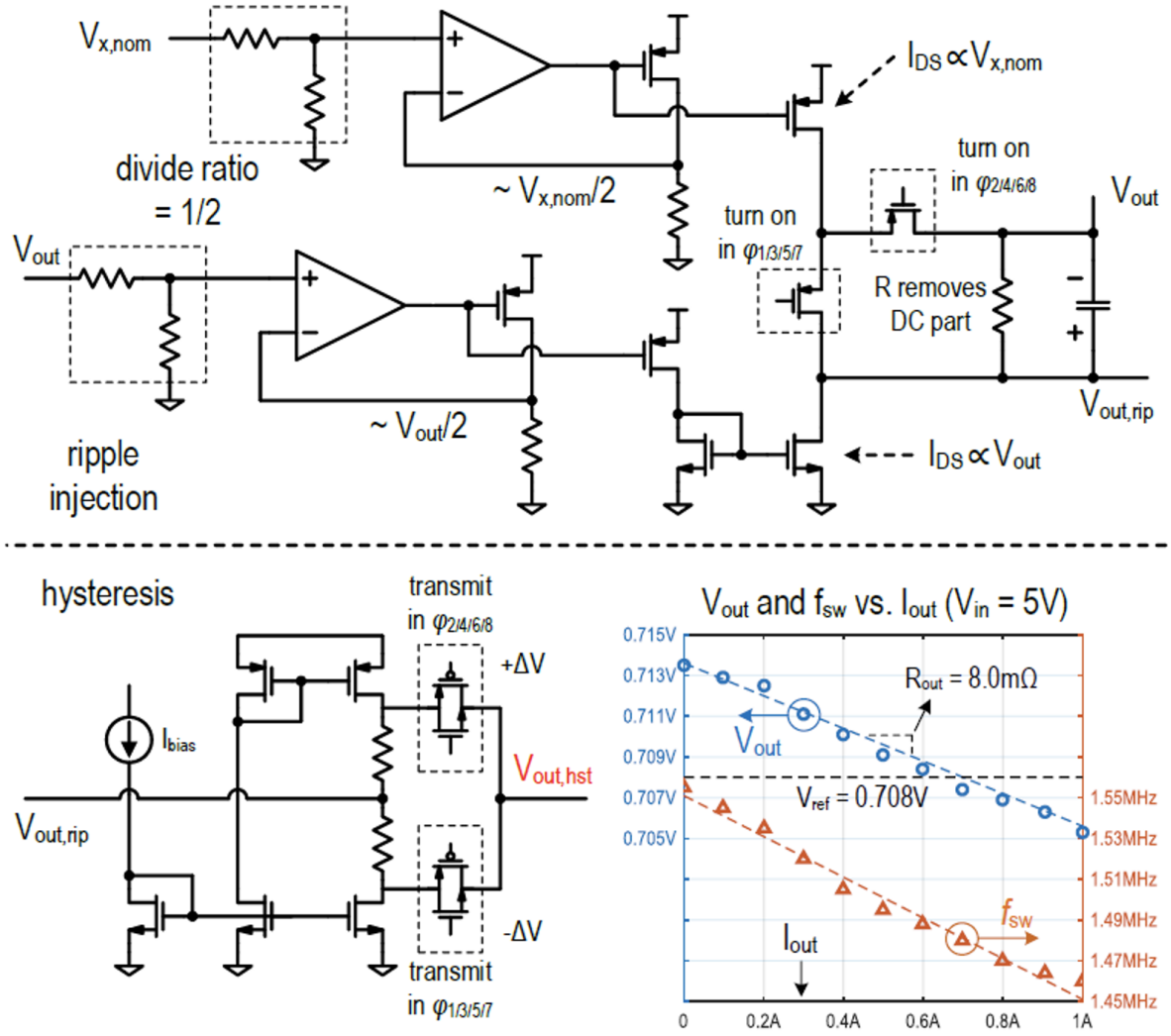


Fig. S3: Additional circuit details in the control block; more closed-loop steady-state characteristics.