Temperature-Dependent Current Dispersion Study in β-Ga_2O_3 FETs Using Submicrosecond Pulsed I–V Characteristics

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***Abstract*— A comprehensive study of drain current dispersion effects in β-Ga_2O_3 field-effect transistors (FETs) has been done using dc and pulsed measurements. Both the virtual gate effect in the gate–drain access region and mobile traps under the gate are the most plausible explanations for the experimentally observed pulsed current dispersion and high-temperature threshold voltage shift, respectively. Unpassivated devices show significant current dispersion between dc and pulsed *I–V* response in gate lag measurements characterized by time constants in the range of 400–690 μs both at room temperature and higher temperatures. The increasing time constant with temperature suggests a complex electron capture and emission process in the virtual gate. The reactive ion etching step during the device fabrication is most likely responsible for introducing the traps. The effect of traps can be minimized by using surface passivation layers, in this case, silicon nitride, which shows significant improvement in the current dispersion. This work demonstrates the detrimental effect that the traps can have on the current dispersion, which significantly limits the high-frequency operation of the device.**

***Index Terms*— β-Ga_2O_3, current dispersion, interface traps, pulsed *I–V*, virtual gate.**

I. Introduction

BETA gallium oxide has garnered a lot of interest of researchers across the globe because of its attractive material properties, such as ultrawide bandgap of ~4.8–4.9 eV [1], [2], good electron mobility, high breakdown field strength of 8 MV/cm [3]–[6], and also the ease of growing high-quality epitaxial films with controllable doping [3], [7]–[13] on melt grown bulk crystals. The large breakdown field strength translates to high Baliga's Figure of Merit (*BFoM*), making it superior candidate for power device applications. Several groups have demonstrated kilovolt class field-effect transistors (FETs) and Schottky diodes [5], [14]–[25]. In addition, β-Ga_2O_3 (Ga_2O_3) also has a high Johnson's Figure of Merit (*JFoM*) due to the large calculated electron velocity [26], which has been experimentally verified [27]. High *JFoM* implies that β-Ga_2O_3 is also suitable for high-frequency devices, such as gigahertz switches and RF amplifiers. Recently, a few groups have successfully demonstrated β-Ga_2O_3 FETs with current gain cutoff frequencies (f_t) in the gigahertz range [28]–[30]. Xia *et al.* [33] reported the highest f_t of 27 GHz in a delta-doped β-Ga_2O_3 FET with regrown ohmic contacts.

In addition to the cutoff frequencies, another important factor for the high-frequency performance of the device is dc to RF drain current dispersion, which causes transconductance to collapse as the frequency of operation increases with an associated knee-walk-off phenomenon. This is primarily caused by interface and/or buffer traps that act as generation and recombination centers. The transient response analysis using pulsed current–voltage measurements is a popular method to identify the type and location, both physical and energy, of the trap. This method has been widely used to study dispersion in GaN-based devices [32]–[37], while only a few reports exist on Ga_2O_3 devices.

There are two kinds of Ga_2O_3 RF FET devices reported, namely: 1) the source/drain (S/D) regions are either regrown or ion-implanted and 2) the S/D n^+ layers are grown and then removed from the channel region by reactive ion etching (RIE), which are called recessed gate FETs. The recessed gate process requires the channel to be exposed to RIE, which has been identified to introduce plasma damage and interface states [38]–[41]. This makes it vital to study the effect of traps and find ways to mitigate their detrimental effects on the device performance. There have been very few studies, specifically on Ga_2O_3 devices. Moser *et al.* [42] have reported pulsed large-signal power performance of Ga_2O_3 MOSFET. They have analyzed continuous and pulsed output power to provide evidence of the presence of traps for the observed dispersion. In contrast, in a previous report, Moser *et al.* [45] show pulsed current–voltage characterization on a 200-nm bulk channel FET, which shows no appreciable

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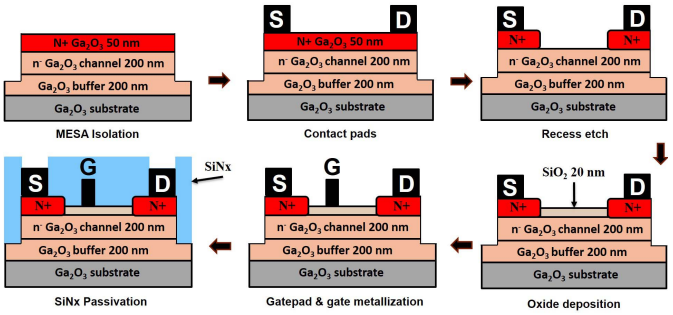

Fig. 1. Figure highlights major steps in fabrication process flow of the device in this study.

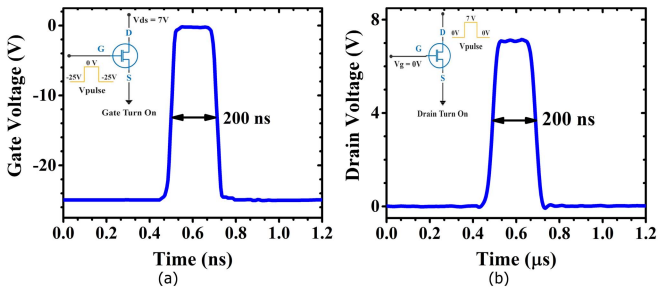

Fig. 2. (a) and (b) 200-ns gate and drain input voltage pulse shapes. (Inset) Schematic representation of measurement setups for gate and drain turn-on measurements, respectively.

current dispersion. A pulsed large-signal RF performance was reported by Singh *et al.* [44], which shows negligible dc-RF dispersion with microsecond pulses. McGlone *et al.* [47]–[49] explore buffer traps in a δ-doped Ga_2O_3 structure using the deep level transient spectroscopy (DLTS) and double-pulsed I–V measurements. Joishi *et al.* [50] report double-pulsed current–voltage measurement using a 5-μs pulse width on a Si δ-doped Ga_2O_3 FET, which shows drastic improvement in current after *in situ* passivation. Nevertheless, a significant knowledge gap exists in the dc-RF dispersion and mitigation strategies for Ga_2O_3 FET devices. In this work, we report a comprehensive temperature-dependent dc-RF dispersion analysis in Ga_2O_3 MOSFETs using a minimum pulse width of 200 ns. We provide the plausible origin of the dc-RF dispersion and the nature and location of traps along with the mechanism of capture and emission processes. We also first report the effectiveness of silicon nitride passivation in reducing the dc-RF current dispersion in Ga_2O_3 MOSFETs.

II. Experimental Details

A cross section of the device layers is shown in Fig. 1. A 200-nm-thick Si-doped (7×10^{17} cm^{-3}) channel and 50-nm highly Si-doped (1×10^{19} cm^{-3}) ohmic capping layers were grown homoepitaxially on top of 200-nm unintentionally doped (UID) Ga_2O_3 buffer layer on Fe-doped semi-insulating substrates. All the growth was carried out at 700 °C by ozone molecular beam epitaxy (MBE) by Novel Crystals Inc., Japan. Fig. 1 shows the schematic of the device fabrication; electron beam lithography (EBL) was used in all the steps. Device isolation etch was first performed using inductively coupled plasma RIE (ICP RIE) with BCl_3/Ar (35/5 sccm, 35 mTorr) chemistry. Next, Ti/Au/Ni source and drain contacts were deposited by e-beam evaporation followed by a 1-min 520 °C N_2 anneal to aid the formation of ohmic contacts. Followed by this, BCl_3/Ar gate recess etch was performed between source and drain ($L_{sd} = 0.5\ \mu$m) to remove the 50-nm ohmic capping layer. Atomic force microscopy was used to confirm the capping layer removal. A 20-nm plasma atomic layer deposition (ALD) SiO_2 was deposited as a gate dielectric layer and subsequently annealed at 450 °C to improve its dielectric properties. For probing, the oxide on the source and drain contact pads was removed using CF_4/Ar RIE. Finally, a Ti/Au gate contact pad and gate were deposited to complete the fabrication for the prepassivation study. A 250-nm-thick plasma-enhanced chemical vapor deposition (PECVD) silicon nitride (SiN_x) was deposited 300 °C to study the passivation of the interface states. The process used SiH_4 (20 sccm) and NH_3 (30 sccm) precursors at a pressure of 1900 mTorr. SiN_x was removed from the source/drain and gate contact pads to facilitate the probing.

DC current–voltage (I–V) measurements were performed using an HP4155B semiconductor parameter analyzer on an MS-TECH 1000H temperature-controlled probe station. Pulsed I–V measurements were done using an *Auriga AU-5* high-voltage pulsed I–V setup capable of sourcing 100 V/200 ns at the input port and 200 V/200 ns at output port with the 20-ns rise and fall times. The device was probed using a coplanar waveguide (CPW) RF probes to ensure minimum reflections at the probe-device interface (see Fig. 2).

To analyze the trapping/detrapping response of traps, the well-known gate-lag and drain-lag measurement technique was implemented as follows:

1) *Gate Turn-On:* The gate bias is pulsed from off state ($V_g = -25$ V) to on state ($V_g = 0$ V) while maintaining a constant drain bias. Complete I–V curves are obtained by sweeping V_d from 0 to 7 V.
2) *Drain Turn-On:* The drain bias is pulsed from off state ($V_d = 0$ V) to on state ($V_d = 7$ V) while maintaining a constant gate bias. Complete I–V curves are obtained by sweeping V_g from −25 to 0 V.

For each study, the pulse width was varied from 200 ns to 1 ms with a pulse period of 20 ms to allow sufficient time for the traps to regain their original state after every on-pulse. The low duty cycle also ensures that device self-heating effects are minimized. For each pulsed measurement, the recorded I_d value was averaged over the last 10% time window of the pulse. S-parameter measurements were carried out using *Agilent E5071* series ENA.

III. Results and Discussion

The final dimensions of the fabricated device are gate length (L_g) = 112 nm, source–gate spacing (L_{sg}) = 50 nm, and gate–drain spacing (L_{gd}) = 340 nm. Fig. 3 shows the SEM micrograph of the fabricated device.

A. DC I–V Analysis

Fig. 4(a) and (b) shows the measured I_d–V_d characteristics at room temperature and 200 °C, respectively. At room

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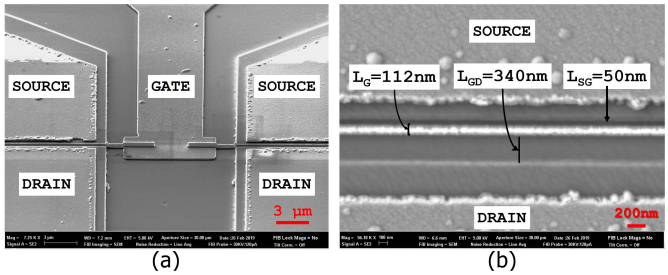

Fig. 3. (a) SEM micrograph of the device showing large source and drain contact pads. (b) Zoomed-in SEM view of the gate recess region showing intrinsic part of the device.

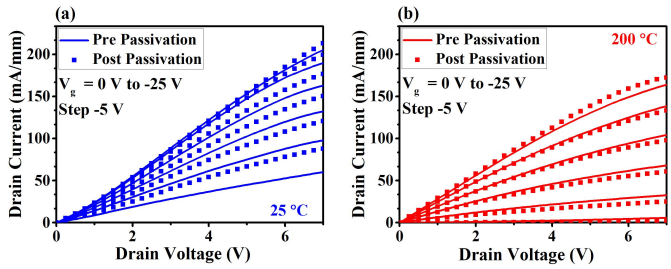

Fig. 4. (a) Static I_d–V_d comparison before the passivation (line) and after passivation (symbol) at room temperature. (b) Static I_d–V_d comparison before the passivation (line) and after passivation (symbol) at 200 °C.

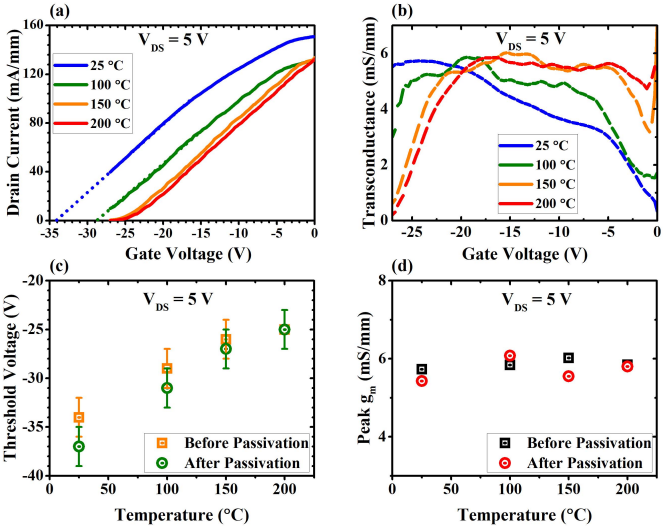

Fig. 5. (a) I_d–V_g (left) and corresponding (b) g_m–V_g (right) plots before passivation at room temperature (blue), 100 °C (green), 150 °C (orange), and 200°C (red). (c) V_{th} shift with temperature data before and after passivation shows a similar monotonic positive shift in V_{th} with temperature. The change in V_{th} at room temperature is attributed to the errors in extrapolation of V_{th}. (d) Peak g_m versus temperature data before and after passivation indicates little to no change in maximum static g_m.

temperature, we see incomplete turnoff even at $V_g = -25$ V. It is attributed to the 200-nm-thick channel with moderately high doping and a smaller gate length resulting in poor gate electrostatics. Gate voltages lower than −25 V were avoided to protect devices from gate dielectric electrical breakdown. The short-channel effects are also evident due to the shorter gate length. A maximum current of 210 mA/mm was recorded for this device at $V_g = 0$ V. Nonlinear behavior of source–drain contacts can also be seen in the graph, which is a consequence of the nonoptimized contact formation process. This also results in higher source and drain resistances, which reduces the net drain current and transconductance. The device shows improved ON/OFF ratio at 200 °C for the same V_g, as indicated in Fig. 4(b) (solid red line), which is due to a threshold voltage (V_{th}) shift that can be attributed to mobile trapped charges in the gate oxide that get activated at higher temperatures. Contact linearity is improved at a high temperature most likely due to reduced thermionic emission barrier. The figures also show that there is a small change in dc I–V characteristics after SiN_x passivation.

Fig. 5(a) and (b) shows temperature-dependent I_d–V_g and g_m–V_g plots, respectively, at $V_{ds} = 5$ V, before passivation. The positive shift in V_{th} is evident again suggesting activation of trapped mobile charges in the gate oxide at higher temperatures. High-temperature gate bias stress confirmed the mobile nature of the traps. Such V_{th} shift was not observed in our previous study [49], suggesting the RIE damage as the probable cause. Further studies are necessary to understand the origin of these traps. A peak g_m of 6 mS/mm is obtained, which is a considerably lower value for designed device dimensions due to higher parasitic source and drain access resistances. S-parameter measurements show a very low f_t of <1 GHz at room temperature. As seen in the temperature-dependent V_{th} and peak g_m plots in Fig. 5(c) and (d), the passivation does not remove the V_{th} shift with temperature since it does not affect the trapped charges in the gate oxide. The peak value of g_m also remains largely unaffected after passivation.

B. Pulsed I–V Analysis

As described in Section I, the pulsed I–V analysis is important to study the dc to RF dispersion that arises from the dynamic response of traps with change in bias. We carried out drain turn-on (drain-lag) and gate turn-on (gate-lag) pulsing individually to isolate the effects of interface traps and buffer traps and localize the source of current dispersion.

Drain Turn-On: Buffer traps are shown to respond to the drain pulse in GaN devices [50], [51]. Recently, Fe diffusion from substrate to buffer has been identified as the source of dispersion in plasma-MBE grown Ga_2O_3 devices [45]. Fig. 6(a) shows the measured device response to drain turn-on pulse before passivation showing negligible dispersion in the I_d–V_d plots for different pulsewidths. Fig. 6(b) shows the drain current pulse, which does not show any delays in either transient edges, ruling out Fe-diffusion into the buffer.

The ozone MBE growth used in this study does not show any appreciable Fe diffusion, as shown in Fig. 3 in [52]. The same growth conditions are used in this study, and the fabrication flow does not involve high-temperature (>520 °C) processes. If both drain and gate are pulsed, we see a change in the device characteristics, as shown in Fig. 7. This is due to the gate lag effect caused by interface traps, which is discussed in Section III-C.

Gate Turn-On: Fig. 8(a) shows dc and gate pulsed I_d–V_d characteristics of the unpassivated device; we can clearly see severe dc-RF dispersion and knee-walk off.

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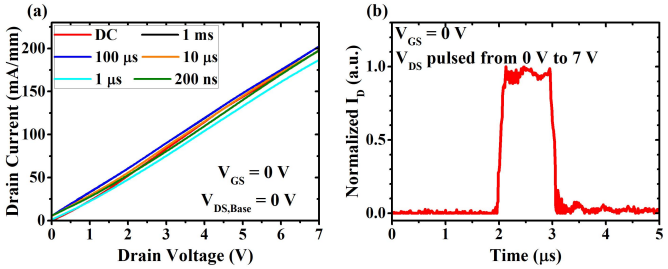

Fig. 6. (a) Drain turn-on I_d–V_d curves for various pulsewidths at $V_{gs} = 0$, showing negligible current dispersion compared to Fig. 8(b). (b) Drain turn-on pulse with pulse width of 1 μs, showing no trapping effects, which reduces the plausibility of bulk traps causing the current dispersion.

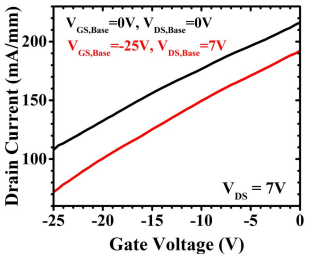

Fig. 7. Double-pulsed transfer curves using a 50-μs pulse width for both gate and drain voltage pulses using the quiescent bias conditions as indicated in the figure. The black curve represents minimum trapping and, hence, more drain current levels, while the red curve has reduced current due to trapping.

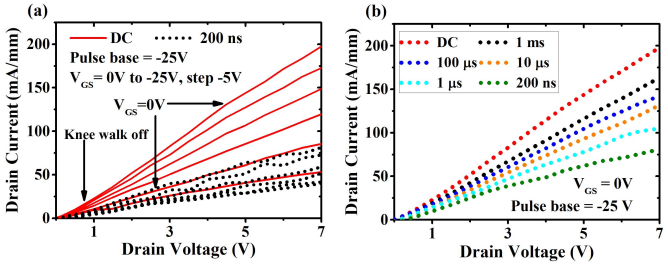

Fig. 8. (a) Drain current profiles for $V_g = 0$ V to $V_g = -25$ V for dc (red solid lines) and 200-ns pulse width (black dotted lines), before passivization. (b) Complete I_d–V_d profile from dc to 200-ns pulse width before passivation for $V_g = -0$ V shows clear dispersion in drain current with decreasing pulse width.

The current collapse during gate turn-on pulse could be related to both traps directly under the gate electrode and the traps in the gate to drain access region [51]. Fig. 8(b) shows I_d–V_d at a constant V_{gs} as a function of pulse width. The current collapse increases with decreasing pulsewidths. The dispersion is caused by interface traps under the gate and in the gate–drain access region.

Fig. 9(a) shows the temperature-dependent time-domain plot of the drain current response to a 1-ms gate turn-on pulse. At all temperatures, the drain current pulse shows a delayed asymptotic turn-on transient, which could be associated with emission time constants of electrons from the traps both in the gate–drain access region and the gate region. This pulse profile makes it self-explanatory as to why we see an increased current dispersion between static and pulsed I_d–V_d data with reduced pulsewidths. Similar behavior is seen during the

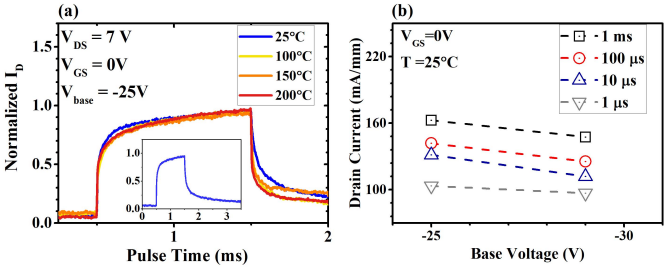

Fig. 9. (a) Temperature-dependent drain current pulse profile for a 1-ms gate turn-on pulse. Graph indicates how the traps response with temperature affects the drain current transient. Inset is room temperature plot for the same pulse width with extended turn-off transient, showing delayed effect due to capture time constants related to traps. (b) Change in maximum drain current recorded at $V_{gs} = 0$ V depending on the base voltage of the pulse for varying pulsewidths as indicated. A more negative base voltage assists more trapping and thus more current collapse.

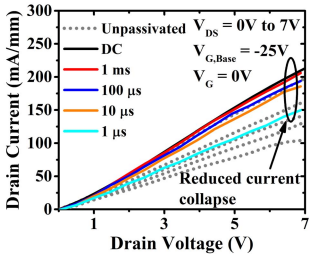

Fig. 10. Complete I_d–V_d profile from dc to 200-ns pulse width before (dotted gray lines) and after (solid lines) passivation for $V_g = -0$ V shows significant improvement in drain current dispersion down to 10-μs pulse width.

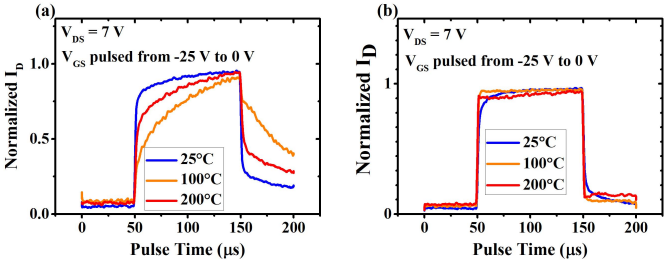

Fig. 11. Temperature-dependent drain current pulse profile for a 100-μs gate turn-on pulse before (a) and after (b) passivation.

turn-off transient edge of I_d pulse, which could be attributed to capture time constants of electrons by the interface traps. Increasing the temperature seems to increase the delay slightly. Inset of Fig. 9(a) shows extended turn-off transient for room temperature pulse to illustrate the slow capture process of electrons by traps after the gate voltage pulse returns to its base value. As shown in Fig. 9(b), the more negative the base voltage of the pulse, the greater the current collapse for the same pulse width. This is obvious since more negative base voltage would trigger more trapping of charges due to which the drain current takes a longer time to recover.

C. SiN_x Passivation

According to the reports in previous studies on AlGaN/GaN devices [50], [53]–[55], SiN_x passivation helps in mitigating dc-RF dispersion. We explore the effect of SiN_x passivated on RIE treated Ga_2O_3 devices.

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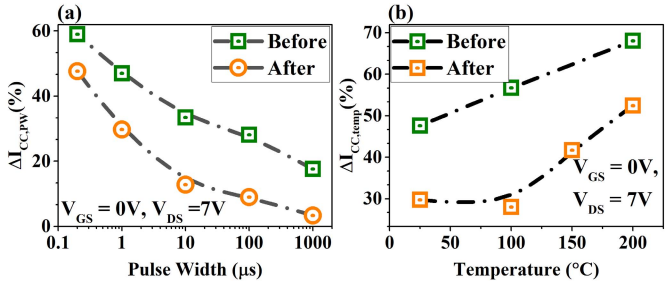

Fig. 12. (a) Percentage drain current collapse with respect to dc measurement as a function of pulsewidths before (green squares) and after (orange circles) passivation. (b) Percentage drain current collapse with respect to dc measurement as a function of temperature before (green squares) and after (orange circles) passivation.

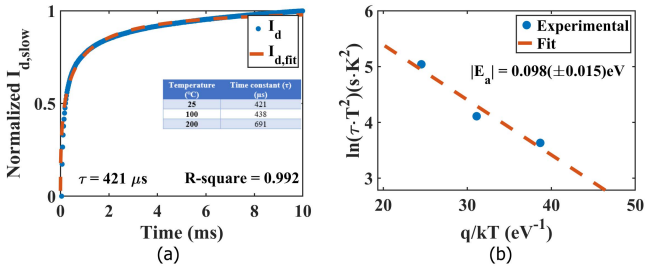

Fig. 13. (a) Normalized $I_{D,slow}$ and a stretched exponential fitted curve give a time constant $\tau = 421$ μs. (Inset) Time constant variation with temperature. (b) Arrhenius plot of q/kT versus $\ln(\tau \cdot T^2)$. The slope of the linear fitting line gives activation energy for the trap. A negative slope to the plot suggests multistep trapping and detrapping mechanism. The Arrhenius relation of the form $\tau \cdot T^2 \propto \exp(E_a/kT)$ was used for curve fitting.

Fig. 10 compares pulsed I–V plots of the device postpassivation with that of before passivation. We see a reduced dc-RF dispersion after passivation, especially the low-frequency dispersion is significantly reduced confirming that the role of traps in the gate–drain access region. While I_d–V_d data corresponding to 1 μs and 200-ns pulsewidths still show dispersion, they both show considerable improvement in I_d value over unpassivated device. The most likely reason for this dispersion is the traps under the gate which are still in play. The temperature-dependent drain current transients in Fig. 11 clearly show the reduction of low-frequency dispersion. Compared to the unpassivated drain current pulse, the passivated data are close to the ideal square wave pulse shape except for a very small delay at the end of the turn-on and turn-off transients, which is responsible for the current dispersion seen in shorter pulsewidths.

To get a more quantitative idea of the effect of passivation on current collapse, we have calculated percentage current collapse in relation to dc data as a function of temperature and pulse width using equations: 1) $\Delta I_{cc,PW} = (I_{d,dc} - I_{d,PW})/I_{d,dc}$ and 2) $\Delta I_{cc,temp} = (I_{d,dc} - I_{d,1\ \mu s})/I_{d,dc}$, where $I_{d,dc}$ is the static drain current value during the dc measurement, $I_{d,PW}$ is the drain current measured for one of the five pulsewidths, and $I_{d,1\mu s}$ is the drain current measured for 1-μs pulse. All the drain current values are measured at $V_{ds} = 7$ V and $V_{gs} = 0$ V. As can be seen in Fig. 12(a), the current collapse is almost entirely recovered for larger pulsewidths down to 10 μs with collapse ratios below 10%, whereas the smaller pulsewidths (1 μs and 200 ns) still show more than 30% current collapse. The temperature-dependent current collapse ratio for 1-μs pulse also shows average 20% improvement over unpassivated data. It is clear that the SiN_x is effective in passivation of low-frequency traps in the drain access regions. Further optimization of the passivation can completely eliminate the high-frequency dispersion.

D. Dynamics of Traps

The trapping and detrapping of electrons from the gate and gate–drain access regions and, hence, the time response can occur by two possible methods: 1) thermionic emission from the trap, and its rate is governed by the Shockley–Read–Hall (SRH) mechanism and/or 2) variable range hopping (VRH), as described in [33]. Assuming a discrete or narrowband of traps in terms of energy level, the time constant of the traps can be determined by curve fitting a stretched exponential function in (1) to the drain current transient, as shown in Fig. 13(a)

$$I_{d,\text{slow}} = 1 - \exp\left(\frac{-t}{\tau}\right)^{\beta} \tag{1}$$

where $I_{d,\text{slow}}$ is the normalized slow transient, τ is the time constant, and β is the fitting parameter. A slow time constant of 421 μs is obtained using the room temperature measurement data. As seen in the inset of Fig. 13, the time constant increases with temperature ruling out the SRH mechanism.

An alternative mechanism reported by Meneghesso *et al.* [33], where the VRH is the rate-limiting step, could explain the observed data. We use the Arrhenius equation fitting to q/kT versus $\ln(\tau T^2)$ plot, which gives a trap activation energy to be 0.098 eV $\pm$ 0.015 eV, as shown in Fig. 13(b). The trap level estimated from Fig. 13(b) corresponds to a relatively shallow trap, which aligns with VRH model. However, the observed negative slope is opposite of what is seen in a previous report on GaN transistors [33], [56] with VRH as the mechanism. There are several possibilities for the observed temperature dependence, including the increase in the trap density at higher temperatures, a multistate mechanism for electron emission and capture, and so on. A deeper understanding of all the processes in play is necessary to explain the complete model of trap dynamics with the help of further studies, such as DLTS.

Following the analysis in Section III-A–III-C, we discuss the likely origin of the dc-RF dispersion. RIE is known to introduce traps in Ga_2O_3 [57]; these traps along with surface traps on SiO_2 could provide a path for the VRH process to form a virtual gate in the gate–drain access region resulting in the dispersion. Passivation of the SiO_2 surface states breaks this path, thus reducing the low-frequency dc-RF dispersion. A comparison with other published results shows that similar dc-RF dispersion was seen in [42], which used RIE on the channel layer, while devices where the channel is not exposed to RIE [43], [44] show negligible dc-RF dispersion. There has been a report of RIE-induced channel depletion in Ga_2O_3 MESFETs [48].

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IV. Conclusion

We successfully fabricated a depletion mode Ga_2O_3 MOSFET with a 0.12-μm gate length with a drain current of 210 mA/mm and low g_m of 6 mS/mm. The low g_m is attributed to high source resistance. The pulsed I–V analysis shows dc-RF dispersion with a peak current collapse ratio of 60% for 200-ns gate turn-on pulse on unpassivated devices. A large trap time constant of 421 μs was obtained at room temperature for an unpassivated device from stretched exponential curve fitting to the measured drain current pulse. The trap time constant increases to 510 μs at 200 °C. SiN_x passivation shows a significant decrease in the current collapse. While the low-frequency dispersion is eliminated, the high-frequency dispersion was present likely due to the traps under the gate.

From the Arrhenius plot, a trap activation energy of 98 meV is calculated. The low activation energy and high time constant suggest a VRH transport as a likely mechanism for trapping and detrapping. However, an increasing time constant with increasing temperature is observed, which is unlike previous studies in GaN devices. A more complex process such as a multistep trapping and detrapping process could be at play, which requires further studies. We hypothesize that the RIE damage is responsible for acceptor-like traps in the drain access region, which provides the path for the said process and helps in the virtual gate formation leading to the current collapse. We also showed that the current dispersion can be mitigated, to some degree, by using a thick passivation layer of a silicon nitride. Trapped mobile charges in the oxide were responsible for the temperature-dependent threshold voltage shift observed in both unpassivated and passivated devices.

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