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Exploring the practical efficiency limit of silicon solar cells using thin solar-grade substrates

A. Augusto, *[a] J. Karas,[b] P. Balaji,[b] S. G. Bowden[a] and R. R. King[a]

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Multiple silicon solar cell technologies have surpassed or are close to surpassing 26% efficiency. Dielectric and amorphous silicon-based passivation layers combined with minimal metal/silicon contact areas were responsible for reducing the surface saturation current density below 3 fA cm^{-2}. At open-circuit, in passivated contact solar cells, the recombination is mainly from fundamental mechanisms (Auger and radiative) representing over 3/4 of the total recombination. At the maximum power point, the fundamental recombination fraction can drop to half, as surface and bulk Shockley–Read–Hall step in. As a result, to further increase the performance at the operating point, it is paramount to reduce the bulk dependence and secure proper surface passivation. Bulk recombination can be mitigated either by reducing bulk defect density or by reducing the wafer thickness. We demonstrate that for commercially-viable solar-grade silicon, thinner wafers and surface saturation current densities below 1 fA cm^{-2}, are required to significantly increase the practical efficiency limit of solar cells up to 0.6% absolute. For a high-quality n-type bulk silicon minority-carrier lifetime of 10 ms, the optimum wafer thickness range is 40–60 μm, a very different value from 110 μm previously calculated assuming undoped substrates and solely Auger and radiative recombination. In this thickness range surface saturation current densities near 0.1 fA cm^{-2} are required to narrow the gap towards the fundamental efficiency limit. We experimentally demonstrate surface saturation currents below 0.5 fA cm^{-2} on pi/CZ/in structures across different wafer thicknesses (35–170 μm), with potential to reach open-circuit voltages close to 770 mV and bandgap-voltage offsets near 350 mV. Finally, we use the bandgap-voltage offset as a metric to compare the quality of champion experimental solar cells in the literature, for the most commercially-relevant photovoltaic cell absorbers and architectures.

1. Introduction

In the last few years silicon-based solar cells have accomplished several important milestones. Efficiencies over 26% were reported for two different cell architectures,[1,2] open-circuit voltages, V_{OC}, over 760 mV were experimentally demonstrated,[3] and bandgap-voltage offsets at open-circuit, W_{OC}, for silicon are now comparable to high-performance direct-bandgap materials.[4] These remarkable achievements were possible due to outstanding surface passivation properties of passivated-contact solar cells. Saturation current densities from the surface component of recombination, J_{0S},[5] below 3 fA cm^{-3} enabled fill-factors, FF, above 83% and V_{OC} over 740 mV.[1] The V_{OC} is primarily shaped by bulk Auger and surface recombination. As we approach the lower minority-carrier injection levels near the maximum power point (MPP) as opposed to open-circuit conditions, surface and bulk Shockley–Read–Hall (SRH) recombination become increasingly important.[6] The theoretical efficiency limit of silicon solar cells is calculated considering the fundamental recombination mechanisms (Auger and radiative in the bulk)[7,8] and Lambertian light trapping limits.[9] A recent assessment[8] indicates the ideal cell should be manufactured on undoped 110 μm-thick Si wafers, giving a calculated maximum efficiency of 29.43%. The highest measured efficiency for a silicon solar cell to date is 26.7%,[1,10] and previous work by this group[11] identifies 27.1% as the practical efficiency limit for their current silicon heterojunction – interdigitated back contact (SHJ-IBC) technology. These calculations assume a 165 μm-thick bulk wafer with 3 Ω cm resistivity (1.549 × 10^{15} cm^{-3} n-type doping concentration), extrinsic minority-carrier lifetime (from surface and bulk SRH) close to 11 ms, and a J_{0S} of 0.9 fA cm^{-2}. The efficiency limit assuming only fundamental recombination mechanisms for those cells was estimated to be 29.1%. The gap between the fundamental and the practical efficiency limit is due to resistive, optical and non-fundamental recombination losses. Together, the surface and bulk SRH recombination represent 35% of the total losses. The bulk SRH contribution to the losses can be mitigated either by improving the bulk quality or by reducing wafer thickness.

[a]School of Electrical, Computer and Energy Engineering, Arizona State University, Tempe, Arizona, 85281, USA. E-mail: augusto@asu.edu
[b]School for Engineering of Matter, Transport and Energy, Arizona State University, Tempe, Arizona, 85281, USA

The open-circuit voltage of a solar cell is largely defined by the total recombination rate in the cell and by its bandgap. The V_{OC} varies greatly across different photovoltaic materials as their energy bandgaps change. The W_{OC} is a valuable metric to compare the quality of experimental solar cells manufactured from different absorber materials because it removes much of the bandgap dependence.[4] The W_{OC} is defined as:

$$W_{OC} \equiv \frac{E_g}{q} - V_{OC} \quad (1)$$

where E_g is the energy bandgap and q the elementary charge. The lower the value of W_{OC}, the lower the recombination and the better the device. The current record silicon solar cell[1] has a W_{OC} of 383 mV, assuming a bandgap of 1.121 eV, according with eqn (1) The best W_{OC} reported at one sun (0.100 W cm^{-2}) was measured on a thin gallium arsenide (GaAs) solar cell with a rear reflector for photon recycling,[10] with a W_{OC} of 293 mV, assuming a bandgap of 1.42 eV. In order to decrease further the W_{OC} it is necessary to reduce the overall recombination in the solar cell. Thinner wafers are attractive because they have the potential to decrease the cost while improving the performance of solar cells.[6,12,13] In a recent technoeconomic study on thin silicon,[14] the authors predict that 50 μm-thick wafers could potentially reduce manufacturing capex (capital expenditure) by 48%, module cost by 28%, and LCOE (levelized cost of electricity) by 24%. Solar cells formed from thinner wafers are more bulk-defect tolerant but are controlled much more by surface recombination.[6] The present state-of-the-art for surface passivation may not presently be sufficient to narrow the gap between practical cells and the intrinsic efficiency limit. Nevertheless, recent results accomplished in passivated contact solar cells with very low surface saturation currents show a path to future improvements.

In this work, we study how the wafer thickness combined with different surface passivation conditions impacts the performance of solar cells manufactured on commercially-relevant, long-lifetime silicon wafers. We quantify the contribution of each recombination mechanism to determine the voltages at open-circuit and maximum-power injection levels. These results help to understand the limits on different solar cell architectures placed by surface passivation capability.

2. Surface passivation driving performance: a brief history

Superb surface passivation is the foundation of +20% efficiency silicon solar cells. In the 1980's teams in University of New South Wales (UNSW), Stanford University and Sanyo were developing the groundwork for today's passivated contact solar cells.[15]

The UNSW team developed the Passivated Emitter and Rear Cell (PERC) family by combining the superior passivation advantages of SiO_2,[16] later generalized to other dielectrics such as silicon nitride (Si_3N_4) and aluminum oxide (Al_2O_3) and minimal contact surface between the metal and silicon. In this solar cell family, the Passivated Emitter Solar Cell (PESC)[17] was introduced first, followed by the Passivated Emitter and Rear Cell (PERC) and finally the Passivated Emitter Rear Locally-diffused (PERL) solar cell.[18,19] In the PESC the emitter was passivated with SiO_2 while retaining a full-coverage Al back-surface field (BSF) on the rear, attaining a V_{OC} of 669 mV. With the PERC design, the passivating oxide was used on the rear, and the V_{OC} increased by 30 mV. Finally, with the PERL design local doping was introduced reducing recombination at the metal-contacted regions on the back, and the metal/silicon surface area was further reduced. With the PERL, UNSW accomplished 25% conversion efficiency and V_{OC} of 706 mV.[20] The total saturation current density (J_0) of the record device was 50 fA cm^{-2}, of which 15 fA cm^{-2} was due to the emitter. In commercial PERC cells with 20–22% efficiency the saturation currents are much higher. The total J_0 (emitter, metal contacts and rear surface) is on the order of 300 fA cm^{-2},[18] the saturation current density due to the emitter J_{0e} is below 90 fA cm^{-2},[19,21] and the J_{0S} at passivated areas is close to 10 fA cm^{-2}.[21] Efficiencies over 23% on PERC cells have been reported by large manufacturers,[22,23] and emitters with saturation current densities below 35 fA cm^{-2} were demonstrated with potential for commercial viability.[24]

At Stanford University a solar cell research team developed an architecture in which the emitter and all the metal contacts were placed on the rear of the cell, the point-contact solar cell (PCSC).[25,26] This structure was the predecessor of the commercial large-area interdigitated back-contact (IBC) cells developed and manufactured by SunPower.[27] SunPower solar cells together with silicon heterojunction (SHJ) cells from Panasonic,[28] Kaneka,[1] and Hanergy[29] are the only architectures to demonstrate efficiencies >25% for commercial-size solar cells. The IBC architecture presents obvious advantages both in generation and surface passivation. By removing the metal contacts and the emitter from the front of the cell, the active area is increased, the blue response improves, and the surface passivation benefits from the lack of high recombination metal/silicon contact area. As a result the Stanford team was able to demonstrate open-circuit voltages over 700 mV from a very early date.[30,31]

In the Sanyo (later Panasonic) approach, the emitter is not diffused but deposited as an amorphous silicon (a-Si) layer on top of crystalline silicon (c-Si), forming a silicon heterojunction.[32–34] The cell architecture is referred to as a Heterojunction with Intrinsic Thin-layer (HIT) cell, or more generally, as a silicon heterojunction (SHJ) cell. The wide-bandgap a-Si layer suppresses the minority-carrier concentration at the metal or transparent conductive oxide (TCO) contacts, which are highly recombination-active regions compared to the absorber.[34] A major breakthrough came with the introduction of a thin, wide-bandgap buffer layer of intrinsic (undoped) amorphous silicon separating the doped a-Si emitter from the c-Si wafer, dramatically reducing the minority-hole concentration at the highly defective interface with amorphous silicon.[35] As a result J_{0S} below 1 fA cm^{-2} (ref. 3 and 11) and voltages over 760 mV (implying a J_{0S} close to 0.1 fA cm^{-2}) on 50 μm-thick structures[3] are possible, leading to W_{OC} values of 0.35 V, close to those in direct bandgap solar cells like GaAs or GaInP. The SHJ structure has demonstrated efficiencies close to 27% (ref. 1) over large-area solar cells (>179 cm^2) and is particularly suitable for producing high-efficiency solar cells on thin wafers. The relatively large W_{OC} of the record silicon cell (>0.360 V) indicates that there is still room for further improvements.

The Stanford team also developed another powerful approach for passivated contacts in which carriers tunnel through a very thin silicon oxide layer to doped polycrystalline silicon, termed SIPOS (semi-insulating polycrystalline silicon: SiO_x, with $x > 2$), forming a carrier selective contact with very low surface recombination.[36–38] More recently teams in ISFH and Fraunhofer ISE have revived and further developed a similar selective contact structure using thin oxides[39] and doped polycrystalline silicon films. These structures have demonstrated surface passivation capabilities comparable with SHJ solar cells ($J_{0S} < 2$ fA cm^{-2}), and efficiencies close to and over 26%. These efficiencies have so far been demonstrated for cells with areas of about 4 cm^2. Two distinguished examples are the IBC-POLO (polycrystalline silicon on oxide)[2] developed ISFH and the TOPCon (tunnel oxide passivated contact)[40] developed by Fraunhofer ISE.

3. Sample preparation

Silicon heterostructures were used as a testbed to measure lifetimes on samples with varying thickness and comparable J_{0S} values. The samples were prepared on 239 cm^2 commercial-grade n-type silicon Czochralski (CZ) wafers with 3–4.5 Ω cm resistivity (1.55×10^{15} to 1×10^{15} cm^{-3} n-type dopant concentration), ⟨100⟩ orientation, and initial thickness of 200 μm. The wafers were thinned down to different thicknesses (35–170 μm) and textured using alkaline chemical etching. The chemical thinning process was previously demonstrated to have produced high efficiency solar cells with good mechanical properties.[41,42] After chemical cleaning, we deposited the intrinsic and doped hydrogenated amorphous silicon layers (a-Si:H) *via* Plasma Enhanced Chemical Vapor Deposition (PECVD), forming the p/i/n-CZ/i/n stack. The PECVD setup has a parallel plate configuration, where the gases used in the deposition were silane and hydrogen, paired with phosphine for n-type films and trimethylboron for p-type films. The thicknesses of the individual a-Si:H layers are between 6–8 nm. Plasma hydrogenation[43] is used during PECVD to improve chemical passivation in the interface by dangling bond saturation, reducing the density of defects at the crystalline silicon surface.[44] Effective minority-carrier lifetimes, implied V_{OC} and J_{0S} values were obtained for 25 °C using the Sinton Instruments WCT-120 lifetime tester using quasi-steady-state photoconductance decay (QSSPC).[45] The J_{0S} values were determined assuming the radiative[46] and Auger recombination parametrization of Richter *et al.*,[47] and extracted using the method of Kane and Swanson.[48] The accuracy of the QSSPC measurement and details on the Richter parameterization are addressed in the Appendix section.

4. Discussion and results

4.1. Background – recombination kinetics

To study how the surface and substrate thickness impact the performance of the solar cell we break the effective minority-carrier lifetime, τ_{eff}, into its component recombination mechanisms. The Auger and radiative recombination mechanisms which take place in the bulk were calculated using Richter parametrization,[47] which includes the Schenk bandgap narrowing model[49] and injection-dependent radiative recombination.[50] Bulk SRH recombination was calculated using a standard SRH model with symmetric recombination parameters for electrons and holes and a single trap state in the middle of the bandgap. The surface recombination (also a SRH recombination mechanism) is calculated using the J_{0S} model proposed by McIntosh *et al.*[5]

In Fig. 1 we model the τ_{eff} for two structures with the same bulk and surface characteristics, *i.e.*, the same SRH bulk lifetime, $\tau_{b,SRH}$, and J_{0S}. The structures have different wafer thicknesses, w, of 170 μm and 40 μm.

The effect of surface recombination on the bulk-normalized total recombination rate, $R_{rec} \equiv \Delta n/\tau_{eff}$ in units of cm^{-3} s^{-1}, varies inversely with the substrate thickness, as described in:

$$\frac{\Delta n}{\tau_{eff}} = \frac{\Delta n}{\tau_{b,SRH}} + \frac{2S\Delta n}{w} + \frac{\Delta n}{\tau_{fund}} \quad (2)$$

where S is the surface recombination velocity, Δn is the excess electron density, which is equal to the excess hole density Δp. To account for bandgap narrowing at higher dopant concentrations or photogenerated carrier concentrations, we use the empirical expression from Richter *et al.*,[47] see Appendix section. Note that τ_{fund}, where the subscript denotes fundamental recombination mechanisms (radiative and Auger), is the same as τ_{int} in Richter *et al.*, where these mechanisms are referred to as intrinsic recombination.

As a result of the dependence of total recombination rate R_{rec} on substrate thickness, described by eqn (2), the structure with a thickness of 40 μm thickness shows higher effect of surface recombination on the total recombination rate (lower $\tau_{surf} \equiv w/2s$) than the one with 170 μm. The impact of the surface is mainly observed at the maximum power point injection level, where the fundamental recombination fraction (Auger and radiative), represented by the color bar in Fig. 1, becomes less dominant. At

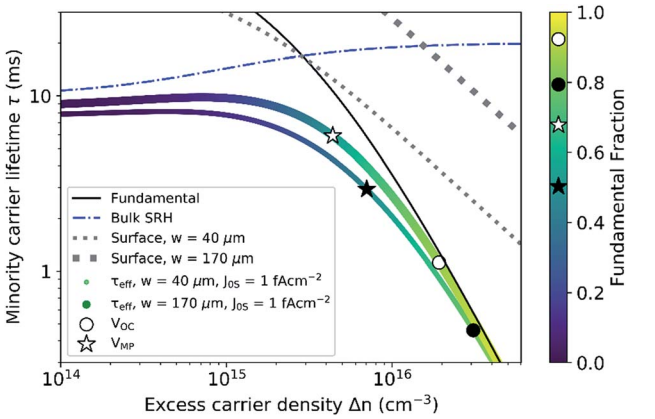

Fig. 1 Effective minority-carrier lifetime model of structures on 170 μm and 40 μm-thick n-type wafers with bulk SRH lifetime of 10 ms and bulk resistivity of 3.55 Ω cm (1.3×10^{15} cm^{-3} dopant concentration), and total J_{0S} (from both surfaces) of 1 fA cm^{-2}. Each curve on the plot corresponds to a different recombination mechanism. The color bar represents the fraction of fundamental (Auger + radiative) recombination. The generation current was defined by the Lambertian light trapping limit for each thickness. The markers in the color bar indicate the fundamental recombination fraction at maximum power and open-circuit injections.

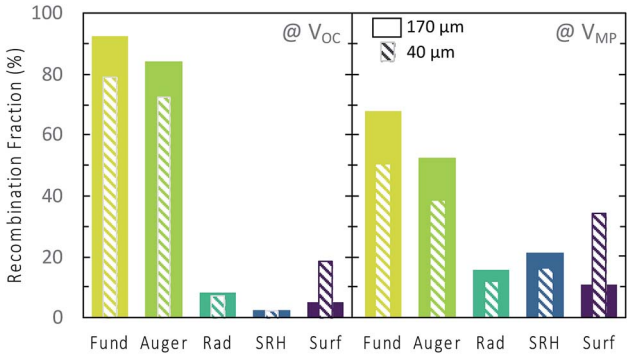

Fig. 2 Recombination fraction details for each recombination mechanism at V_{OC} and V_{MP} for 40 μm and 170 μm-thick samples.

open-circuit (V_{OC}), the fundamental recombination fraction is over 90% for the thicker wafer and close to 80% for the thinner one. In contrast, at maximum power voltage (V_{MP}), surface and bulk SRH recombination have considerably higher impact, reducing the overall fundamental fraction to near 60% for the thicker cell and 50% for the thinner one, as shown in Fig. 2.

In a semiconductor under steady-state illumination, the photogenerated current density J_{ph} minus the recombination current density, J_{rec}, of electron–hole pairs is balanced with any current density J being extracted (for instance through the terminals of a solar cell): $(J_{ph} - J_{rec}) = J$ and the photogenerated excess hole and electron concentrations are balanced as well, $\Delta p = \Delta n$. As a result, for a sample of thickness w we can write J_{rec} and J_{ph} as functions of the effective minority-carrier lifetime and the excess minority-carrier density:[45]

$$J_{rec} = (J_{ph} - J) = \frac{qw\Delta n}{\tau_{eff}} \quad (3)$$

The voltage in a solar cell in general depends on the product of electron, n, and hole, p, concentrations and can be written as:

$$V = \frac{kT}{q} \ln\left(\frac{np}{{n_i}^2}\right) = \frac{kT}{q} \ln\left(\frac{(n_0 + \Delta n)(p_0 + \Delta p)}{{n_i}^2}\right) \quad (4)$$

where n_i is the intrinsic carrier concentration, k the Boltzmann constant, and T is the temperature. For a solar cell under steady-state illumination and manufactured on n-type wafers with a dopant density N_D, the voltage can be written as:

$$V = \frac{kT}{q} \ln\left(\frac{\Delta n(N_D + \Delta n)}{{n_i}^2}\right) \quad (5)$$

For high doping densities, or high-injection conditions, where $\Delta n \gg N_D$, the intrinsic carrier concentration n_i can be replaced by the effective intrinsic carrier concentration, $n_{i,eff}$, to include the effect of bandgap narrowing, ΔE_g:[49]

$${n_{i,eff}}^2 = {n_i}^2 e^{\frac{\Delta E_g}{kT}} \quad (6)$$

Eqn (5) can then be rewritten as function of wafer thickness and effective minority-carrier lifetime by applying eqn (3):

$$V = \frac{kT}{q} \ln\left(\frac{(J_{ph} - J)\tau_{eff}\,(N_D + \Delta n)}{qw{n_{i,eff}}^2}\right) \quad (7)$$

In the high-injection (hi) regime, eqn (7) can be simplified further, becoming independent of the base doping:

$$V_{hi} = \frac{kT}{q} \ln\left(\frac{(J_{ph} - J)\tau_{eff}\,\Delta n}{qw{n_{i,eff}}^2}\right) \quad (8)$$

The current density–voltage (J–V) curve is calculated using eqn (2) and (3), as a function of voltage:[51]

$$J(V) = J_{ph}(V) - J_{rec}(V) = J_{ph}(V) - qwR_{rec}(V) \quad (9)$$

The J_{ph} was determined assuming the Lambertian light-trapping limit described by Green,[52] which increases the mean path-length for a light ray inside the cell of $4{n_r}^2\,w$, where n_r is the refractive index of silicon. The AM1.5G spectrum at 25 °C is assumed and normalized to an illumination intensity of 0.100 W cm^{-2}. Note that J_{ph} also depends on the voltage *via* free carrier absorption, but weakly.[51]

4.2. Experimental results and analysis

Thin solar cells can only perform closer to the fundamental limit if the J_{0S} decreases dramatically from the present state of the art. In Fig. 3 we show how efficiency varies with J_{0S} and cell thickness, and how bulk SRH impacts the performance. The bulk parameters were chosen to be representative of a high-performance material that is economically competitive for the industry, *i.e.*, Czochralski (CZ) n-type silicon with SRH bulk lifetime of 10 ms. We also consider high quality p-type material. The best efficiencies reported for p-type solar cells[2] were on float zone (FZ) silicon with bulk lifetimes over 3 ms. Standard p-type CZ wafers have bulk lifetimes in the 200–500 μs, in contrast with FZ material having typical lifetimes in the range of 2–5 ms. Through a hydrogenation process, substantial increases in the bulk minority carrier lifetime are observed for commercial-grade p-doped CZ wafers from 200–500 μs to over 1 ms. However, the passivation is reversible, and the passivated defects can be reactivated during the cell processing.[53] FZ silicon is not economically viable for large scale deployment in low-cost photovoltaics manufacturing. As a result, we consider an optimistic scenario for p-type CZ Si wafers with 1 ms SRH bulk lifetime. The dashed lines represent the case where the bulk SRH bulk lifetime is not considered (SRH bulk recombination assumed to be zero). If bulk SRH is not considered, the optimum thickness for the highest efficiencies near 29% is 100–110 μm. These thicknesses are close to the ones estimated for the fundamental limit considering only the fundamental mechanisms of Auger and radiative recombination.[7,8] However, if we take into account the typical bulk SRH lifetime of a commercially available high-performance n-type wafer, the optimum thickness range is much thinner, between 40 to 60 μm.

The experimental data in Fig. 4–6 are the implied values extracted from effective minority carrier lifetime measurements of

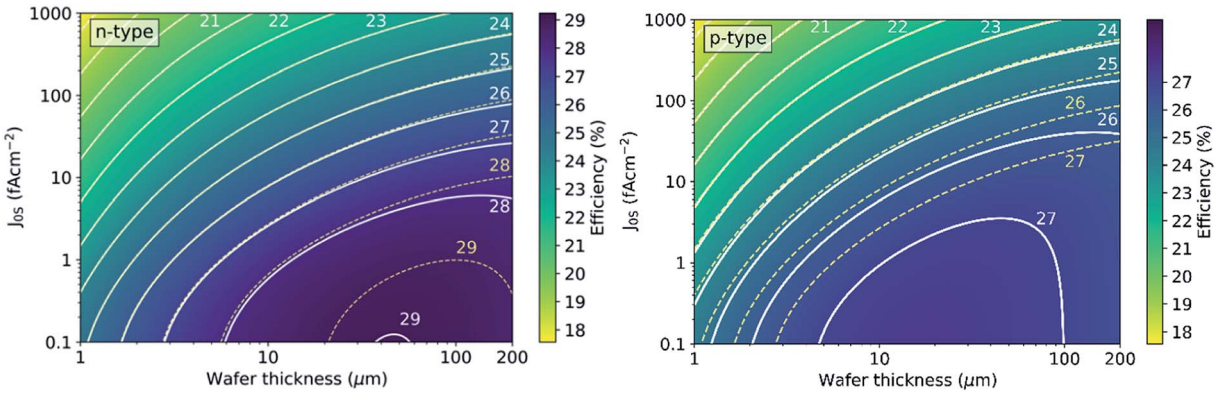

Fig. 3 Conversion efficiency of (left) n-type Si solar cells with bulk SRH lifetime of 10 ms and of (right) p-type Si solar cells with SRH bulk lifetime of 1 ms, as functions of wafer thickness and J_{0S}. The dashed lines take into account only surface recombination, and Auger and radiative recombination in the bulk. The solid lines (and the color map) take into account all recombination mechanisms, including bulk SRH lifetime. For the n-type solar cell the optimum thickness is 100 to 110 μm when bulk SRH is disregarded and 40 to 60 μm when it is considered, for the highest efficiencies. For the p-type solar cells, wafer thicknesses below 100 μm are required to achieve efficiencies over 27%. The efficiency was calculated using the *J*–*V* relationship described by eqn (9). The generation current is defined by the Lambertian light-trapping limit for each thickness, assuming the AM1.5G spectrum at 25 °C and normalized to an illumination intensity of 0.100 W cm^{-2}.

p/i/n-Cz/i/n heterostructures grown on wafers with different thicknesses (35–170 μm), with bulk SRH lifetimes of 2–10 ms, and different intrinsic a-Si:H layers. The white markers represent samples with baseline passivation capabilities comparable with the state-of-the-art passivated-contact solar cells with total J_{0S} (contribution from both surfaces) between 1–5 fA cm^{-2}.[2,11,40] The red markers represent samples with an improved intrinsic a-Si:H passivation layer recently developed in-house with total J_{0S} < 0.5 fA cm^{-2} across multiple wafers thicknesses. The new intrinsic a-Si:H was developed using thin wafers as testbed in order to increase the response to improved surface passivation and by varying temperature and silane dilution ratios during the PECVD. Further details can be found in ref. 54. In both types of intrinsic a-Si:H the layer is 6–7 nm thick. In the past, using the baseline recipe, we achieved J_{0S} close to 0.1 fA cm^{-2} by applying an intrinsic a-Si:H bi-layer with a combined thickness of 15 nm, leading to implied V_{OC} over 760 mV on 50 μm samples.[3] With the new recipe we achieve implied V_{OC} of 770 mV using an intrinsic layer that is at least 2 times thinner (6 nm) on 40 μm-thick substrates.

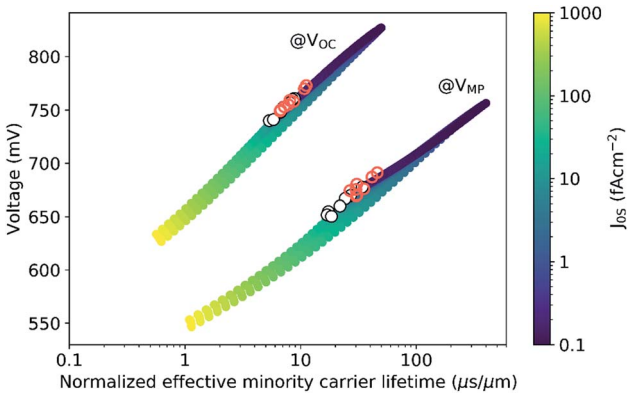

Fig. 4 The V_{OC} and V_{MP} as functions of the effective minority-carrier lifetime normalized by the wafer thickness for passivated samples with different J_{0S}. The simulation assumed wafers with thicknesses between 1 and 200 μm and J_{0S} between 0.1 and 1000 fA cm^{-2}. The voltages were calculated using eqn (7). The wafer thicknesses of the experimental samples are between 35–170 μm.

In Fig. 4 we demonstrate how voltages at open-circuit and maximum power, vary with τ_{eff} when normalized with the wafer thickness (τ_{eff}/w). The logarithmic dependence was not a surprise considering eqn (7) and (8). The color bar in Fig. 4 shows the J_{0S} values assumed in the model and the markers are experimental data, as previously described, from lifetime measurements on p/i/n-CZ/i/n samples with different wafer thicknesses and different intrinsic a-Si:H layers. For higher J_{0S} there is no benefit to thin the wafers further, as the surface "leakage" (controlled by the surface passivation quality) is significantly larger than the bulk recombination that can be reduced in thinner wafers. This can be seen in Fig. 4 where only cases with total J_{0S} <10 fA cm^{-2} can reach V_{OC} over 750 mV. Additional lower J_{0S} values show wider dispersion of voltages values (for instance purple region in Fig. 4 is more dispersed than yellow values), indicating that they are more responsive to wafer thickness. That is why certain solar cell technologies do not show a significant gain in voltage for thinner wafers, since their surface recombination is too high to benefit from the reduced bulk recombination with reduced thickness.

The experimental values show less variation from predicted performance at open-circuit than at maximum power. There are several different possible explanations for this behavior. First, in accordance with eqn (8) in high injection, voltage is independent of the doping concentration N_D. The carrier concentration at V_{OC} is at least 10 times higher than the doping concentration in these samples. At V_{MP} the carrier concentration is very close to the samples doping carrier concentration, so variations in N_D are able to cause variations in V_{MP}. The doping concentration assumed in the model is 1.3 × 10^{15} cm^{-3} and our samples have doping concentration that range from 1 × 10^{15} to 1.55 × 10^{15} cm^{-3}. Second, in accordance with Fig. 1 and 2 at maximum power injection, voltage is

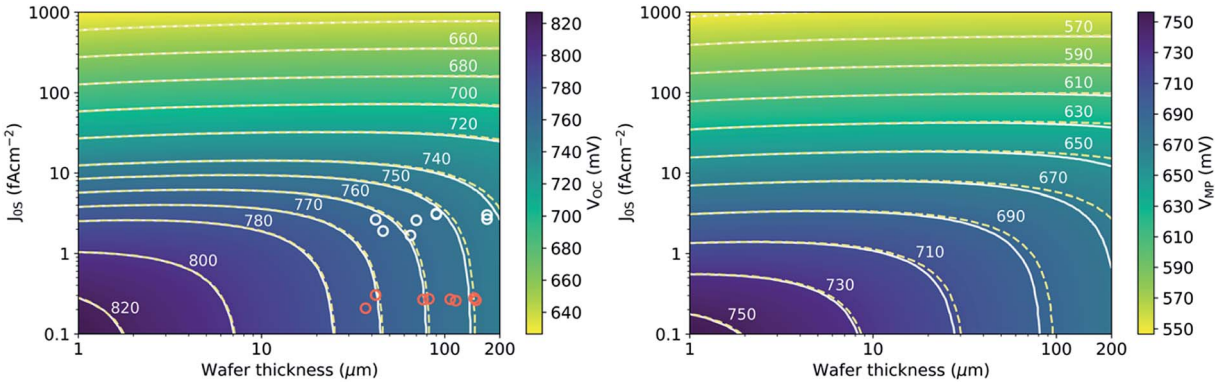

Fig. 5 Voltages at (left) open-circuit and (right) maximum power as function of the wafer thickness and J_{0S} for the n-type wafer represented. The solid lines (and the color map) represent voltages calculated considering bulk SRH recombination and the adjacent dashed lines represent the same voltage but disregarding the bulk SRH recombination. In the voltage calculations the generation current is defined by the Lambertian light trapping limit for each thickness.

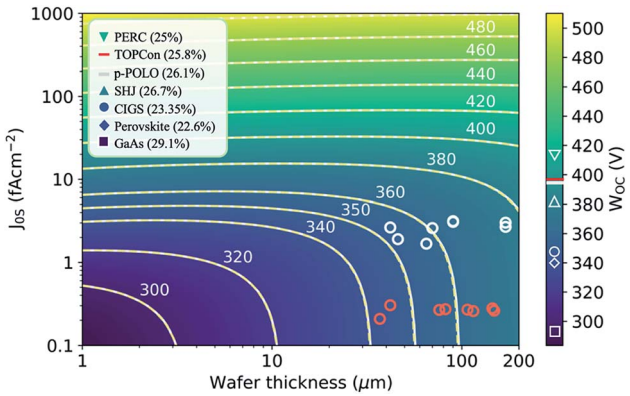

Fig. 6 Bandgap-voltage offset at open-circuit (W_{OC}) as a function of wafer thickness and J_{0S} for the same n-type wafer specifications represented in Fig. 3. The wafer thicknesses of the experimental samples are between 35–170 μm. The W_{OC} of the samples were calculated using eqn (10) and the measured effective lifetimes at open-circuit carrier concentrations. The W_{OC} of the top performing cells for different absorbers were estimated using eqn (1).

significantly more sensitive to bulk SRH lifetime than at open circuit, so that variation in bulk SRH lifetime results in significant variation in voltage. In our ingots we have measured bulk lifetimes in n-type CZ wafers from 2–10 ms, depending the ingot region. At V_{OC}, most of the recombination is governed by Auger and surface contributions, and the effect of bulk SRH is minimal. As a result, the V_{OC} variation within samples with the same thickness, and between the modeled and the actual implied V_{OC} (i-V_{OC}) is small.

In Fig. 5 we show how J_{0S} and wafer thickness impacts the voltages of the cell at open-circuit and maximum power. The impact of the bulk SRH and J_{0S} in Fig. 5 is translated by the gap between the solid lines, where voltage is calculated considering bulk SRH, and the adjacent dashed lines, that represent the same voltage value but now calculated disregarding the bulk SRH recombination. The bulk SRH recombination (seen through the dependence on wafer thickness) has a significant impact at maximum power for $J_{0S} < 10$ fA cm^{-2}, and little role at open-circuit. This result was expected according with Fig. 1 and 2, where the recombination is mostly fundamental at V_{OC}, due to the cubic dependence of Auger recombination rate on excess carrier concentration.

In high-efficiency solar cells W_{OC} values are typically below 400 mV.[4] As mentioned earlier, the best reported W_{OC} value is 293 mV for thin GaAs, and the present record efficiency silicon solar cell has an estimated W_{OC} of 383 mV. To further reduce the gap between silicon solar cells and direct bandgap solar cells we need to increase voltage by reducing the total recombination rate and the thickness of the wafer. In Fig. 6 we show how W_{OC} changes for varying Si wafer thickness and varying J_{0S}. The W_{OC} in high-level injection can be expressed as:

$$W_{OC} = \frac{kT}{q} \ln\left(\frac{qwN_V N_C}{J_{ph}\tau_{eff}\,\Delta n}\right) \quad (10)$$

as derived in ref. 3, for long τ_{eff} where Δn is approximately constant across the wafer, and accounting for bandgap narrowing ΔE_g, where N_V and N_C are the effective densities of states in the valence band and the conduction band respectively. In eqn (10) as in eqn (2) and (3), the dependence on wafer thickness, w, is explicitly expressed, and the recombination rate is described by the effective minority carrier lifetime τ_{eff}. This expression is used to calculate the W_{OC} of our experimental samples using the lifetime parameters at V_{OC} level injection. In Fig. 6, we display the W_{OC} of our experimental samples and the W_{OC} of the top performing cells[9] for different absorbers and for different silicon solar cells technologies. The W_{OC} of the top performing cells were estimated using eqn (1), assuming a bandgap of 1.42 eV for GaAs, 1.08 eV for copper indium gallium selenide (CIGS)[55] and 1.121 eV for crystalline silicon. The top reported efficiency for perovskite solar cells is over 25%.[56] There is limited information describing the stability, composition and bandgap of this solar cell. Perovskite solar cells include absorbers with a wide range of chemistry compositions, and the methods used to calculate the bandgap produce often different results.[57] In Fig. 6, we report an exemplary recent perovskite with a well-characterized bandgap (1.53 eV) and a certified stabilized efficiency of 22.6% (initially 23.4%), and one of the lowest W_{OC} reported for a perovskite to date (340 mV), to

our knowledge.[58] The W_{OC} for the record cadmium telluride (CdTe) solar cell (22.1%)[9] is not displayed in Fig. 6 because is over 580 mV, assuming a bandgap of 1.47 eV.[59] When we compare different silicon solar cells technologies, is clear that the passivation of the metal contacts is critical to accomplish W_{OC} below the 400 mV threshold. In the PERC structure, the metal contacts passivation scheme is insufficient, limiting the V_{OC}, and subsequently the W_{OC} and efficiency in this type of devices.

In Table 1 we summarize the parameters derived from the lifetime measurements of the p/i/n-Cz/i/n samples, including the experimental data of Fig. 5 and 6. As previously discussed, and in accordance with Fig. 1 and 2 and eqn (7) and (8), measurements at maximum power injection are significantly more sensitive to bulk SRH lifetime and doping concentration (N_D) than measurements at open circuit. Variations in the bulk SRH lifetime and doping concentration between samples will result in significant variation in V_{MP} and efficiency. At open-circuit injection levels, most of the recombination is governed by Auger and surface, and the effects of the bulk SRH lifetime and doping concentration are minimal. As a result, the differences between the V_{OC} and W_{OC} modeled in Fig. 5 and 6, and the values in Table 1 are smaller. That is not necessarily the case in Fig. 3. For instance, if we take the 42 μm-thick samples in Table 1, and assume a doping concentration of 1.3×10^{15} cm^{-3} and bulk SRH lifetimes between 2 ms and 10 ms, the result is V_{OC} of 762 ± 1 mV and efficiency 27.7 ± 0.3% for the baseline case, and V_{OC} of 772 ± 1 mV and efficiency 28.3 ± 0.4% for the optimized case.

The baseline samples have similar passivation capabilities to the state-of-the-art silicon heterojunction structures, *i.e.*, J_{0S} = 1–5 fA cm^{-2},.[11] In the samples with improved intrinsic a-Si:H layers, the J_{0S} drops to values ~10 times lower leading to i-V_{OC} 10 mV higher for the thinner samples. By decreasing the wafer thickness from 170 μm (commercial standard) to 40 μm and J_{0S} values 10 times lower, we were able to increase the implied fill factor (i-FF) by 1% absolute, the i-V_{OC} by 30 mV, and the implied efficiency (i-Eff) by 0.6% absolute.

Table 1 Summary of the parameters derived from lifetime measurements of p/i/n-Cz/i/n samples. The baseline values are for samples deposited with baseline intrinsic a-Si:H, the values labelled improved are for samples with a new intrinsic a-Si:H process giving lower J_{os} values. The i-Eff and i-FF were calculated from the implied *J*–*V* curve, assuming a generation current defined by the Lambertian light-trapping limit for the AM1.5G spectrum at 25 °C and normalized to an illumination intensity of 0.100 W cm^{-2}

w, μm	J_{0S}, fA cm^{-2}	i-V_{OC}, mV	W_{OC}, mV	i-FF, %	i-Eff, %
Baseline					
42 ± 2	2.6 ± 0.2	761 ± 3	355 ± 3	85.2 ± 0.1	27.6 ± 0.1
46 ± 2	1.9 ± 0.2	760 ± 3	354 ± 3	84.4 ± 0.1	27.4 ± 0.1
65 ± 2	1.7 ± 0.2	757 ± 2	358 ± 2	84.1 ± 0.1	27.4 ± 0.1
70 ± 2	2.6 ± 0.2	753 ± 2	362 ± 2	84.0 ± 0.1	27.3 ± 0.1
90 ± 2	3.1 ± 0.2	748 ± 2	367 ± 2	83.5 ± 0.1	27.1 ± 0.1
90 ± 2	3.2 ± 0.2	748 ± 2	367 ± 2	83.5 ± 0.1	27.1 ± 0.1
170 ± 2	3.0 ± 0.2	740 ± 1	378 ± 1	84.3 ± 0.1	27.5 ± 0.1
170 ± 2	2.7 ± 0.2	741 ± 1	377 ± 1	84.1 ± 0.1	27.4 ± 0.1
Optimized					
37 ± 2	0.2 ± 0.2	772 ± 3	343 ± 3	85.6 ± 0.1	28.0 ± 0.1
42 ± 2	0.3 ± 0.2	770 ± 3	346 ± 3	85.3 ± 0.1	28.0 ± 0.1
76 ± 2	0.3 ± 0.2	759 ± 2	357 ± 2	84.5 ± 0.1	27.7 ± 0.1
82 ± 2	0.3 ± 0.2	758 ± 2	359 ± 2	85.2 ± 0.1	28.0 ± 0.1
107 ± 2	0.3 ± 0.2	755 ± 2	364 ± 2	86.0 ± 0.1	28.3 ± 0.1
115 ± 2	0.3 ± 0.2	753 ± 1	365 ± 1	85.7 ± 0.1	28.2 ± 0.1
145 ± 2	0.3 ± 0.2	750 ± 1	369 ± 1	85.9 ± 0.1	28.3 ± 0.1
148 ± 2	0.3 ± 0.2	749 ± 1	369 ± 1	85.8 ± 0.1	28.2 ± 0.1

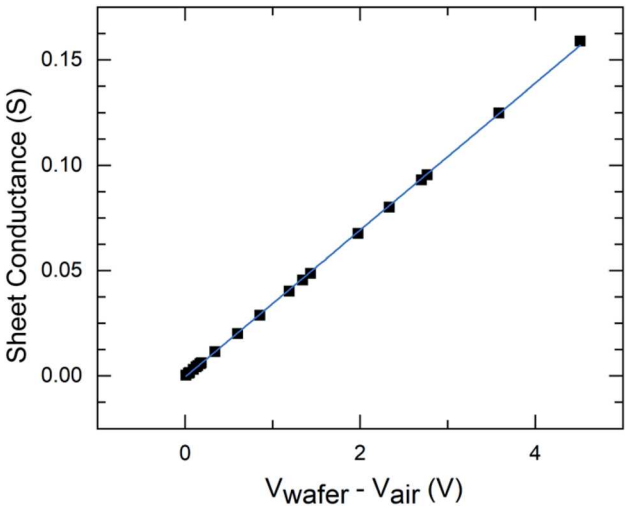

Fig. 7 Sheet conductance measured by four-point-probe *vs.* dark voltage (V_{wafer}–V_{air}) measured by the inductive coil of our WCT-120 system, for samples with various sheet conductance and thickness values. Sheet conductances between 0.003–0.005 S were measured on silicon wafers with thicknesses between 40–200 μm. Higher sheet conductances were measured on indium tin oxide and aluminium films sputtered on glass.

5. Conclusions

We demonstrate that for commercially-viable solar-grade silicon with the surface saturation current density J_{0S} < 0.5 fA cm^{-2} and n-type bulk minority-carrier lifetime of 10 ms, the calculated optimum wafer thickness is between 40–60 μm, far from the projected optimum of 100–110 μm in the ideal case. By optimizing the intrinsic a-Si:H layer we demonstrate experimental J_{0S} values below 0.5 fA cm^{-2} on textured samples, leading to a 10 mV increase in implied V_{OC} for 40 μm-thick samples, 770 mV implied V_{OC}, and W_{OC} of 350 mV. By decreasing the wafer thickness from 170 μm (commercial standard) to 40 μm and decreasing J_{0S} by a factor of 10 in experimental samples, we were able to increase the implied FF by 1% absolute, the implied V_{OC} by 30 mV, and the implied efficiency by 0.6% absolute.

Conflicts of interest

There are no conflicts to declare.

Appendix

(A) Auger and radiative recombination

To account for bandgap narrowing at higher dopant concentrations or photogenerated carrier concentrations, we use the empirical expression from Richter *et al.*:[47]

$$\frac{\Delta n}{\tau_{\text{fund}}} = \frac{\Delta p}{\tau_{\text{int}}} = \frac{\Delta p}{\left(np - {n_{\text{i,eff}}}^2\right)(2.5 \times 10^{-31} g_{\text{eeh}} n_0 + 8.5 \times 10^{-32} g_{\text{ehh}} p_0 + 3.0 \times 10^{-29} \Delta p^{0.92} + B)} \quad \text{(A1)}$$

where the n_0 and p_0 are the equilibrium electron and hole density, and the enhancement factors are defined by:

$$g_{\text{eeh}}(n_0) = 1 + 13\left\{1 - \tan h\left[\left(\frac{n_0}{N_{0,\text{eeh}}}\right)^{0.66}\right]\right\} \quad \text{(A2)}$$

$$g_{\text{ehh}}(p_0) = 1 + 7.5\left\{1 - \tan h\left[\left(\frac{p_0}{N_{0,\text{ehh}}}\right)^{0.63}\right]\right\} \quad \text{(A3)}$$

where $N_{0,\text{eeh}} = 3.3 \times 10^{17}$ cm^{-3} and $N_{0,\text{ehh}} = 7.0 \times 10^{17}$ cm^{-3}. B is the radiative recombination coefficient.[46]

(B) Accuracy of the lifetime measurement

According with a study from Black *et al.*,[60] the relative sensitivity of the inductive coil that measures the sample conductance in the WCT-120 lifetime tester seems to depend on the wafer thickness. A linear relationship between the dark voltage measured by the coil and the sample conductance measured by four-point probe indicates that the lifetime setup is measuring accurately. In Fig. 7 we show a linear relationship between the dark voltage measured by our WCT-120 lifetime tester (V_{wafer}–V_{air}) and the sheet conductance measured using a four-point probe.

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