

Improving surface passivation on very thin substrates for high efficiency silicon heterojunction solar cells

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ABSTRACT

Silicon solar cells are now less than 3% absolute from the theoretical efficiency limit. Advanced passivated contact architectures have demonstrated surface saturation current densities close to 1 fA/cm². We have optimized the thin intrinsic hydrogenated amorphous silicon layer by controlling the deposition temperature and the silane-to-hydrogen dilution ratio. Thin wafers were used as a testbed to increase the sensitivity to surface passivation. By optimizing the intrinsic layer, we reduced the surface saturation current densities from 1.7 fA/cm² to 0.6 fA/cm² on textured wafers with thicknesses ranging between 40 and 180 μm. Implied open-circuit voltages over 760 mV were accomplished on p-i/c-Si/i-n structures deposited on n-type CZ wafers with wafer thicknesses below 50 μm. Further, we demonstrated experimentally the potential of using very thin wafers by manufacturing screen-printed silicon heterojunction solar cells on 40 μm thick standalone wafers while achieving an efficiency of 20.48%.

1. Introduction

In the last decade, the quality of commercially affordable bulk silicon has improved remarkably, especially with n-type Czochralski (CZ) wafers reaching bulk lifetimes over several milliseconds [1]. As a result, surface passivation is now the main factor limiting solar cell efficiency. Passivated emitter and rear cell (PERC) solar cells are the new market standard, replacing aluminum back surface field (BSF) solar cells [2]. Further, more advanced architectures, with better surface passivation schemes are now paving their way into the market [3–6]. The silicon heterojunction (SHJ) [7] and interdigitated back contact (IBC) solar cells [4] are two architectures that are already commercially available with open-circuit voltages (V_{OC}) surpassing 700 mV and with demonstrated potential to surpass 25% efficiency on large-area devices. These devices typically have surface saturation current densities (J_{0S}) below 10 fA/cm² [8]. The record efficiency silicon solar cell combines both IBC and SHJ architectures, thereby demonstrating the potential to achieve J_{0S} down to 0.9 fA/cm² [6].

Since effective minority carrier lifetime (τ_{eff}) response to surface recombination increases inversely with wafer thickness [9], thin wafers were used in this work as a testbed to improve surface passivation. From a commercial perspective, thinner wafers are an opportunity to increase the competitiveness of silicon solar cells. The use of thinner wafers can

potentially decrease the capital expenditure (capex) of solar modules [10] and positively impact the levelized cost of energy (LCOE) of PV systems. Additionally, thinner wafers enable more flexible and lighter module designs, making them more compelling in market segments like building integrated photovoltaics (BIPV) [11], portable power applications [12,13] and aerospace and automotive industries [14]. These factors have led to an increasing interest in exploring SHJ solar cells using thin wafers. Recently, researchers at CEA, France [15], AIST, Japan [16], Sanyo, Japan [17,18] and IMEC, Belgium [19,20] have reported V_{OC} values greater than 740 mV using thin silicon wafers with efficiencies above 20%.

In the past, we have demonstrated open-circuit voltages over 760 mV and J_{0S} below 1 fA/cm² on 50 μm thick SHJ structures [21]. Those structures were designed to maximize surface passivation and voltage by using a thick (15 nm) intrinsic hydrogenated amorphous silicon (a-Si:H) layer on non-textured surfaces. Both implied (iFF) and pseudo fill factors (pFF) were greater than 85%. However, the use of a very thick intrinsic layer led to fill factors (FF) below 60%. Various groups have reported intrinsic a-Si:H layers in the range of 5–7 nm thickness to deliver efficiencies greater than 20% [22,23]. In this work, we accomplished J_{0S} below 1 fA/cm² and implied open-circuit voltage (iV_{OC}) of 764 mV on 40 μm thick textured wafers by developing a 6 nm thick intrinsic a-Si:H layer. We manufactured large area, screen-printed silicon

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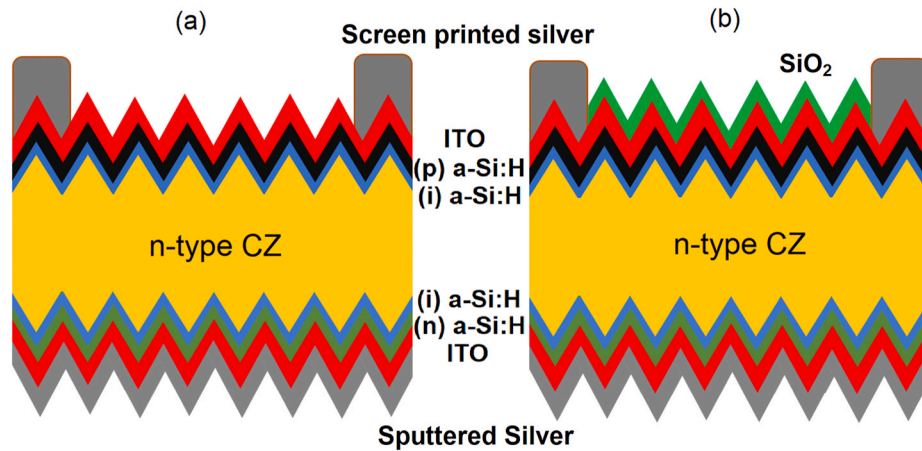


Fig. 1. Illustration of SHJ solar cells fabricated with two different ARC structures: a) 75 nm ITO and b) 100 nm SiO_x and 40 nm ITO stack.

heterojunction solar cells using these thin wafers and achieved efficiencies close to 21%. Light trapping was also improved by using SiO_x :ITO stacks as a front anti-reflective coating (ARC) film.

2. Experimental procedure

Silicon heterojunction samples were fabricated on n-type CZ wafers, with a starting thickness of 200 μm and bulk resistivity of 3–4 $\Omega\text{-cm}$. The wafers were thinned to different thicknesses from 180 to 40 μm using potassium hydroxide (KOH) solution. The samples were textured using alkaline wet etching (KOH and GP Solar additive), followed by an acidic cleaning process which is described in detail elsewhere [24]. The thickness of the wafers was measured after texturing, at five different points, using a digital thickness gauge with 1 μm resolution. A three-chamber plasma enhanced chemical vapor deposition (PECVD) cluster tool was used to deposit 6–15 nm thick intrinsic and n/p-doped hydrogenated amorphous silicon (a-Si:H) layers, forming a p-i/c-Si/i-n stack. The p-i stack was first deposited on one side of the wafer followed by the i-n stack on the other side. The intrinsic a-Si:H was treated with an in-situ hydrogen plasma to improve the chemical passivation [25]. To improve the passivation properties of the intrinsic a-Si:H layer, we varied the PECVD susceptor temperatures and silane (SiH_4)-to-hydrogen (H_2) dilution ratios. The doped a-Si:H layers deposition parameters (susceptor temperature and gas flows) were kept constant across the entire study. Specifically, the susceptor temperature used for the doped layers was 250 $^\circ\text{C}$. The effective minority carrier lifetime was measured using a Sinton photoconductance-decay lifetime tester (WCT-120). The implied voltage parameters and J_{05} were calculated from the lifetime measurement.

Indium tin oxide (ITO) was deposited on both front and rear surfaces using a DC sputtering technique. A silver contact, also acting as a reflective mirror, was sputtered on the rear side. Front contacts were screen printed with silver paste. As shown in Fig. 1, two different anti-reflective coatings (ARC) were fabricated. In the standard process, Fig. 1(a), 75 nm layer of ITO is sputtered on the front surface of the solar cell. To mitigate the parasitic absorption of the front ITO, the thickness of ITO was reduced to 40 nm and 100 nm of non-stoichiometric silicon oxide (SiO_x) layer was deposited by PECVD to complement the anti-reflective properties of the thinner ITO, Fig. 1 (b). All the cells were annealed for 30 min at 200 $^\circ\text{C}$. A Sinton FCT-450 flash tester was used to measure the I-V characteristics of the solar cells.

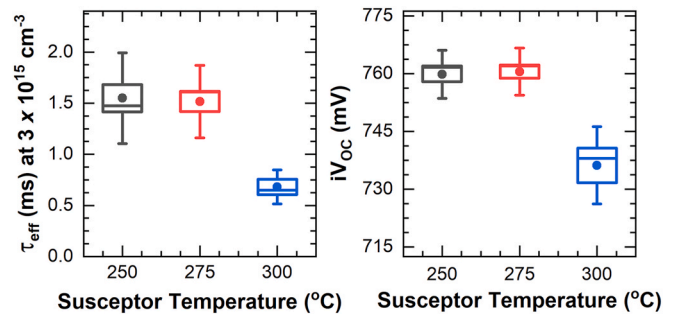


Fig. 2. Measured effective minority carrier lifetime (at $3 \times 10^{15} \text{ cm}^{-3}$ injection level) and implied open circuit voltage (iV_{oc}) of p-i/c-Si/i-n structures deposited on $42 \pm 2 \mu\text{m}$ thick wafers. The deposition temperature of the intrinsic layer was varied by controlling the susceptor temperature. The intrinsic layer thickness (6 nm) and silane-to-hydrogen (SiH_4 : H_2) dilution ratio (20%) were kept constant for all samples. The p and n doped layers were the same for all samples. Ten samples were measured for each deposition condition.

3. Results and discussion

3.1. Impact of susceptor temperature and silane-to-hydrogen dilution ratio

In our intrinsic a-Si:H baseline deposition process, the PECVD susceptor temperature is 250 $^\circ\text{C}$ and silane-to-hydrogen dilution ratio is 20%. A deposition temperature setpoint of 250 $^\circ\text{C}$ has been previously reported to deliver an intrinsic layer with good passivation properties [26,27]. Different temperatures may be desirable as they impact the hydrogen content and microstructure of the film [28,29], which controls the passivation properties of the a-Si:H layer. In this study, we used textured thin wafers ($\sim 40 \mu\text{m}$) as a testbed to increase the sensitivity to the surface passivation. In Fig. 2, we show the distribution of effective minority carrier lifetime (left) and implied open-circuit voltage (iV_{oc}) (right) for depositions of intrinsic a-Si:H at different setpoint temperatures and with a silane-to-hydrogen dilution ratio of 20%. As the deposition rate is temperature dependent, the deposition time was adjusted to achieve the same thickness of a-Si:H (6 nm) for all samples. The average effective minority carrier lifetime is comparable for 250 $^\circ\text{C}$ and 275 $^\circ\text{C}$, approximately 1.5 ms, but considerably lower for 300 $^\circ\text{C}$, 0.6 ms. Lower effective minority carrier lifetimes at 300 $^\circ\text{C}$ can be due to the amorphous-to-crystalline transition of the a-Si:H layer at higher temperatures [27]. We varied the wafer temperature in the PECVD tool by controlling the susceptor temperature. The temperature is measured on the bottom of the susceptor, and the software incorporated in the tool

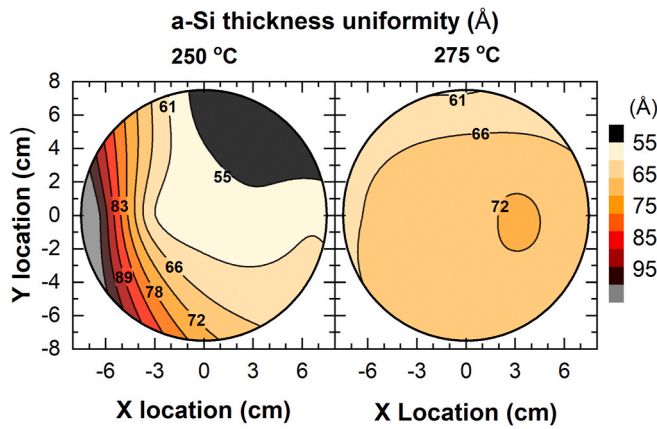


Fig. 3. Variation of a-Si thickness deposited on a 150 mm polished wafer for two different susceptor temperatures measured using VASE. The average thickness is 6.5 nm for both deposition conditions. The non-uniformity is 5.1% at 275 °C and 34.6% at 250 °C.

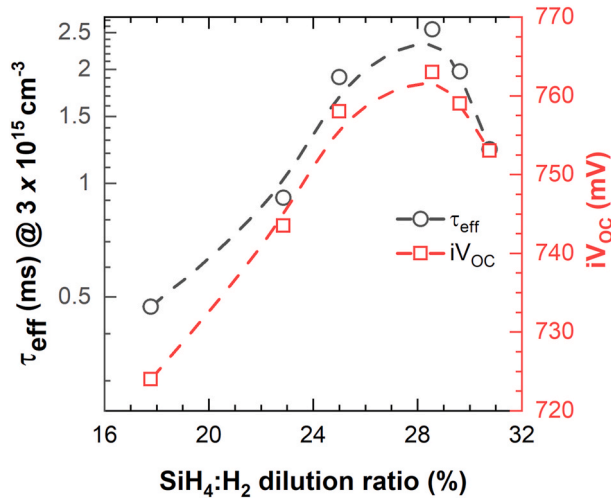


Fig. 4. Effective minority carrier lifetime and iV_{OC} of $42 \pm 2 \mu\text{m}$ thick wafers as a function of different silane-to-hydrogen ($\text{SiH}_4:\text{H}_2$) dilution ratios for a susceptor temperature of 275 °C. p-i and i-n a-Si:H layers were deposited on these wafers. Each data point represents an average effective minority carrier lifetime and iV_{OC} obtained from two wafers. The dashed lines are a guidance to the eye obtained using b-spline smoothing function to fit the data. The average thickness of a-Si:H doesn't vary significantly between different dilution ratios. An injection level of $3 \times 10^{15} \text{ cm}^{-3}$ represents the maximum power point for $42 \pm 2 \mu\text{m}$ thick wafers.

and developed by the PECVD manufacturer estimates the wafer temperature. For susceptor temperatures of 250 °C, 275 °C, and 300 °C, the estimated wafer temperatures are 233 °C, 244 °C, and 265 °C, respectively. These wafer temperatures are within the range of optimum deposition temperatures reported by other groups [16,26,27].

Thickness uniformity of the intrinsic a-Si:H layer across the wafer area is a required condition to deliver high efficiencies on commercial size SHJ solar cells. The thickness uniformity of the a-Si:H films deposited at 250 °C and 275 °C were measured on 150 mm polished wafers using variable angle spectroscopic ellipsometry (VASE). As shown in Fig. 3, the thickness uniformity improves when samples are deposited at 275 °C. The non-uniformity, for the same intrinsic layer thickness, was 34.6% for samples deposited at 250 °C and 5.1% for samples deposited at 275 °C. The deposition of the intrinsic a-Si:H layer is not only controlled by temperature but also by multiple other parameters [30]. Previous studies on gas-phase reaction and transport

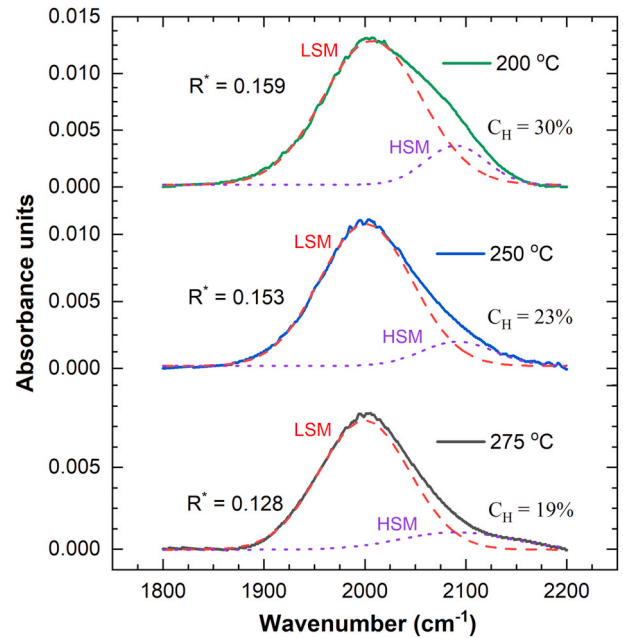


Fig. 5. Comparison of FTIR spectra for different susceptor temperatures in transmission mode. The solid lines represent the absorbance. The dashed lines indicate the LSM peak fits done between 1900 and 2010 cm^{-1} . The dotted lines indicate the HSM peak fits done between 2090 and 2110 cm^{-1} . R^* for each peak is calculated according to Ref. [28]. C_H is calculated according to Refs. [32]. The intrinsic a-Si:H thickness of 110 nm and in-situ hydrogen plasma time was kept constant for all samples.

phenomenon for PECVD processes illustrate wafer temperature regulation, within a range of 7 °C, along concentric zones have sizable impact ($>10\%$) on thickness uniformity [31]. Since we are targeting very thin layers, we are constrained by our process to use extremely short deposition times, on the order of five to 7 s. Over this temporal range, seemingly subtle differences in plasma ignition time and incipient plasma uniformity can have a sizable impact on film reproducibility. The susceptor temperature of 275 °C was the condition that delivered the best reproducibility and uniformity for the desirable film thickness, Fig. 3.

The hydrogen content of the intrinsic a-Si:H layer is also controlled by the silane-to-hydrogen dilution ratio during the deposition. In Fig. 4, we show how effective minority carrier lifetime and iV_{OC} change with different dilution ratios for a susceptor temperature of 275 °C. As the dilution ratio increases from 17.8% to 28.6%, the effective minority carrier lifetime increases from 0.5 ms to 2.4 ms around the maximum power point injection level. A further increase in the dilution ratio to 30.8% leads to about a 1 ms loss in effective minority carrier lifetime. The best effective minority carrier lifetime and iV_{OC} were obtained for a dilution ratio of 28.6%. For a $42 \pm 2 \mu\text{m}$ thick wafer, we measured an effective minority carrier lifetime and iV_{OC} of 2.4 ms and 763 mV, respectively.

The content of hydrogen in the a-Si:H layer is one of the critical factors to achieve high effective minority carrier lifetime [29]. Hydrogenation of silicon dangling bonds reduces the density of defects at the interface leading to higher effective minority carrier lifetimes [29]. In Fig. 5 we measure the hydrogen content and the microstructure fraction coefficient (R^*) [28] of the intrinsic a-Si:H films deposited at different susceptor temperatures using Fourier transform infrared (FTIR) spectroscopy in transmission mode. The samples measured in Fig. 5 were prepared by depositing 110 nm of intrinsic a-Si:H layer on single side polished wafers. Similar thicknesses were achieved by controlling the deposition time for different susceptor temperatures. The in-situ hydrogen plasma treatment parameters were kept constant for the

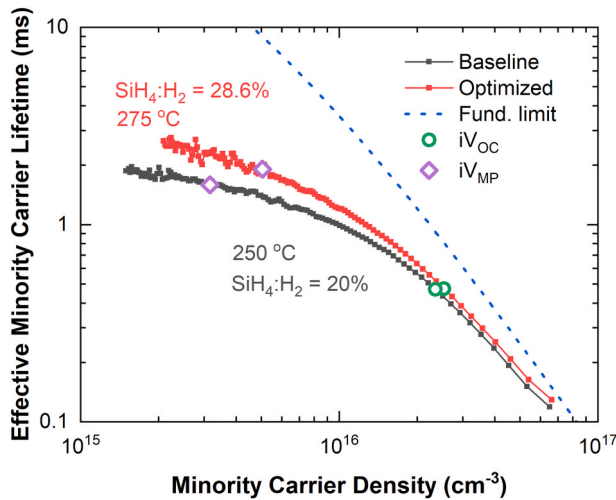


Fig. 6. Comparison of τ_{eff} vs minority carrier density on $42 \pm 2 \mu\text{m}$ thick wafers for the baseline and optimized process. iV_{OC} and iV_{MP} are indicated as seen in the graph. The dashed blue line represents the fundamental (Auger and radiative) minority carrier lifetime limit calculated according to Richter et al. parameterization [36]. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

different susceptor temperatures.

Silicon hydride (Si-H_x) bond vibrations have been extensively studied and determined to have three characteristic absorptions: a wagging mode at 640 cm^{-1} , a bending scissor mode at $840\text{--}890 \text{ cm}^{-1}$, and a stretching mode between 1980 and 2160 cm^{-1} [33]. Stretching modes can be further divided into a low stretching mode (LSM) at $1980\text{--}2030 \text{ cm}^{-1}$ and a high stretching mode (HSM) at $2060\text{--}2160 \text{ cm}^{-1}$ [33]. Previous results have shown the LSM to be associated with monohydride (Si-H) bonds; similarly, the HSM is attributed to dihydride (Si-H_2) bonds [34]. The total hydrogen content (C_{H} %) was obtained by the integration of the Si-H absorption peak at 640 cm^{-1} [32]. An increase of the R^* value has been correlated with a decrease in density of the a-Si:H film due to the presence of vacancies and voids and hydrogen content as well [35]. A high R^* value has been also attributed to higher disorder in the film [35].

Higher susceptor temperatures show lower and broader HSM absorbance peaks (Fig. 5) resulting in lower R^* values and more ordered films. However, higher temperatures also result in lower hydrogen content. The passivation capability of the a-Si:H layer benefits from a more ordered and hydrogen-rich film [29]. The a-Si:H shows better R^* for the 275°C process and incorporates lesser hydrogen than films deposited at lower temperatures. From this point further, the process to deposit films using a susceptor temperature of 275°C and a dilution ratio of 28.6% will be named as the optimized process.

3.2. Implied voltage characteristics at maximum power and open circuit

A comparison of effective minority carrier lifetime between the baseline and optimized processes is shown in Fig. 6. The difference in lifetime between the fundamental and the experimental data decreases with increasing carrier density, indicating that the fundamental recombination plays a larger role at open circuit than at maximum power injection. For $40 \mu\text{m}$ thick samples the optimized process shows voltage improvements of 20 mV at implied maximum power (iV_{MP}) and 5 mV at implied open circuit (iV_{OC}). The implied fill factor (iFF) improves over 1% absolute. The improvement of voltage at the maximum power is larger than at open circuit, as surface recombination plays a larger role at maximum power [9].

To evaluate the benefits of the optimized process for different wafers thicknesses, we manufactured p-i/c-Si/i-n structures on textured wafers

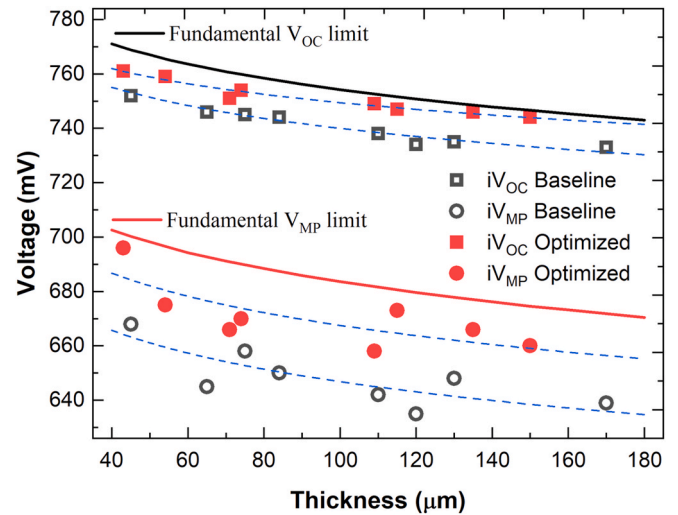


Fig. 7. Comparison of iV_{OC} and iV_{MP} of the optimized and baseline processes for textured wafers of different thicknesses. The solid black and red lines represent the fundamental V_{OC} and V_{MP} limits. The dashed lines indicate logarithmic fits to the data. Implied voltages are obtained for the wafers using the Sinton lifetime tester, after depositing i-p and i-n layers on them. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

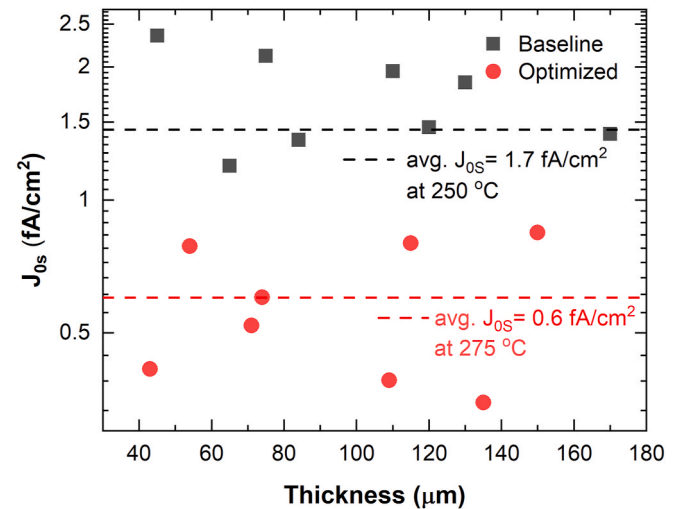


Fig. 8. The $J_{0\text{S}}$ for different wafer thickness for optimized and baseline processes. The dashed lines indicate the average $J_{0\text{S}}$ obtained from all the data points for different thicknesses. A base-10 log scale is used for the Y axis.

with thickness between 40 and $175 \mu\text{m}$. Fig. 7 shows how voltage is impacted by the two processes as the wafer thickness changes. The fundamental limits of V_{OC} and V_{MP} were calculated using the method previously described in Ref. [17]. In Fig. 7 the optimized process delivers higher iV_{MP} and iV_{OC} than the baseline process, independent of the wafer thickness. At iV_{OC} for the optimized process, the fundamental recombination is the dominant contributor to the total recombination. As the thickness of the wafer decreases the contribution of fundamental recombination decreases whereas the contribution of surface recombination increases, resulting in a larger deviation from the fundamental limit for thinner wafers ($<80 \mu\text{m}$). At iV_{MP} , both bulk Shockley-Read-Hall (SRH) and surface recombination play an important role. As we reduce the thickness of the wafer, the contribution of the surface to the total recombination increases, whereas the bulk SRH recombination decreases. As a result, the total contribution of these two

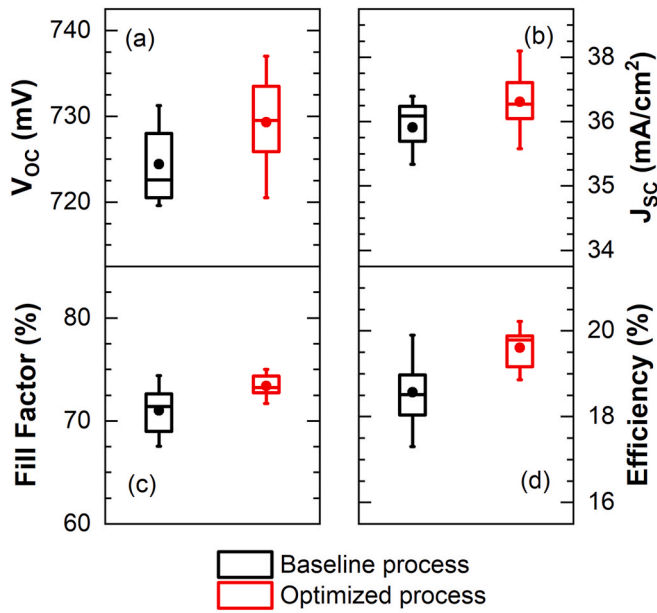


Fig. 9. I–V characteristics of $42 \pm 2 \mu\text{m}$ thick, 4 cm^2 SHJ solar cells manufactured using the intrinsic a-Si:H layer baseline and optimized processes. The thickness of intrinsic a-Si:H layer is 6 nm for both the cases. The V_{OC} (a), J_{SC} (b), FF (c), and efficiency (d) are improved with the optimized process. The structure of these cells is as represented in Fig. 1(a). The sample size was greater than 10 for each process.

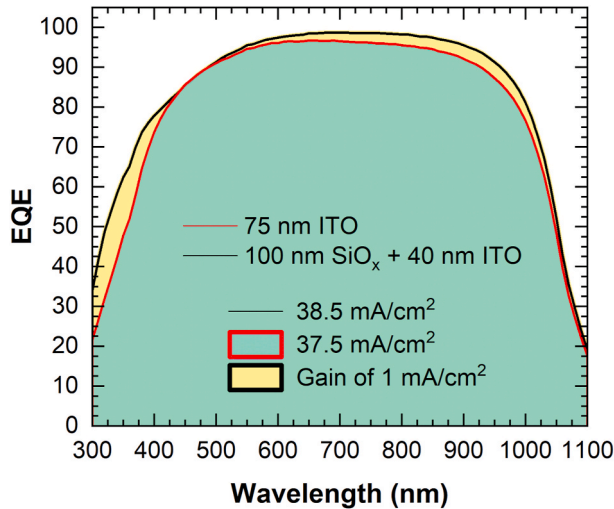


Fig. 10. EQE of representative samples for the two types of solar cell structures shown in Fig. 1 using $42 \pm 2 \mu\text{m}$ thick textured wafers. J_{gen} of 37.5 mA/cm^2 achieved using 75 nm ITO and 38.6 mA/cm^2 using SiO_x/ITO stack. The optimized process was used to deposit the intrinsic a-Si:H layer for these samples.

recombination mechanisms at iV_{MP} seems to balance each other for different wafer thicknesses.

3.3. Improvement of surface saturation current density

The total surface saturation current density (J_{0S}) was estimated from a linear fit to the Auger-corrected inverse effective minority carrier lifetime data as a function of excess carrier density in the range of 8×10^{15} and $1.3 \times 10^{16} \text{ cm}^{-3}$ [37]. Fig. 8 shows the total J_{0S} values using the two processes for different wafer thicknesses. Average J_{0S} of 0.6 fA/cm^2 was accomplished using the optimized process. Previously [21], we demonstrated J_{0S} close to 0.1 fA/cm^2 by depositing a 15 nm thick

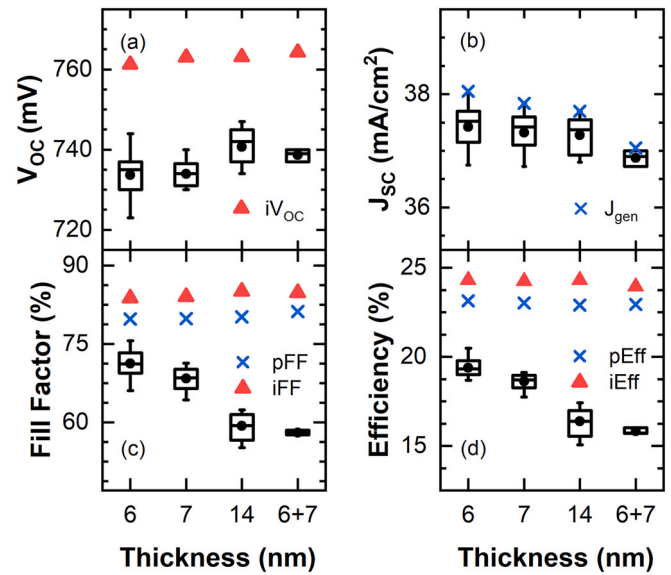


Fig. 11. I–V characteristics of $42 \pm 2 \mu\text{m}$ thick, 4 cm^2 , SHJ solar cells as a function of intrinsic a-Si:H layer thickness: a) V_{OC} , the markers represent iV_{OC} ; b) J_{SC} , the markers represent J_{gen} ; c) FF, where the x marks indicate the pFF, the triangles indicate implied fill factor (iFF); and d) efficiency, where the x marks indicate the average pseudo efficiency (pEff) and the triangles indicate implied efficiency (iEff). The optimized process was used to deposit intrinsic a-Si:H for all the samples. The structure of these cells is as represented in Fig. 1(b). The sample size is greater than 10 for 6, 7, and 14 nm thick intrinsic a-Si:H layer and 4 for a bilayer intrinsic a-Si:H layer.

layer of intrinsic a-Si:H on untextured wafers. The thick layer prevented us to obtain a fill factor (FF) greater than 60%. In this work we are demonstrating similar levels of passivation by using a layer that is more than two times thinner compared to our previous work. Moreover, all the J_{0S} and implied voltage characteristics presented here are on textured wafers.

3.4. Solar cell results

We manufactured SHJ solar cells using the two intrinsic layers previously described. The I–V characteristics are shown in Fig. 9. All I–V parameters improved with the new intrinsic layer. The V_{OC} , J_{SC} , FF and efficiency increase by 5 mV, 0.5 mA/cm^2 , 2% absolute and 1% absolute, respectively. The optimized process improves the V_{MP} which also influences the gain seen in FF when compared to the baseline process. The variation in J_{SC} can be attributed to non-uniformities in the ITO layer, wafer thickness and texturing variations, and slight deviation in alignment between screen printed samples due to handling.

We manufactured SHJ solar cells with two anti-reflective coating stacks as shown in Fig. 1. To mitigate the light absorption, we reduced the thickness of ITO and added a silicon oxide layer to preserve the anti-reflective properties of the cell [38]. In Fig. 10, the SiO_x/ITO stack shows an improvement (yellow shaded area) of 1 mA/cm^2 in photogeneration current density (J_{gen}). The J_{gen} for the device was calculated by measuring the external quantum efficiency (EQE). The SiO_x/ITO stack shows a gain in current across a wide range of wavelengths. As compared to structure (a) of Fig. 1, there is an absolute gain of 0.6 mA/cm^2 in the wavelength range of 300–450 nm and an increase of 0.3 mA/cm^2 in the wavelength range of 800–1050 nm by using structure (b) of Fig. 1.

A thicker intrinsic a-Si:H layer is expected to deliver better surface passivation leading to higher minority carrier lifetime and open circuit voltage. In the past we successfully grew a thick intrinsic a-Si:H layer in two steps forming a bilayer [21]. The idea is to deposit a thin layer, perform the hydrogen plasma treatment and then deposit the rest of the

Table 1

Comparison of $42 \pm 2 \mu\text{m}$ thick SHJ solar cells of different areas but with similar effective minority carrier lifetimes at $3 \times 10^{15} \text{ cm}^{-3}$. τ_{eff} , iV_{OC} and $i\text{FF}$ were measured on p-i/c-Si/i-n structures. V_{OC} , pFF, FF, J_{SC} , R_{S} and Efficiency (Eff) were measured on completed SHJ solar cells. The J_{SC} values for the first two solar cells shown here are lower than in Fig. 11 because the SiO_x/ITO stack was not incorporated in this experiment.

Cell area (cm^2)	τ_{eff} (μs)	iV_{OC} (mV)	$i\text{FF}$ (%)	V_{OC} (mV)	pFF (%)	FF (%)	J_{SC} (mA/cm^2)	R_{S} ($\Omega \text{ cm}^2$)	Eff (%)
153.9	1440	764	83.7	747	82.4	75.7	34.0	1.57	19.22
4	1432	764	83.7	740	80.8	73.5	36.4	1.60	19.80
4 ^a	1767	761	85.0	741	81.4	72.3	38.3	1.99	20.48

^a Represents the best SHJ solar cell using SiO_x/ITO ARC stack Fig. 1(b).

stack. This could promote a better diffusion of hydrogen to the intrinsic a-Si:H/c-Si-interface, enhancing the surface passivation [17]. In this work, a bilayer of intrinsic a-Si:H was formed by first depositing a 6 nm of intrinsic a-Si:H, followed by hydrogen plasma, and finally a 7 nm of intrinsic a-Si:H was deposited. Fig. 11 shows the I-V characteristics of the SHJ solar cells as a function of intrinsic a-Si:H thickness. The best efficiency on a $40 \pm 2 \mu\text{m}$ thick wafer using the optimized process and SiO_x/ITO ARC stack was 20.48%. The V_{OC} of the cells increases with an increase of intrinsic a-Si:H thickness, Fig. 11 (a). The difference between iV_{OC} and V_{OC} is mitigated when we use a thicker intrinsic layer, Fig. 11 (a), as the interface is likely to be partially shielded from sputtering damage [39]. The short circuit current density (J_{SC}) decreases slightly as the absorption increases with layer thickness, Fig. 11 (b). Fig. 11 (b) also shows slightly different values of J_{SC} between the 14 nm thick layer and the bilayer (6 + 7 nm). This slight difference could be related with the fact that the number of samples processed with the bilayer was less than half of any other type samples, since we didn't expect sizable differences between the thick intrinsic a-Si:H and the bilayer samples. Implied fill factors (iFF) greater than 84% were attained for all the SHJ solar cells used in the study. The pseudo fill factor (pFF) increases by 1.3% absolute when a thicker intrinsic layer is deposited. However, thicker layers lead to higher series resistance [40], as seen in Fig. 11 (c). The fill factor reduces to less than 60% for a thick layer of intrinsic a-Si:H. Implied efficiency (iEff) of the SHJ solar cells was calculated by using the product of iV_{OC} , iFF and J_{gen} , Fig. 11 (d). Using the recombination limit and the light trapping characteristics of our cells, i.e., the implied voltage parameters and the generation current of our stacked ARC structure respectively, we get implied efficiencies greater than 24% and pseudo efficiencies greater than 23% for all the samples, Fig. 11 (d). Improvement in carrier selectivity of doped layers, increasing the mobility of the ITO layer, mitigating sputter damage and better front metallization scheme are some of ways to reduce the difference between pseudo efficiency and the actual efficiency for our SHJ solar cells.

The top efficiencies on SHJ solar cells are typically reported on large area solar cells [1,4,6,7]. The reported results of SHJ solar cells in Figs. 9–11 are 4 cm^2 in area. We manufactured solar cells with two different areas and similar implied I-V parameters to evaluate the impact of the area on the cell performance, and the results are provided in Table 1. The larger cell shows lower V_{OC} loss and higher pFF. Since both the cells experienced the same manufacturing process, the only difference is the ratio of cell perimeter to cell area. This seems to indicate that smaller cells, that is, those with a larger perimeter-to-cell-area ratio, have larger edge recombination [41]. The difference in iV_{OC} and V_{OC} can also be attributed in part to the sputtering damage which results in the loss of surface passivation [39]. According with the values shown in

Table 1, about 87% of the difference between the pFF and FF is caused by the series resistance (R_{S}). The R_{S} values are obtained from the Sinton I-V measurement tool. This is also the case for the SHJ solar cells shown in Fig. 11.

4. Conclusions

Modifying the deposition parameters of the intrinsic a-Si:H led to improvements in surface saturation current density, implied voltages at maximum power and open circuit across the entire range of wafer thicknesses considered in this study. An average surface saturation current density of $0.6 \text{ fA}/\text{cm}^2$ was accomplished using the new process, reducing the surface saturation current density by half of the baseline. Implied voltage at maximum power and open circuit improved by an average of 21 mV and 8 mV, respectively. Open circuit voltage over 760 mV and implied fill factors above 85% were measured on i-p/i-n stacks deposited on $40 \mu\text{m}$ thick wafers. We successfully demonstrated experimentally the potential to exceed 21% efficiency using screen printed $40 \mu\text{m}$ thick silicon heterojunction solar cells. Further improvements in efficiency need to address losses in open circuit voltage and fill factor. The results suggest the losses are in part related to the damage induced during the sputtering process of ITO and the solar cell area. The FF losses are largely driven by the series resistance that can be partially improved by a better metallization design.

CRedit authorship contribution statement

Pradeep Balaji: Conceptualization, Investigation, Writing - original draft. **William J. Dauksher:** Methodology, Writing - review & editing. **Stuart G. Bowden:** Resources, Funding acquisition, Writing - review & editing. **André Augusto:** Conceptualization, Writing - review & editing, Supervision.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Appendix

Accuracy of lifetime measurements

Recent work by Black et al. [42] discusses how parameters extracted from lifetime measurements, e.g. $J_{0\text{S}}$ and iV_{OC} , can be incorrectly estimated when using an inductively coupled photoconductance decay method [43]. The relative sensitivity of the inductive coil used to measure the sample conductance appears to depend on the silicon wafer thickness. A linear relationship between the dark voltage measured by the coil and the sample conductance measured by a four-point probe is a good indicator of lifetime measurement accuracy [42].

In Fig. 12(a) we show how the sheet conductance varies with excess carrier density and wafer thickness. For wafer thicknesses between 20 and 160 μm our experimental setup must measure sheet conductance accurately between 0.005 S and 0.09 S. These values correspond to the excess carrier densities of interest to measure the voltage at maximum power and open circuit voltages. To estimate these excess carrier densities, we assumed the fundamental limit of recombination.

Samples with a wide range of sheet conductance values were manufactured. By varying the thickness of bare silicon wafers, we were able to measure sheet conductance between 0.003 and 0.005 S; for higher values of sheet conductance, we sputtered different film thicknesses of ITO and aluminum on glass slides. In Fig. 12(b), we show that the dark photovoltage measured by the lifetime testers has a linear relationship with the sheet conductance measured using the four-point probe. This is a good indication that the parameters derived from the lifetime measurements are accurate.

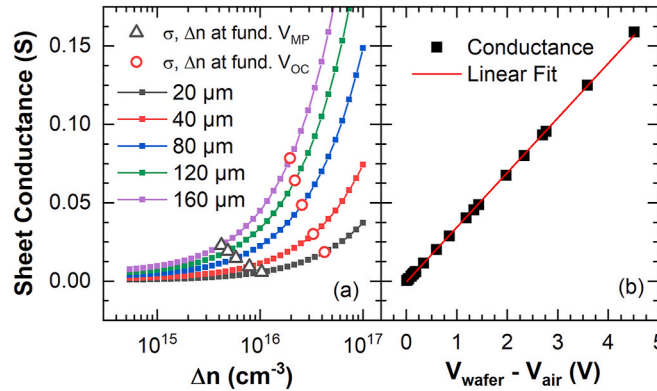


Fig. 12. (a) Variation of sheet conductance calculated for n-type silicon wafers of different thicknesses with a base doping of $1.5 \times 10^{15} \text{ cm}^{-3}$ at different excess carrier density. The triangular markers represent the sheet conductance calculated vs excess carrier density (Δn) of wafers at their fundamental V_{MP} limit and the red circular markers represent the same at their fundamental V_{OC} limit. (b) Sheet conductance measured by four-point-probe versus voltage measured by the inductive coil of the WCT-120 system obtained using samples with various resistivities and thicknesses.

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