3-D Physical Model for On-chip Power Inductor Design with Evaluation of Airgap Variation Effect

Zhiyong Xia, *Student Member*, *IEEE*, Jaber A. Abu Qahouq, *Senior Member, IEEE* and Sushma Kotru, *Senior Member, IEEE*

The University of Alabama
Department of Electrical and Computer Engineering
Tuscaloosa, Alabama 35487, USA

***Abstract*—The miniaturization of power inductor helps to achieve high power density of power converters. The development of on-chip power inductors is an important step towards achieving this goal. A 3-D model for an on-chip power inductor is developed in ANSYS®/Maxwell® software in this paper to facilitate the design of on-chip power inductor with on-chip ferrite core. The effects of air gap variation in the on-chip inductor are evaluated using the 3-D physical model and simulations with the on-chip ferrite core. The tradeoff between high inductance value and high saturation value as a function of the air gap between the ferrite layer and winding layer is evaluated from the model and simulations in order to facilitate the optimization and design before fabrication of the complete device.**

Keywords—Power inductor, on-chip, inductance, saturation current, air gap, ferrite, ANSYS®/Maxwell®, 3-D model, simulation, miniaturization, power converter, power electronics.

I. INTRODUCTION

Power inductor as one of the largest components used in power electronic converters significantly affects the dimensions and weight of these converters [1-10]. The miniaturization of power inductor helps to reduce power converter solution size and increase power density [1-6]. The development of on-chip power inductors as one important direction for miniaturization of power inductors has become a research topic of significant interest.

Inductance and saturation current are two critical performance metrics of power inductor. Higher inductance and higher saturation current are desired in power electronics products. In order to fabricate on-chip power inductors that meet the specific requirements of practical applications with regard to inductance value and saturation current, the design parameters of on-chip power inductor need to be optimized and carefully tuned. 3-D physical model and simulation can be utilized to guide the optimization and tuning of design parameters of on-chip power inductor before fabricating the complete device. It can help to reduce development cycle and cost of fabrication process.

Air gap between the ferrite layer and copper winding layer is an important design parameter of on-chip power inductor. It affects the inductance value and saturation current value of on-chip power inductor. In order to fabricate on-chip power inductors with satisfactory performance, the air gap of on-chip power inductor needs to be carefully tuned and selected. In this paper, 3-D physical model of on-chip power inductor is developed in ANSYS®/Maxwell® software to guide the tuning and optimization of air gap of on-chip power inductor before fabrication of the complete on-chip power inductor device. The simulation results presented in this paper evaluated the tradeoff between high inductance value and high saturation value as a function of the air gap between ferrite layer and winding layer.

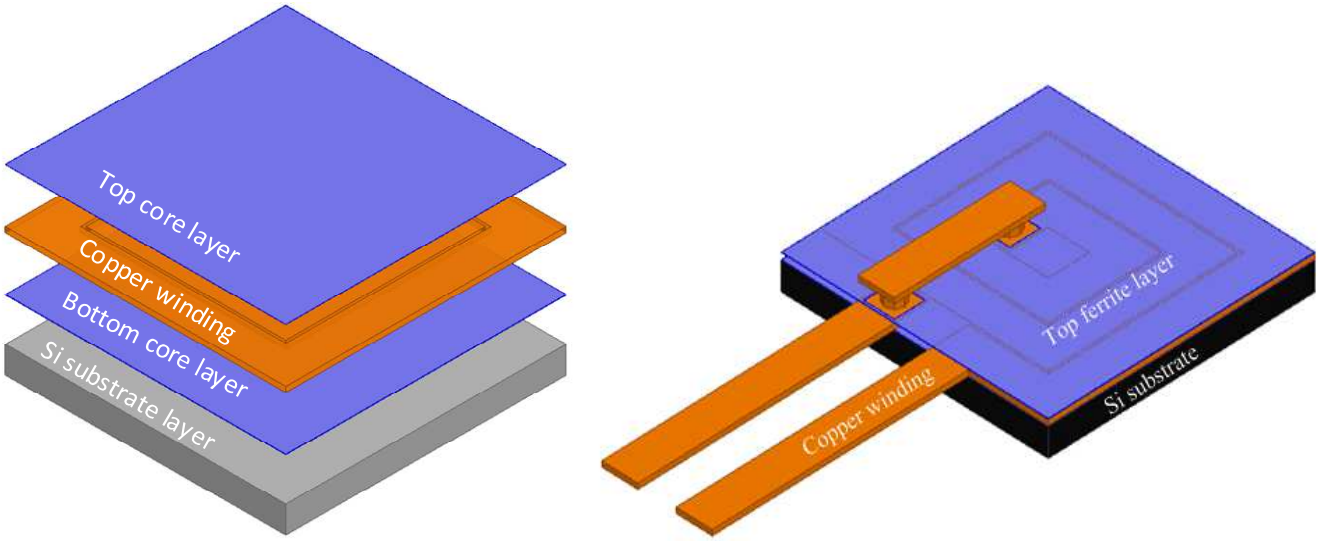
Next section presents the structure, dimension, and utilized materials of the on-chip power inductor presented in this paper. Section III presents simulation results of the on-chip power inductor and the effects of air gap on the inductance value and saturation current of power inductor. The conclusion of this paper is given in Section IV.

II. STRUCTURE, DIMENSION, AND UTILIZAED MATERIALS OF ON-CHIP POWER INDUCTOR

The presented on-chip power inductor design includes four different layers, i.e., top ferrite core layer, copper winding layer, bottom ferrite core layer, and silicon substrate layer. These layers are stacked as illustrated in Fig. 1(a). The copper winding layer is placed between the top ferrite core layer and bottom ferrite core layer. The overall assembly structure of the on-chip power inductor is illustrated in Fig. 1(b).

The dimension parameters and material property of each layer of the on-chip power inductor are given in Table I. The thickness for each of the top ferrite layer and bottom ferrite layer is 525 μm with width of 5.2 mm and length of 5.2 mm. The utilized ferrite material is Ni-Zn type ferrite with permeability of 100 and saturated flux density, i.e., B_s, of 0.28 T, as obtained from the fabrication results in [1]. The top air gap between top ferrite layer and copper winding and the bottom air gap between top ferrite layer and copper winding are set to be equal. The design is evaluated with airgap values of 4 μm, 7 μm, and 10 μm

to investigate effects of air gap on the saturation current and inductance value of designed on-chip power inductor. For the winding layer, the spiral structure is adopted. There are three turns in the cooper winding with each copper turn width of 0.7 mm, 50 µm winding gap between each turn, and winding thickness of 100 µm. The thickness of substrate layer is 200 µm. The overall heights of the designed on-chip power inductor are 1.358 mm, 1.364 mm, and 1.37 mm for the 4 µm air gap case, 7 µm air gap case, and 10 µm air gap case, respectively.



(a) (b)

Fig. 1. (a) Layer placement of on-chip power inductor and (b) overall assembly structure of on-chip power inductor.

TABLE I
The dimension parameters and material property of each layer of the designed on-chip power inductors

Name	Dimension	Material
Top ferrite core layer	5.2mm × 5.2mm 525µm thick	NiZn ferrite Bsat=0.28T µ=100 [1]
Top air gap between winding and top core layer	4µm/7µm/10µm	SiO_2 (or other insulator)
Spiral winding	5.2mm × 5.2mm 100 µm thick Wire width: 0.7mm Winding gap: 50µm	Copper
Bottom air gap between winding and top core layer	4µm/7µm/10µm	SiO_2 (or other insulator)
Bottom ferrite core layer	5.2mm × 5.2mm 525µm thick	NiZn ferrite Bsat=0.28T µ=100 [1]
Substrate	200 µm thick	Si

III. Simulation Results of Designed On-Chip Power Inductor in ANSYS®/MAXWELL®

Based on the dimension parameters and material property of on-chip power inductor, the 3-D physical model of the on-chip power inductor is created in ANSYS®/Maxwell® software. For the on-chip power inductor with ferrite layers, three different designs are modelled with the three different airgap values. For comparison purposes, the air core inductor (i.e., without ferrite layers) is also modelled in the software. The inductance value and saturation current can be obtained from the simulation results obtained from ANSYS®/Maxwell® software. The comparison between the modelled on-chip power inductor with different airgap values is given in Table II.

From Table II, it can be observed that the inductance value of air core on-chip power inductor is only 33.2 nH. When the two ferrite layers are added to the power inductor, the inductance value increase significantly. For example, for the case where 4µm air gap is added between each of the two ferrites layer and the winding layer, the inductance value is 253.3 nH. Compared

with the air core on-chip power inductor, this is a ~660% increase in inductance value. The saturation current in this case is ~12 A.

When the air gap between ferrite layer and winding layer is increased from 4 µm to 7 µm and then from 7 µm to 10 µm, the inductance value of the on-chip power inductor decreased. However, the saturation current of on-chip power inductor increases. For example, when the air gap is changed from 4 µm to 7 µm, the inductance value decreased from 235.3 nH to 228.7 nH (2.8% decrease) and the saturation current increased from 12 A to 13 A (8.3% increase). This is a tradeoff between inductance value and saturation current of the power inductor. The air gap of on-chip power inductor can be tuned to meet the specific requirements using this model and for this ferrite core before fabricating the new device.

The flux density distributions of bottom ferrite layer for the on-chip power inductor with ferrite layer are shown in Fig 2, Fig 3, and Fig. 4 with the three airgap values. From Fig. 2 to Fig. 4, it can be observed that the flux density of bottom ferrite layer increases with the increasing of DC input winding current. In Fig. 2, part of bottom ferrite area is red when the input winding current is 12 A. This means the flux density of ferrite layer is close to the saturation point, i.e., 0.28 T [1]. This indicates the saturation current of the on-chip power inductor with 4 µm air gap is 12 A. In Fig 3, 7 µm air gap is used in the on-chip power inductor. It can observed that the ferrite layer is saturated at 13 A. For the case where 10 µm air gap is used in the on-chip power inductor, the flux density distribution of bottom ferrite layer is shown in Fig. 4. From the results shown in the Fig. 4, the saturation current is 14 A for this case.

TABLE II
The comparison between on-chip power inductors with different configurations

		Air core	4 um air gap	7 um air gap	10 um air gap
Inductor dimensions (without substrate)		5.2mm ×5.2mm ×100µm	5.2mm×5.2mm ×1158µm	5.2mm×5.2mm ×1164µm	5.2mm×5.2mm ×1170µm
Inductance (nH)		33.2	235.3	228.7	221.6
Inductance density	(nH/mm^3)	12.3	7.51	7.27	7.00
	(nH/mm^2)	1.23	8.70	8.46	8.20
Saturation current I_{sat} (A)		-	12	13	14

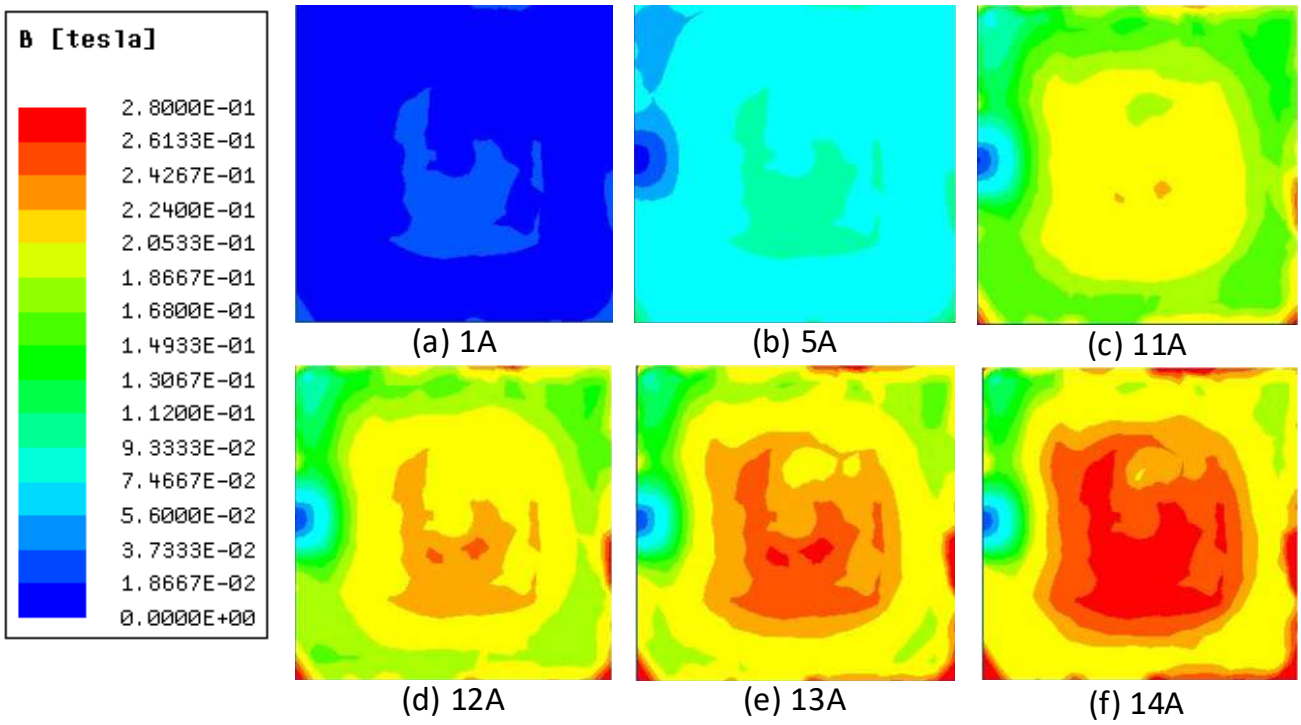


Fig. 2. Flux density of bottom ferrite layer under different DC input current values when the air gap between ferrite layer and winding layer is equal to 4 µm: (a) 1A, (b) 5A, (c) 11A, (d) 12A, (e) 13A, and (f) 14A.

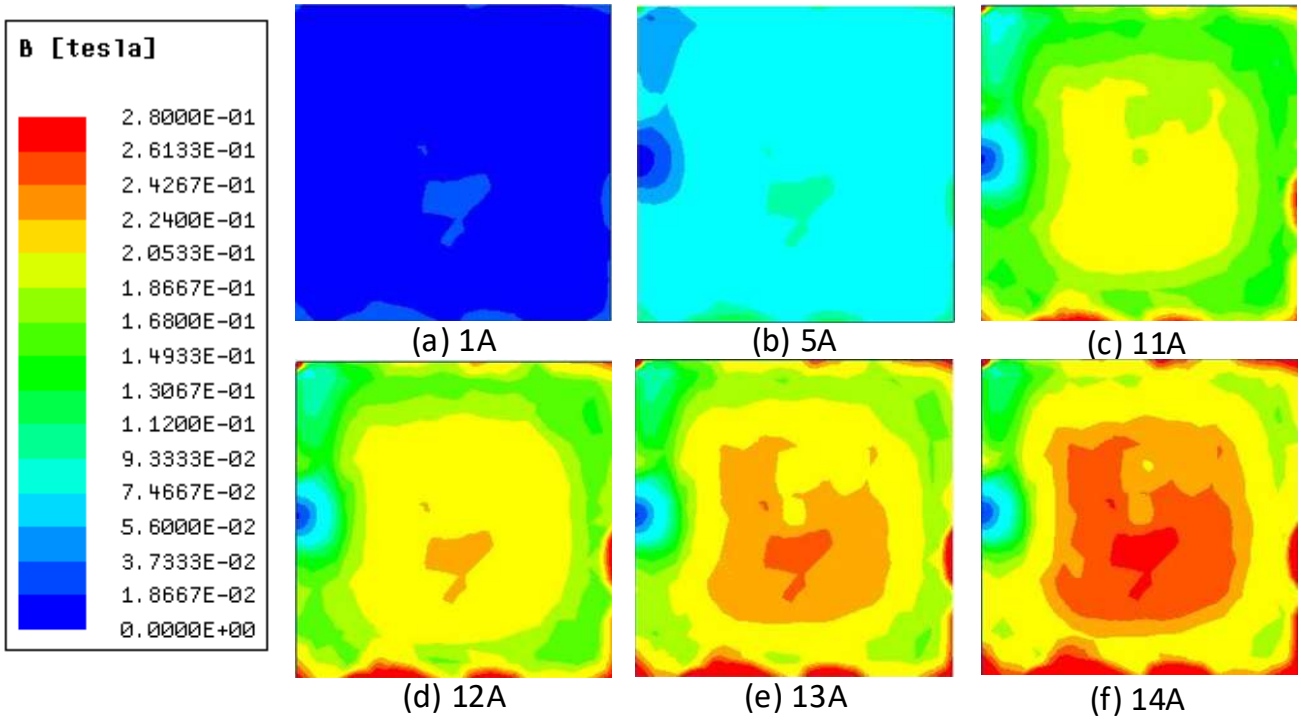


Fig. 3. Flux density of bottom ferrite layer under different DC input current values when the air gap between ferrite layer and winding layer is equal to 7 μm: (a) 1A, (b) 5A, (c) 11A, (d) 12A, (e) 13A, and (f) 14A.

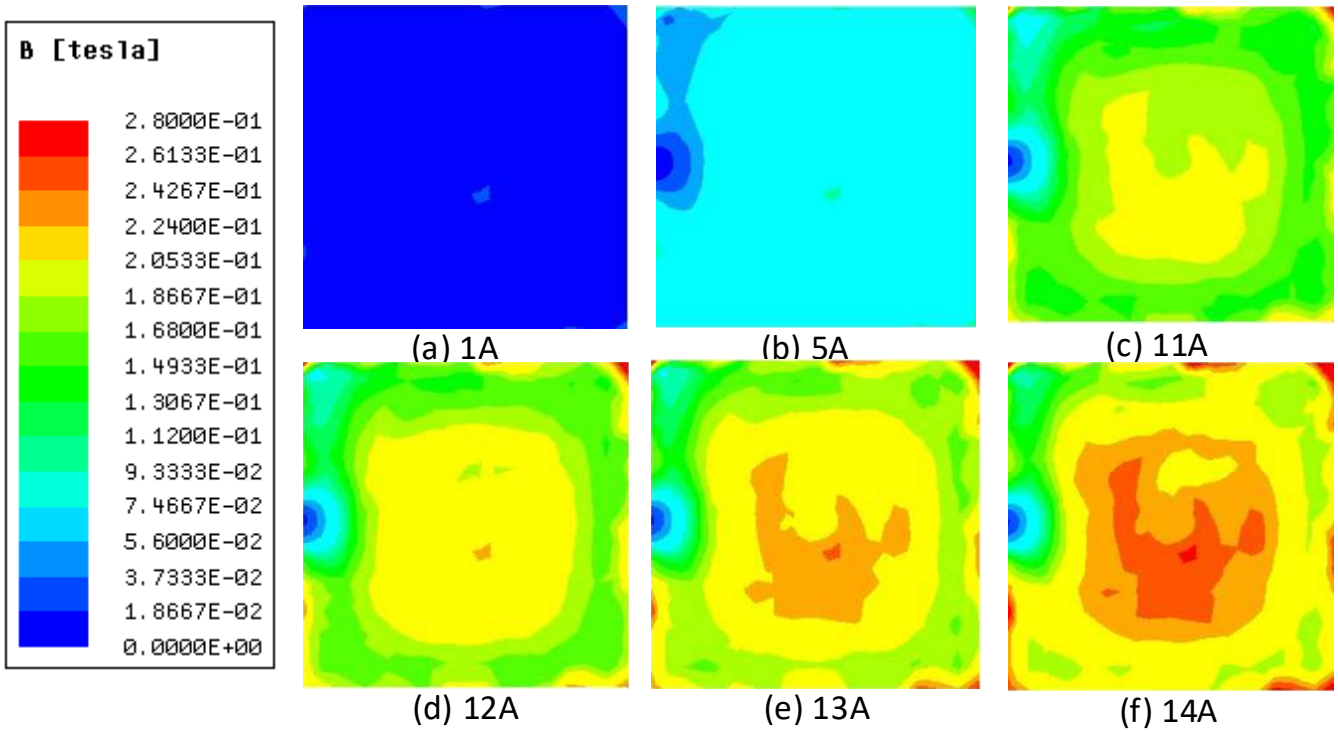


Fig. 4. Flux density of bottom ferrite layer under different DC input current values when the air gap between ferrite layer and winding layer is equal to 10 μm: (a) 1A, (b) 5A, (c) 11A, (d) 12A, (e) 13A, and (f) 14A.

IV. Conclusion

The developed 3-D physical models for on-chip power inductors are useful for design optimization of the power inductor parameters based on fabricated on-chip material before fabricating the complete on-chip device. Based on experimentally fabricated on-chip ferrite core, the developed model is used to evaluate and optimize the design of on-chip power inductor that would utilize this fabricated ferrite core. The model is used to predict the tradeoff between the inductance value and saturation current as a function of airgap which can be used as a guide before fabricating the complete on-chip power inductor device.

Acknowledgement

This material is based upon work supported in part by the National Science Foundation under Grant No. 1708690. Any opinions, findings and conclusions or recommendations expressed in this material are those of the author(s) and do not necessarily reflect the views of the National Science Foundation.

References

[1] Z. Hayashi, Y. Katayama, M. Edo and H. Nishio, "High-efficiency dc-dc converter chip size module with integrated soft ferrite," *IEEE Transactions on Magnetics*, vol. 39, no. 5, pp. 3068-3072, Sept. 2003.

[2] Z. Dang and J. A. Abu Qahouq, "Evaluation of high-current toroid power inductor with NdFeB magnet for DC–DC power converters," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 11, pp. 6868-6876, November 2015.

[3] Z. Xia, J. A. Abu Qahouq, and S. Kotru, "Evaluation of Permanent Magnet Distribution Schemes for Toroid Power Inductor with Increased Saturation Current Using 3D Physical Models," *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Anaheim, CA, USA, 2019, pp. 2894-2899.

[4] S. L. Selvaraj et al., "On-Chip Thin Film Inductor for High Frequency DC-DC Power Conversion Applications," *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA, 2020, pp. 176-180.

[5] Z. Xia and J. A. Abu Qahouq, "State-of-Charge Balancing of Lithium-Ion Batteries With State-of-Health Awareness Capability," *IEEE Transactions on Industry Applications*, vol. 57, no. 1, pp. 673-684, Jan.-Feb. 2021.

[6] Z. Dang and J. A. Abu Qahouq, "Permanent-Magnet Coupled Power Inductor for Multiphase DC–DC Power Converters," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 3, pp. 1971-1981, March 2017.

[7] J. A. Abu Qahouq and Z. Xia, "Single-perturbation-cycle online battery impedance spectrum measurement method with closed-loop control of power converter," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 9, pp. 7019-7029, September 2017.

[8] Z. Xia and J. A. Abu Qahouq, "High Frequency Online Battery Impedance Measurement Method Using Voltage and Current Ripples Generated by DC-DC Converter," *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA, 2020, pp. 1333-1338.

[9] Z. Xia and J. A. Abu Qahouq, "Method for online battery AC impedance spectrum measurement using DC-DC power converter duty-cycle control," in *APEC*, pp. 951-958, March 2017.

[10] W. Dong, S. Li, X. Fu, Z. Li, M. Fairbank and Y. Gao, "Control of a Buck DC/DC Converter Using Approximate Dynamic Programming and Artificial Neural Networks," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 68, no. 4, pp. 1760-1768, April 2021.