Highly Efficient Rectifier And DC-DC Converter Designed in 180 nm CMOS Process for Ultra-Low Frequency Energy Harvesting Applications

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***Abstract*—This paper presents the integration of an AC-DC rectifier and a DC-DC boost converter circuit designed in 180 nm CMOS process for ultra-low frequency (<10 Hz) energy harvesting applications. The proposed rectifier is a very low voltage CMOS rectifier circuit that rectifies (converts AC voltage into DC voltage) the low-frequency signal of 100 -250 mV amplitude and 1-10 Hz frequency into DC voltage. In this work, the energy is harvested from the REWOD (Reverse Electrowetting-On-Dielectric) generator, which is a Reverse Electrowetting technique that converts mechanical vibrations to electrical energy. The objective is to develop a REWOD based self-powered motion (such as walking, running, jogging, etc..) tracking sensors that can be worn on hand or ankle, thus harvesting energy from the regular activities. To this end, the proposed circuits are designed in such a way that the output from the REWOD is rectified and regulated using a DC-DC converter which is a 5-stages of a cross-coupled switching circuit. Simulation results show a voltage range of 1.1 V-2.1 V i.e., 850-1200 % (VCE (Voltage Conversion Efficiency) and 30 % (PCE (Power Conversion Efficiency) for low input frequency signal 100 - 250 mV in the low-frequency range. This performance verifies the integration of the rectifier and DC-DC boost converter which makes it highly suitable for various motion-based energy harvesting applications.**

***Index Terms*—CMOS, energy harvesting, low-frequency, Rectifier, DC-DC boost converter, Charge pump, reverse electrowetting-On-Dielectric (REWOD).**

I. Introduction

In literature for the voltage rectification and DC-DC boosting with no external supply, there are many techniques. Firstly discussing [1], it explains Energy is harvested from the REWOD generator, REWOD configuration defined as Mechanical force applied to either the bottom or top electrodes squeezes the electrolyte, periodically increasing and decreasing the effective interfacial area and generating alternating current and that unconditioned REWOD output of 95-240 mV AC is generated using a 50 μL droplet of 0.5M NaCl electrolyte and 2.5 mm of electrode displacement from an oscillation frequency range of 1-3 Hz. This work uses COTS (Commercial Off-The-Shelf components) which involves the integrated circuit design of the CMOS process, make it a highly miniaturized system. 135-240 mV and a forward current of 1 mA convert the generated AC signal to DC voltage. 3 V DC is measured at the boost converter output, proving the system could function as a self-powered motion sensor.

For another approach, consider a full-wave rectifier or bridge rectifier consists of p-n junction diodes, which is not suitable for very low input voltage, as they require 0.7 V forward bias voltage to conduct. Similarly, for DC-DC converter the Dickson charge pump is one of the most popular architectures that is used as a DC-DC boost converter but the input voltage needs to be high because of the forward voltage requirement of traditional diodes. Hence, Cross-coupled switched-capacitor circuits are better for low input voltage boosting[2]. For a rectifier, the highly efficient voltage-boosting rectifier has a wider frequency operation range of 10 kHz – 100 MHz. The designed rectifier by Suri achieved a power conversion efficiency (PCE) of 51% with 100 mV @ 7.25 MHz input signal, which makes it highly applicable for the inductive-coupling based wireless power transfer applications for implantable sensors[3]. Jingmin et al. showed [4] it achieves very high efficiency of 95.5% at 0.2 V @ 100 Hz. The proposed technique by et al uses DTMOS, for which the body terminal is connected to the gate in a diode-connection form. This factor helps in rectifying the input voltage with wider dynamic control over the threshold voltage. Not only the frequency of the input signal but also the start-up voltage plays a major role in the efficient operation of the circuit. Huan Peng in [5] proposed a charge pump circuit designed in a standard 0.18 μm CMOS process. It consists of 6 stages, each with a 24 pF pumping capacitor the minimum start-up required is 350 mV output voltage rise from 0 to 2.04 V within 0.1 milliseconds, making it not suitable for input voltage amplitude of 100 mV. A similar problem can be observed for the work present in [6], where the PCE dropped by more than 50% when the input voltage is reduced from 500mV to 220mV. But at 500 mV the VCE and PCE are 90% and also for this design, the minimum operating voltage is 380 mV. Similarly, for the DC-DC voltage booster, the charge pump circuit is used to regulate the output DC voltage. Apart from that, Buck-Boost converters are also a better technique for DC-DC conversion. An Inductorless DC-DC Converter is used for micro-power harvesting, it provides output regulation at 1.4V with 58 % efficiency but, the minimum input voltage for this design is

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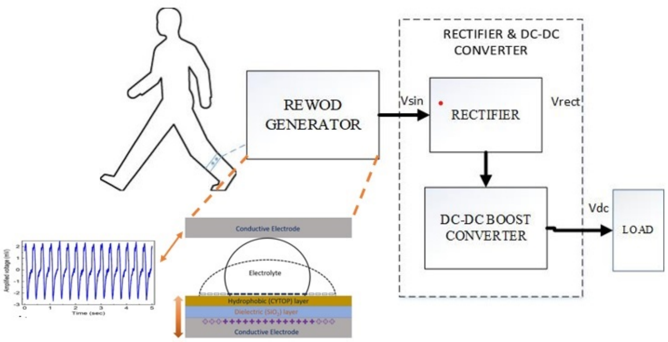

Fig. 1: Block diagram for proposed energy harvesting circuitry

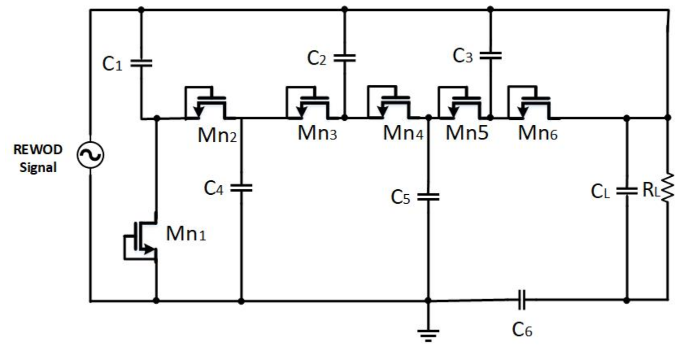

Fig. 2: Proposed boost rectifier

270 mV.

This paper is arranged as follows: Section II discusses the design of rectifier and DC-DC boost converter, Section III presents the simulation results with a comparative analysis and a summary, Section IV and Section V provided Conclusion and Acknowledgement respectively.

II. DESIGN ARCHITECTURE

The AC signal harvested from the REWOD generator for human motion activities such as walking and running is of very low frequency (1 - 10 Hz) and amplitude (95 - 240 mV). The low-frequency signal needs to be rectified and the rectified DC voltage (V_{rect}) needs to be boosted to a certain constant voltage using pump circuits or converters according to the system requirement without using any external sources. The major contributions of the paper are the rectifying and voltage boosting circuitry designed for the signal generated by the REWOD energy harvester. The main challenge for the design is that the entire circuit should not have any external supply voltage, to make the transducer and the circuit completely self-powered.

A simple block diagram is shown in Fig- 1 for a better understanding of the concept. As shown in the block diagram in Fig- 1, the REWOD generator generates current as the person walks/runs, which is provided as an input to the rectifier and DC-DC voltage booster circuit. REWOD has been demonstrated to effectively generate electrical current proportional to the displacement at the low-frequency range of 1-10 Hz, which is the frequency range for various physical activities of a human being such as running, jogging, walking, etc. Output that captured in the REWOD generator is given to the AC-DC boost rectifier as an input. The following sub-sections present the design architecture of the proposed rectifier and DC-DC voltage converter circuits.

a) Rectifier: This is a transistor-level implementation using NMOS transistors. With the help of cross-coupling capacitors the design circuit will convert AC to DC voltage. The output from the REWOD generator is provided as an input to the rectifier. The AC voltage signal generated by the REWOD is around 100 - 250 mV with a frequency range of 1-10 Hz. As discussed in the previous section, a bridge rectifier or any other diode-based rectifiers will not be suitable for this signal as the output from the REWOD generator is as low as 100 mV and the diode will only conduct at $700mV(0.67V$ in exact) voltage. So, using MOSFET's with cross-coupling capacitors are used in the design. The circuit is shown in Fig- 2 consists of all NMOS transistors where positive and negative peaks of the input AC signal are rectified by the circuit. The circuit is a 3-stage boost rectifier each stage of the circuit is for better smoothening and boosting the signal. When the output from the REWOD generator is given to the rectifier then the capacitor C_1 will discharge to M_{n2} and similarly C_4 discharge to M_{n3}, in this way both positive and negative peaks are rectified and during every stage, the output is boosted. With the help of a 180 nm CMOS process using the ideal capacitance of 1 nF and NMOS transistors of Length (L) is 180 nm and width (W) is 220 nm with a load resistance of 10 Mohm according to the current requirement, the circuit is designed. More stages can also be added but by increasing more components the power consumption with-in the circuit increases. So, 3-stages is the best for better output. Thereafter, that rectified voltage from the rectifier (Vrect) is provided to the 5-stage DC-DC voltage booster.

b) DC-DC Booster: The circuit shown in Fig- 3 is a voltage

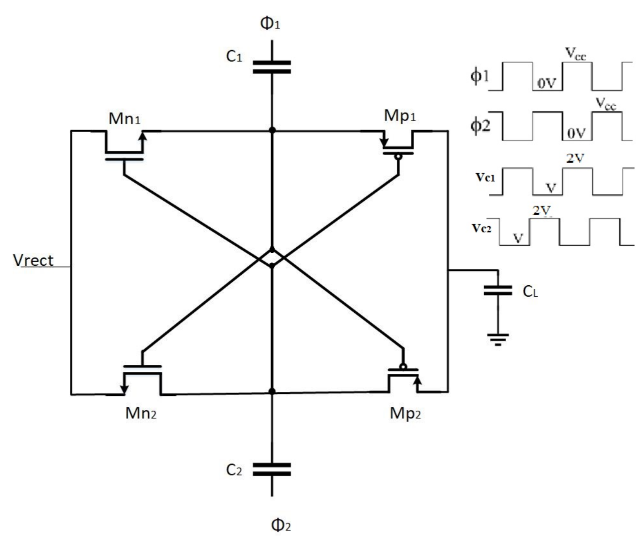

Fig. 3: DC-DC Booster

doubler circuit or a charge pump. So, adding multiple stages of this circuit and gain our required output DC voltage. The main objective of the circuit is to reduce the power consumption by the transistors so, taking low L and W values will result in high efficiency during the output. In this design 5-stages of Cross-coupled switched capacitor are cascaded and It is implemented using CTS (NMOS charge transfer switches) technique where it is designed by using four MOSFETs and two transfer capacitors in each stage. Each stage is made of two latched CMOS pairs (M_{n1}, M_{p1}, M_{n1}, M_{p1}). The transfer capacitors of each stage are alternately charged to the voltage of the previous stage and then boosted by Vrect to charge the next stage at a higher voltage.during the first half cycle when ϕ_1 is high (ϕ_2 is low) transistors (M_{n2}, M_{p1}) are ON (V1= V_{ϕ_1}, V2=0), and transistors (M_{n1}, M_{p2}) are OFF, transfer capacitor C1 is charged to Vin through N2, while transfer capacitor C2 is boosted to Vrect +V_{ϕ_1} through M_{p1}. During the second half cycle, transistors (M_{n1}, M_{p2}) are turned ON, and transistors (M_{n2}, M_{p1}) are turned OFF, transfer capacitor C2 is charged to Vin, while transfer capacitor C1 is boosted to charge next stage to V_{ϕ_1} + Vrect. Once NMOS (M_{n1}) has enough gate-source voltage then PMOS (M_p2starts charging and similarly for M_{n2} and M_{p2}. thereby, the output transfers to the next stage. The clock frequency used in the design is 1k Hz with default transistors.

III. Simulation Results

The simulation results of the rectifier and the DC-DC converter circuit are discussed in this section. Fig- 4 presents the simulation results between V_{out} vs V_{in} of the rectifier. As can be seen from the figure, the output voltage boosts the input voltage linearly at frequency range of 1 - 10 Hz. The minimum voltage to conduct this circuit is 80 mV and output voltage at 80 mV is 190 mV.
The Fig- 5 is the plot between voltage conversion efficiency vs. input voltage at different frequencies from 1-10Hz.
In the same figure, the plot lines are voltage conversion efficiency for 2Hz, 4Hz, 6Hz, 8Hz, 10Hz frequencies respectively with an input voltage range of 100 mV - 250 mV.

$$VCE_n = \frac{V_{out_n}}{V_{in}} \times 100\% \tag{1}$$

Where V_{out_n} is the output voltage at different frequencies, V_{in} is the input voltage and equation (1) is the formula for the voltage conversion efficiency. It is used in the calculation after the results are obtained from the simulation. The results are shown in Fig-5. It can be observed that when input voltage increases the voltage conversion efficiency increases with respect to the input frequency. Efficiency is directly proportional to the input frequency. So, from the fig- 5, at higher input voltage of 250 mV @ 10 Hz, the voltage conversion efficiency is nearly 400 %.

From the Fig- 6, we can observe the power conversion efficiency vs P_{in} of the rectifier. At 250 mV @ 10 Hz frequency the PCE is 15%. The figure is plotted between different input voltages at different frequencies. To achieve

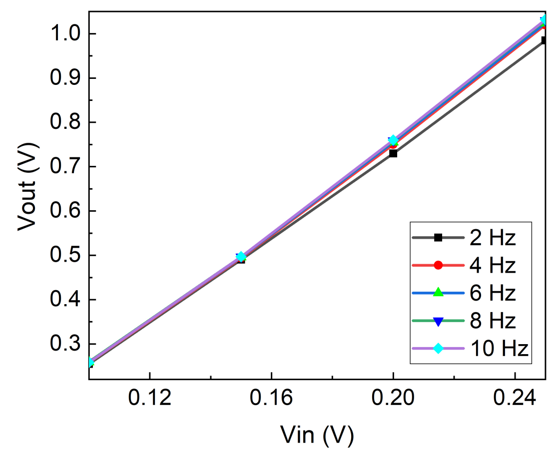

Fig. 4: V_{out} vs V_{in} for the proposed rectifier

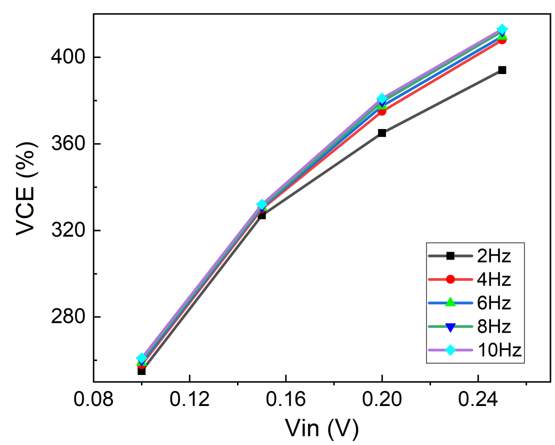

Fig. 5: Voltage conversion efficiency vs. input voltage of the proposed rectifier

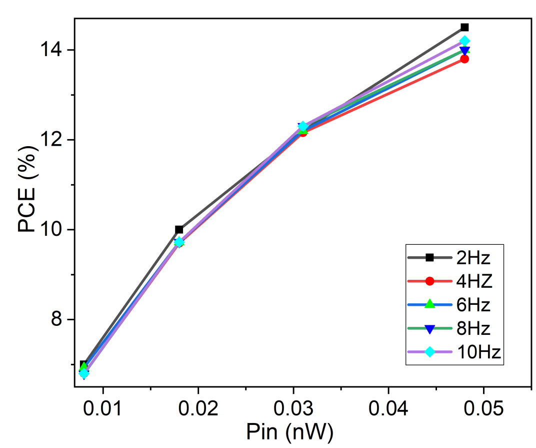

Fig. 6: PCE vs. P_{in} of the proposed rectifier

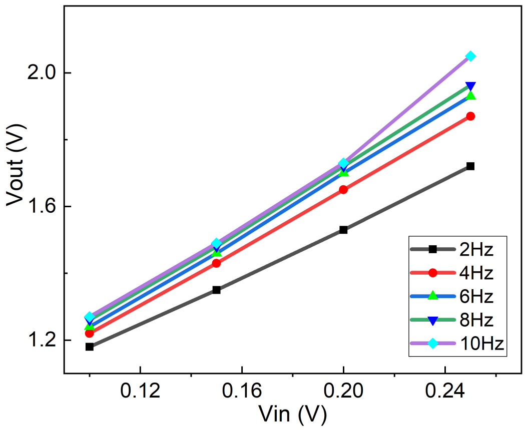

Fig. 7: V_{out} vs. V_{in} for the DC-DC boost converter

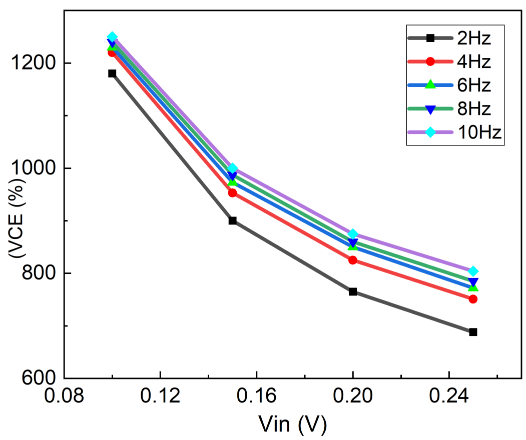

Fig. 8: VCE vs. Vin of both rectifier and DC-DC boost converter

more power efficiency, Schottky diode is used instead of MOSFET's to gain some more power.

In the Fig- 7 it is clear that at $100mV$ of AC the output DC voltage is 1.18 V. Increasing the input voltage linearly increases the output DC voltage. The conversion rate is as shown in Fig 8. The Fig- 8 is the plot between Voltage conversion efficiency vs. input AC voltage (100 - 250 mV) from the REWOD. At 250 mV @ 10 Hz of the frequency, the average output DC voltage is 2.1 V, which is high enough to be used as a supply voltage for the load. Along with the output voltage the power conversion efficiency is also very important.

$$PCE_n = \frac{P_{out_n}}{P_{in}} \times 100\% \quad (2)$$

The above equation (2) represents the power conversion efficiency at different frequencies(n). Fig- 9 shows the plot between power conversion efficiency(P_{out}) and input power(P_{in}). The graphs represent the power efficiency for 2 - 10 Hz frequency range for the corresponding input according to Vin range of 100 - 250 mV. From the observation both VCE and PCE, It is evident that at 100 mV input with 2 Hz frequency both VCE and PCE efficiencies are 840% and 30% respectively.

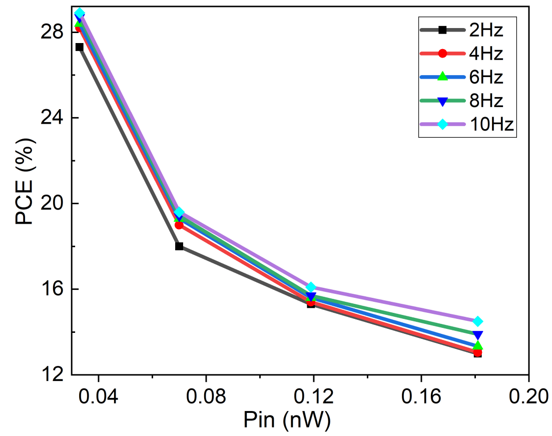

Fig. 9: PCE vs. Pin for rectifier and DC-DC boost converter

TABLE I: summarise the performance summary and comparisons of this work rectifier and charge-pump and the state-of-the-art designs.The charge pump in [8] and [9] cannot operated at very low voltage. However, they are fabricated in 130 nm CMOS process. The boost converter in [7] is having less power efficiency and also the operating voltage is also more. Rectifier used in [4] is operated with very high efficiency at low voltage. However, it is not used as boost rectifier. Considering the overall performance the proposed circuit achieves the low voltage operation with effective output efficiency.

IV. Conclusion

Using 180 nm CMOS technology standards a 3-stage boost rectifier and a 5-stage DC-DC boost converter are designed. As part of the work a very-low AC voltage of 100mV is converted and boosted into 1.2 V DC voltage and 250 mV of AC voltage input is converted into 2.1 V DC voltage, validating the design approach in terms of efficiency and optimization. Hereby, the self-generated current from the REWOD generator is effectively converted and boosted into appropriate DC voltage which is applicable for various harvesting circuits.

V. ACKNOWLEDGEMENTS

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References

[1] P. R. Adhikari, N. T. Tasneem, D. K. Biswas, R. C. Reid, and I. Mahbub, "Reverse electrowetting-on-dielectric energy harvesting integrated with charge amplifier and rectifier for self-powered motion sensors," in *ASME 2020 International Mechanical Engineering Congress and Exposition*, 2020.

TABLE I
Performance summary and comparisons

Ref, Year	**Mechanism**	**Start-up voltage** (mV)	**Input voltage** (mV)	**Output voltage**	**VCE**	**PCE**	**Process** (nm)
[7], 2015	Boost converter	300	300	1.1V	367%	39%	180
[3], 2019	Boost Rectifier (10k-100MHz)	200	200	2.03V	1015%	51%	130
[4], 2016	Rectifier (10Hz-1kHz)	200	200	181 mV	90.5%	90.5%	180
This work	Booster & Rectifier(1-10Hz)	100	100	1.2V	1180%	29%	180
This work	Booster& Rectifier(1-10Hz)	100	250	2.1V	840%	15%	180

[2] A. Ballo, A. D. Grasso, and G. Palumbo, "A review of charge pump topologies for the power management of iot nodes," *Electronics*, vol. 8, no. 5, p. 480, 2019.

[3] R. S. Suri, N. T. Tasneem, and I. Mahbub, "Low-power highly efficient voltage-boosting rectifier for wide-band inductively-coupled power telemetry," in *2019 United States National Committee of URSI National Radio Science Meeting (USNC-URSI NRSM)*. IEEE, 2019, pp. 1–2.

[4] W. Jingmin, Y. Zheng, Z. Zhangming, and Y. Yintang, "An ultra-low-voltage rectifier for pe energy harvesting applications," *Journal of Semiconductors*, vol. 37, no. 2, p. 025004, 2016.

[5] H. Peng, N. Tang, Y. Yang, and D. Heo, "Cmos startup charge pump with body bias and backward control for energy harvesting step-up converters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 6, pp. 1618–1628, 2014.

[6] C. Peters, J. Handwerker, D. Maurath, and Y. Manoli, "A sub-500 mv highly efficient active rectifier for energy harvesting applications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 7, pp. 1542–1550, 2011.

[7] H. Hernández and W. Van Noije, "Fully integrated boost converter for thermoelectric energy harvesting in 180 nm cmos," *Analog Integrated Circuits and Signal Processing*, vol. 82, no. 1, pp. 17–23, 2015.

[8] Y.-C. Shih and B. P. Otis, "An inductorless dc–dc converter for energy harvesting with a 1.2-muw bandgap-referenced output controller," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 58, no. 12, pp. 832–836, 2011.

[9] C. Ulaganathan, B. J. Blalock, J. Holleman, and C. L. Britton, "An ultra-low voltage self-startup charge pump for energy harvesting applications," in *2012 IEEE 55th International Midwest Symposium on Circuits and Systems (MWSCAS)*. IEEE, 2012, pp. 206–209.