Massive-MIMO and Digital mm-Wave Arrays on RF-SoCs using FDM for M-Fold Increase in Antennas per ADC/DAC

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***Abstract*—Communication systems of the future will require hundreds of independent spatial channels achieved through dense antenna arrays connected to digital signal processing software defined radios. The cost and complexity of data converters are a significant concern with systems having hundreds of antennas. This paper explores frequency division multiplexing as an approach for augmenting the baseband signals of multiple antenna channels such that a single ADC can sample a multitude of antennas in an array. The approach is equally applicable to both massive MIMO and mm-wave digital wireless arrays. An example design based on Xilinx RF SoC for combining 4 antenna channels at 28 GHz into a single ADC is provided.**

I. Introdction

Emerging mm-wave, 5G and/or holographic/massive multi-input multi-output (MIMO) based wireless systems [1]–[3] share a common requirement of a large number of independent radio-frequency (RF) channels corresponding to individual antenna elements [4]–[6]. Conventional approaches based on analog-digital hybrid beamforming, for example, allow beamsteering over large numbers of elements while reducing the number of analog to digital (ADC) (and/or digital to analog converters (DACs)); however, hybrid approaches based on analog phased-array front-ends reduce the degrees of freedom available to the digital communication system by $M-$ fold, where M is the number of antennas combined in analog domain before being digitized using a single ADC, for example in [7].

The advent of radio-enabled digital hardware platforms, e.g., the Xilinx RF system on chip (SoC) technology, allows the combined realization of programmable digital fabrics with high-speed ADC/DAC on the same chip [8]. An RF SoC platform such as Xilinx ZCU 1275 shown in Fig. 1 (a), contains 16 high-speed ADCs (2 GS/s) and 16 high-speed DACs (6 GS/s) on the a field programmable gate array (FPGA) chip. Although such state-of-art RF SoCs support only upto 16 channels, the bandwidth per DAC channel can be up to 3 GHz. Time division multiplexing (TDM), code-division multiplexing (CDM) [9], [10] and frequency-division multiplexing (FDM) are techniques for combining multiple independent analog baseband streams into a single DAC/ADC for sampling. Analog TDM can suffer from switching artifacts, and CDM requires M unique modulation waveforms for coded down-conversation and sampling.

Interestingly, many wireless communication systems have relatively small channel bandwidth, for example 150-800 MHz for 28 GHz 5G systems, that raises the question, "can we trade ADC bandwidth in favor of increasing the number of channels?". For example, if each ADC supports 2 GHz of bandwidth, can we multiplex 20 independent antenna signals at 100 MHz per channel into a single ADC, thereby supporting up to 320 antenna channels on a single RF SoC chip? This paper explores this idea using Xilinx RF SoC ZCU 1275 (supports 16 ADCs and 16 DACs on a single FPGA chip) by FDM using four independent channels at 28 GHz into an ADC. That is, for $M = 4$ we design a system that increases the number of supported independent RF antennas by a factor of 4 for an RF SoC device.

II. Design of an FDM Array Receiver

The proposed system will employ FDM for M antenna signals into an IF channel where each receiver is frequency translated to a known center frequency. In the discrete domain, sampled FDM multiplexed (baseband) signals are split into their corresponding channels using sub-band filtering methods. The filters are implemented using a polyphase finite impulse response (FIR) perfect-reconstruction filterbank [11]. A variety of filter topologies can be utilized for signal recovery.

A. Microwave Circuits for FDM

A bank of M phase- and frequency-locked oscillators are used to frequency translate inputs at known

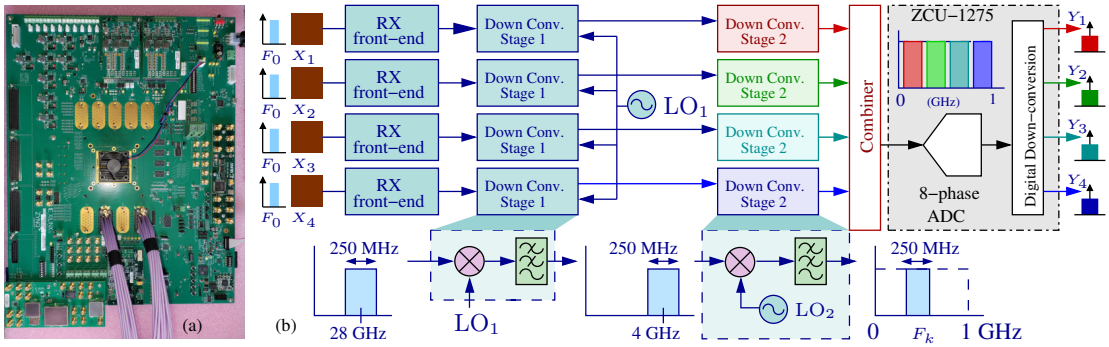

Fig. 1. (a) Xilinx RFSoC ZCU1275. (b) Overview of F_0 = 28 GHz, 240 MHz/channel 4-element FDM array receiver.

frequency offsets. This FDM architecture is shown in Fig. 1 (b). These oscillators will be synchronized using a stable low-jitter reference clock via a bank of integer-N frequency synthesizers. In our example, we assume a double-sided signal bandwidth of $B = 240$ MHz per receiver, and $M = 4$ antenna elements, each designed for 28 GHz operation. The double-sided bandwidth of 4 frequency multiplexed channels with a 10 MHz guard band per channel is therefore 1 GHz. The RF channels having 240 MHz of bandwidth and centered at 28 GHz are uniformly down-converted in stage 1 to a fixed intermediate frequency (IF) of 4 GHz.

In a second-stage, the IF signals are down-converted to the required IF for sampling, centered at $F_k = 250k - 125$ MHz, where $k = 1, 2...M$. Local oscillator (LO) frequencies of 3.125, 3.375, 3.625, and 3.875 GHz are then applied to each of the antennas respectively to translate the received signals to 875, 625, 375, and 125 MHz center frequencies. These IF components are fed into a combiner to create the FDM signal. Note that the FDM "baseband" can be sampled using a single ADC and the subsequent digital signal can be filtered, down-converted, and subjected to a Hilbert transform to obtain the quadrature component. The inter-band frequency guardbands B_g are needed for accommodating finite order FIR filtering in the digital domain and are 10 MHz wide. The output from this second stage analog down-conversion is fed to the ADC and sampled at $F_s = 2$ GHz Nyquist sampling rate.

B. DDC and FIR Filtering

Fig. 2 (a) shows the sampled spectrum showing 4 FDM channels each having a 250 MHz bandwidth including guard bands. Simulations have used a combination of 32 tones with $240/32 = 7.5$ MHz space to generate the wideband signal, such that $\sum_{n=1}^{16} \cos(2\pi(F_k \pm 7.5n)t)$ for $k = 1, 2, 3, 4$. Digital down conversion (DDC) leads the aliased image components to fall back into the same Nyquist zone. Highly-selective FIR low-pass filters of order 70 were applied to filter out the image components from each of the antenna spectra. The simulation of DDC shows the filtered spectrum in Figs. 2 (c-f).

C. Experimental Verification

A 4-element array was designed to operate in the frequency range 27.5-28.35 GHz. For experimental validation, a tone was transmitted at 28 GHz and the antenna array was used to receive the signal at a DOA of 0^o. The down conversion stage 1 for each of the 28 GHz antennas are using Analog Devices EVAL01-HMC1065LP4 [12] modules containing the HMC1065 chips. Each EVAL01-HMC1065LP4 RF receiver contains an internal frequency doubling circuit in the LO path of the first down-conversion stage. A Valon 5015 frequency synthesizer was used to generate the first LO signal of 12 GHz, yielding an LO of 24 GHz. The 4 GHz centered IF signals resulted from mix-down operation are low pass filtered for image-rejection and noise suppression, and passed to the second down-conversion stage shown in Fig. 3 (a). Two Valon 5009 frequency synthesizers were used to generate the four LO frequencies that are needed for stage-2 down-conversion.

After the second down-conversion stage, outputs are combined and sampled using an RF-SoC ADC at 2 GS/s. The sampled signal is shown in Fig. 2 (f). Xilinx ZCU-1275 was used to sample the input, DDC and FIR filtering. Since the digital hardware is designed to run using a 250 MHz clock, samples at 2 GS/s were processed using a 8-phase multirate DSP implementation. Samples arriving from the ADC were then digitally down-converted to 25 MHz and then lowpass filtered to retrieve the original spectra shown in Fig. 3 (b-e).

III. Conclusion

FDM is used at the receiver to reduce ADC requirement. The proposed architecture was verified for Xilinx ZCU-1275 RF-SoC using a 4-element, 28 GHz antenna array system and samples were analyzed using MATLAB. The proposed system can achieve a factor of 4 in ADC reduction at a cost of the received spectrum getting

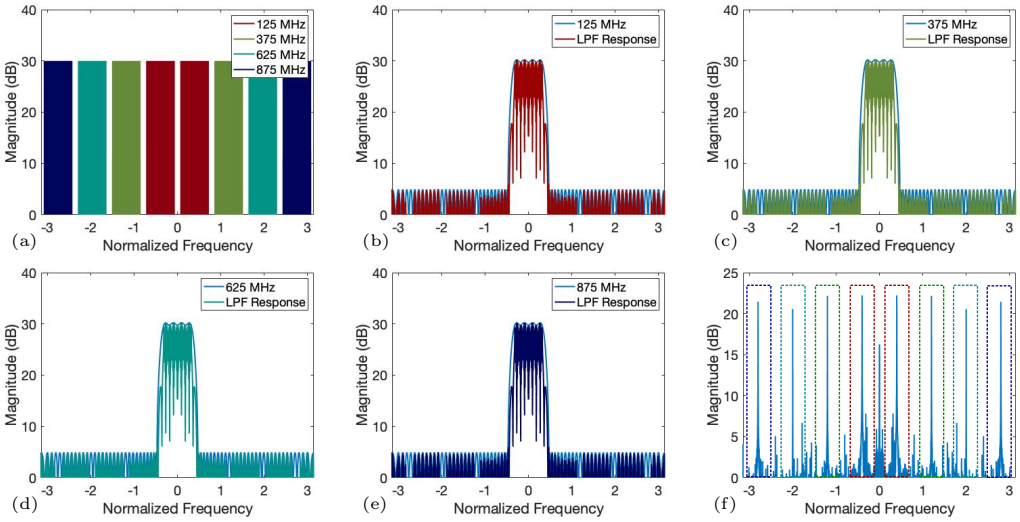

Fig. 2. (a) Combined output from the second stage analog downconversion fed to the ADC. Digital downconversion and filtering for narrowband signals centered at (b) 125 MHz, (c) 375 MHz, (d) 625 MHz, and (e) 875 MHz. (f) Received signal sampled by RFSoC.

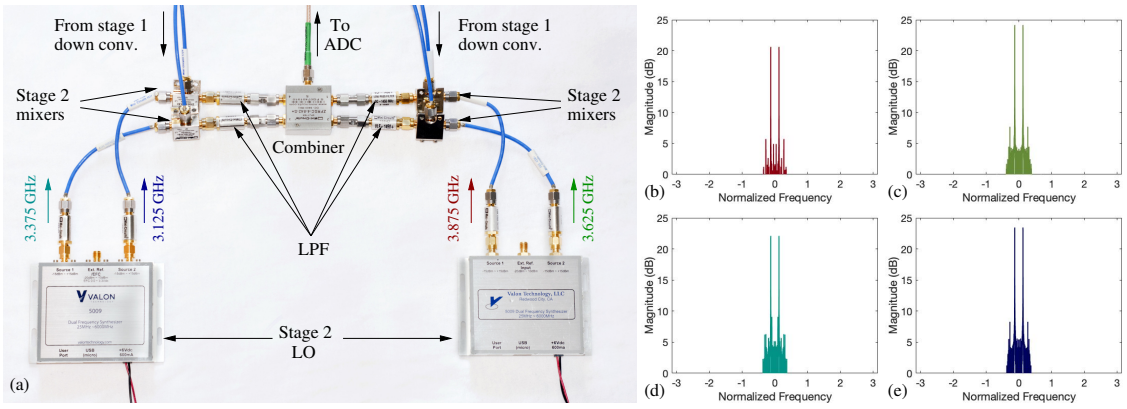

Fig. 3. (a) Down conversion stage 2 setup for 4 element, 28 GHz antenna array. Retrieved carrier signals digitally down converted to 25 MHz.

affected by the nonlinearities of the system (signal to interference and noise ratio about 15 dB). Therefore, appropriate steps are required to avoid intermodulation products and harmonics from aliasing into the signal spectrum.

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