A 27 Gb/s 5.39 pJ/bit 8-ary Modulated Wireline Transceiver Using Pulse Width and Amplitude Modulation Achieving 9.5 dB SNR Improvement over PAM-8

Mohamed Megahed, Yusang Chun, Zhiping Wang, and Tejasvi Anand
Oregon State University, Corvallis, OR 97331, USA, Email: megahedm@oregonstate.edu

Abstract

This paper presents a novel 8-ary modulation technique with higher SNR compared to the PAM-8. The proposed modulation (SNR-Enhanced), modulates the pulse width and amplitude to achieve an average SNR improvement of 9.5 dB over PAM-8 in the near-end eye at the cost of 8.2% reduction in the horizontal eye margin. Using 3-tap FFE and CTLE, the proposed transceiver achieves 1×10^{-7} BER at 9 dB channel loss with an efficiency of 5.39 pJ/bit in the 65 nm CMOS process.

Keywords: PAM-8, wireline, SNRE-8, transceiver, I/O.

Introduction

The emergence of artificial intelligence and big data workloads has pushed the wireline data rates to 112 Gb/s and beyond. As a result, wireline transceivers are facing two simultaneous challenges: (a) higher baud rate, and (b) higher channel loss, which results in high power consumption. While moving from NRZ to PAM-4 has helped to double the data rate without increasing the baud-rate, data rates beyond 224 Gb/s may require employing even higher-order modulations such as PAM-8 [1] or PAM-16. Higher-order modulations suffer from SNR reduction; moving from NRZ to PAM-4 reduces the SNR by 9.5 dB and moving from NRZ to PAM-8 reduces the SNR by16.9 dB. In addition to the SNR reduction, higher-order modulations also suffer from increased ISI sensitivity. While techniques such as sequence encoding can achieve up to 5.26 dB SNR improvement in PAM-4, it comes at the cost of overhead on data-rate and large latency [2]. In view of these limitations, we propose an 8-ary modulation scheme with improved SNR and ISI sensitivity compared to the PAM-8 modulation. The proposed modulation can achieve an average of 9.5 dB better SNR in near-end eyes compared to PAM-8 at the cost 8.2% smaller horizontal eye margin while operating at 27 Gb/s. Due to improved SNR, we call the proposed modulation SNR enhanced (SNRE) modulation. The proposed SNRE-8 transceiver can achieve BER of 1×10^{-7} at 27 Gb/s with 5.39 pJ/bit power efficiency in the 65 nm CMOS.

Proposed SNR Enhanced-8 (SNRE-8) Modulation

PAM-8 is generated by modulating the amplitude of the signal, which results in a smaller vertical opening (Fig. 1). PWM [3] is generated by modulating the phase of the signal, which results in a smaller horizontal opening, making PWM more susceptible to jitter. The proposed SNRE-8 modulates the signal in both voltage and phase domain in such a way that it results in a larger vertical margin than PAM-8 and a larger horizontal margin than PWM-8 (Fig. 1). A larger vertical margin translates to higher SNR. In PAM-8, peak-to-peak signal transition reduces the horizontal eye margin. In SNRE-8, the signal resets to the common-mode voltage after every UI, and therefore, does not degrade the horizontal eye margins. As a result, despite modulating the signal in time, the SNRE-8 still shows a comparable horizontal opening compared to PAM-8. Theoretically, the proposed SNRE-8 has a 1.75× lower ISI sensitivity (define as V_{MAX}/V_{MIN}) as compared to PAM-8 (Fig. 2). This results in reduced equalization requirements.

The SNRE-8 modulated signal is generated by employing the frequency-dependent loss of the communication channel (Fig. 3). A wide pulse has a narrow-band spectrum, and when it is transmitted on a lossy channel, it suffers from small amplitude loss. Alternatively, a narrow pulse has wide-band spectrum and suffers from higher amplitude loss when transmitted on the same channel. This property of the channel which converts a phase modulated (PM) signal at the input to an amplitude modulated (AM) signal at the output is leveraged for SNRE-8 generation. Instead of generating narrow pulses in the transmitter, which can be power inefficient, the phase of two clock signals is differentially modulated and transmitted on two wires (channel). By carefully selecting the modulation time ($\Delta T_{1\text{-}4}$) and modulation position, the desired width and amplitude of the output pulse corresponding to different eyes of SNRE-8 signal can be obtained at the receiver.

SNRE-8 Transceiver Architecture

The transmitter consists of a PRBS generator, 32-to-2 mux followed by a decoder and delay blocks to modulate the rising and falling edges of two clock signals (Fig. 4). The rising and falling edge modulation of clock signals are performed by changing the pull-down strength of the clock buffer. Both I and Q phases of the clocks are modulated simultaneously to support a wide range of phase modulation, these phases are then combined at the end using an edge combiner circuit. The rising and falling edge modulator also consists of a 3-tap time-domain FFE. The receiver consists of 2-CTLEs and 2 amplifier stages in the front-end followed by half-rate slicers, resynchronizers, and the decoding logic. Digitally controlled delay lines (DCDL) are used on the clock path to generate different sampling phases required for the SNRE-8 modulated data.

Measurement Results

The proposed SNRE-8 transceiver was fabricated along with a conventional PAM-8 transmitter on the same die in 65 nm CMOS. Both SNRE-8 and PAM-8 transmitters are measured with same output driver supply and on the same channels with measured loss shown in Fig. 5. By comparing the near-end (channel 1) average eye heights and widths, the SNRE-8 achieves a 9.5 dB SNR gain at the cost of 8.2% eye width degradation (Fig. 6). Far-end (channel 2) measurement shows that without FFE the PAM-8 eyes are completely shut but SNRE-8 still has open eyes, which demonstrates the reduced ISI sensitivity of SNRE-8. The measured bathtub plot of SNRE-8 transceiver on channel 3 shows that BER of 1×10^{-7} can be achieved (Fig. 5). The power breakdown of the SNRE-8 transceiver, PAM-8 transmitter and die micrograph are shown in Fig. 7. Compared to the PAM-8 transmitter, the SNRE-8 transmitter power overhead is 23%. A comparison with the state-of-the-art is shown in Table 1. Compared to [2] the proposed system achieves 4.24 dB more SNR gain with no overhead on the data-rate.

Acknowledgements This work was supported by CDADIC and NSF grant number 2003015.

References

[1] Y. Chun, *ESSCIRC*, 2019, pp. 269-272. [2] Aurangozeb, JSSC, 2020, pp. 27-37. [3] W. Chen, JSSC, 2001, pp. 1498-1505.

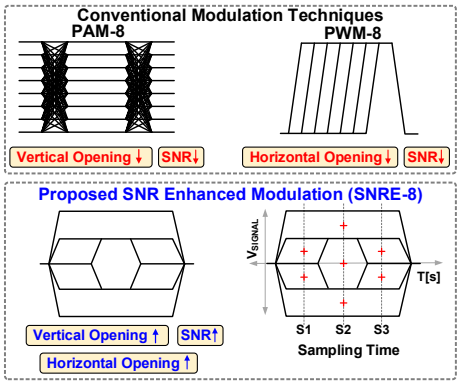

Fig. 1 Comparison between PAM-8, PWM-8 and the proposed SNRE-8 modulation.

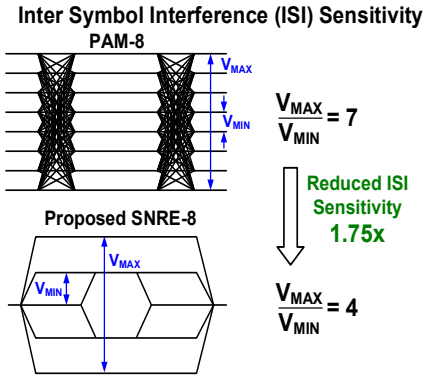

Fig. 2 ISI sensitivity reduction in the SNRE-8 over PAM-8.

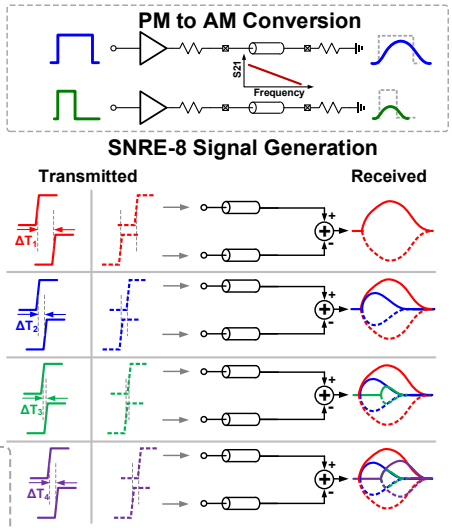

Fig. 3 SNRE-8 signal generation using PM to AM conversion property of the channel.

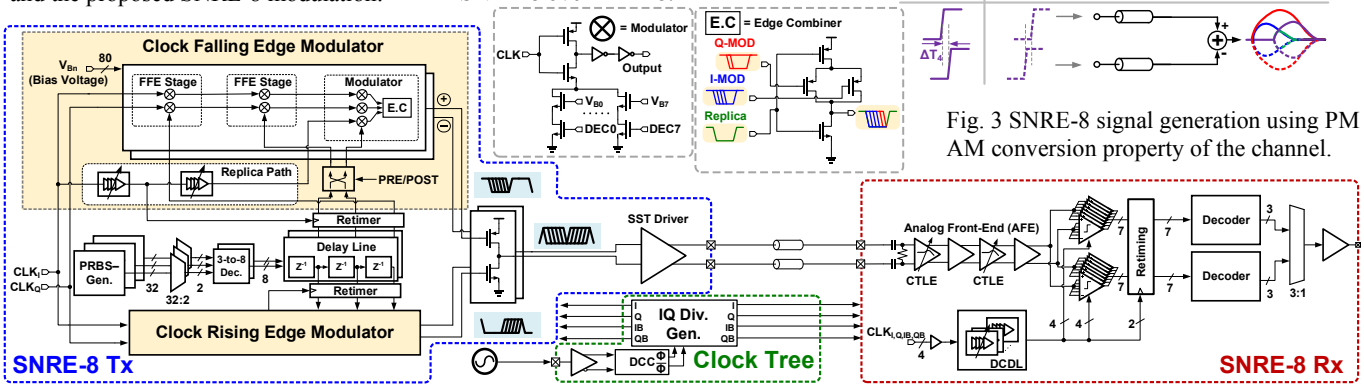

Fig. 4 Proposed SNRE-8 transceiver architecture.

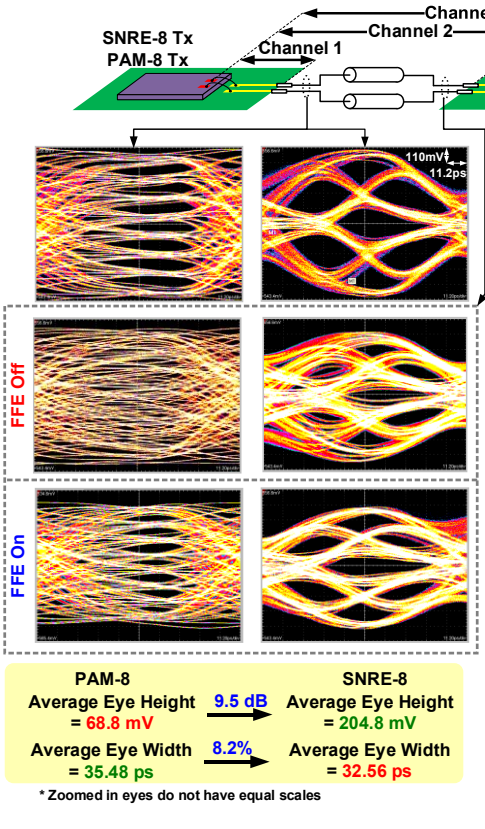

Fig. 6 Measured eye diagrams of PAM-8 and SNRE-8 transmitter at near-end, and far-end with and without FFE. A comparison of near-end eye measurements of SNRE-8 and PAM-8 shows 9.5dB SNR gain.

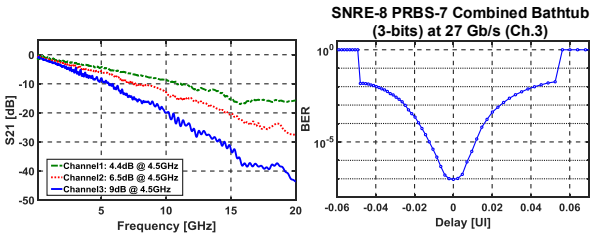

Fig. 5 Measured channel loss profiles and SNRE-8 transceiver bathtub at 27 Gb/s on 9 dB channel loss.

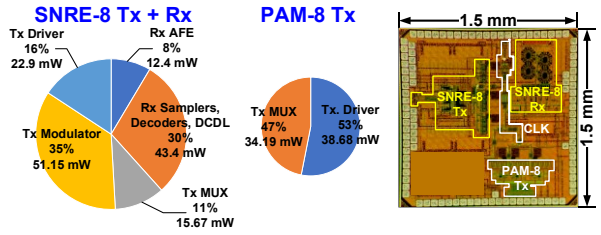

Fig. 7 SNRE-8 Tx+Rx, PAM-8 Tx power and chip micrograph.

Table I: Performance summary and comparison with state-of-the-art

	SNR Enhancement Links			Conventional Links	
	This work		Arungozeb, JSSC'20[2]	Y. Chun, ESSCIRC'19 [1]	A. Roshan-Zamir, JSSC'17
Process	65nm CMOS		28nm FDSOI	65nm CMOS	65nm CMOS
Bits/symbol	3		2	3	2
Modulation	SNRE-8 (Tx + Rx)	PAM-8 (Tx only)	Sequence Encoded PAM-4	PAM-8	PAM-4
Equalization	3-tap FFE + CTLE	3-tap FFE	3-tap FFE, Sequence encoding, CTLE, Trellis Decoding	4-tap RX FFE	3-tap FFE + 2-tap DFE
Data Rate (Gb/s)	27	27	28	36 - 39.6	32
Channel Loss (dB)	9	-	30	12.7, 14	13.5
BER	10^{-7}	-	10^{-12}	10^{-6}, 10^{-4}	10^{-12}
SNR Gain (dB)	9.5	-	5.26	-	-
Data-rate Overhead	0	0	12.5%	0	0
Tx Power (mW)	89.77	72.87	38	-	158.6
TxPower Efficiency (pJ/bit)	3.32	2.7	No	-	4.96
TxRx Power (mW)	145.62	-	93	311.4 ,342.9	176.3
TxRx Power Efficiency (pJ/bit)	5.39	-	2.9	8.66, 8.65	5.5
Area (mm²)	0.7	-	0.4	0.39	0.074