High-k Oxide Field-Plated Vertical (001) β-Ga_2O_3 Schottky Barrier Diode With Baliga's Figure of Merit Over 1 GW/cm^2

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***Abstract*— We report a vertical (001) β-Ga_2O_3 field-plated (FP) Schottky barrier diode (SBD) with a novel extreme permittivity dielectric field oxide. A thin drift layer of 1.7 μm was used to enable a punch-through (PT) field profile and very low differential specific on-resistance ($R_{on\text{-}sp}$) of 0.32 mΩ-cm^2. The extreme permittivity field plate oxide facilitated the lateral spread of the electric field profile beyond the field plate edge and enabled a breakdown voltage (V_{br}) of 687 V. The edge termination efficiency increases from 13.2 % for non-field plated structure to 61 % for high permittivity field plate structure. The surface breakdown electric field was extracted to be 5.45 MV/cm at the center of the anode region using TCAD simulations. The high permittivity field plated SBD demonstrated a record high Baliga's figure of merit (BFOM) of 1.47 GW/cm^2 showing the potential of Ga_2O_3 power devices for multi-kilovolt class applications.**

***Index Terms*— Ga_2O_3, field plate, high-k, Schottky diode, edge termination, power device, HVPE.**

I. Introduction

THE rise of β-Ga_2O_3 as the next generation power electronic material due to its large bandgap (~4.6 eV) and very high Baliga's figure of merit (3400_{Si}) [1] has enabled researchers to demonstrate multi-kV class devices. The estimated critical electric field of β-Ga_2O_3 (8 MV/cm) is significantly higher than GaN (3.3 MV/cm) and SiC (2.4 MV/cm). Various power devices including SBDs and transistors in both lateral and vertical geometry have been demonstrated with high breakdown voltages [2]–[16].

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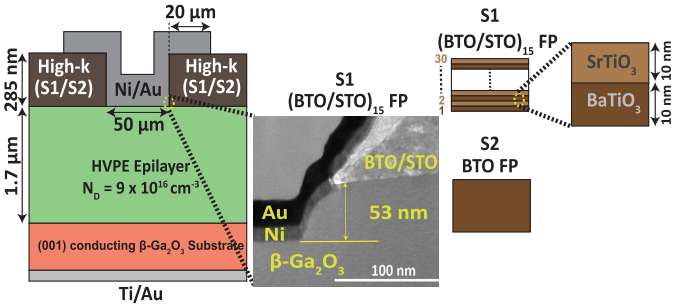

Fig. 1. Schematic of Ga_2O_3 SBD with high-k dielectric field plate, where S1 is the $(BTO/STO)_{15}$ dielectric field oxide for $(BTO/STO)_{15}$ FP SBD and S2 is the BTO dielectric field oxide for BTO FP SBD. The expanded region shows the TEM image of the anode edge of the $(BTO/STO)_{15}$ FP SBD.

Despite its huge potential, β-Ga_2O_3 poses several challenges regarding the management of electric field at the device corners and edges, causing premature breakdown of devices. The lack of p-type doping, which is widely used in GaN and SiC devices for edge field management also poses a fundamental challenge in device design and complicated hetero-integration is needed for β-Ga_2O_3 [17]. Even with non p-type edge terminations, the average electric field for demonstrated β-Ga_2O_3 devices are far lower than the theoretical material limit which makes the search of robust and efficient alternative edge termination techniques extremely necessary.

In this letter, we demonstrate a field-plated vertical SBD with an extreme permittivity ($BaTiO_3/SrTiO_3$) [18] field plate oxide [19] with PT design. By achieving a high dielectric constant of ~325, we have managed to increase the surface electric field at breakdown to 5.45 MV/cm. A breakdown voltage of 687 V in conjunction with a very low $R_{on\text{-}sp}$ (0.32 mΩ-cm^2) has resulted in a record BFOM of 1.47 GW/cm^2.

II. Device Fabrication

Device fabrication of the field plated SBD as shown in Fig. 1 started with the growth of the (001) β-Ga_2O_3 epilayers in a custom-designed subatmospheric vertical HVPE reactor using GaCl and O_2 precursors [20]. GaCl is produced in-situ by flowing Cl_2 over liquid Ga (7N purity), and is subsequently transported to the wafer surface through a quartz injector. Growth rate of ~5 $\mu m/hr$ is controlled by the GaCl molar flow rates. The as-grown samples were dipped in HF followed by HCl for 5 minutes. 15 layers of 10 nm thick $BaTiO_3$

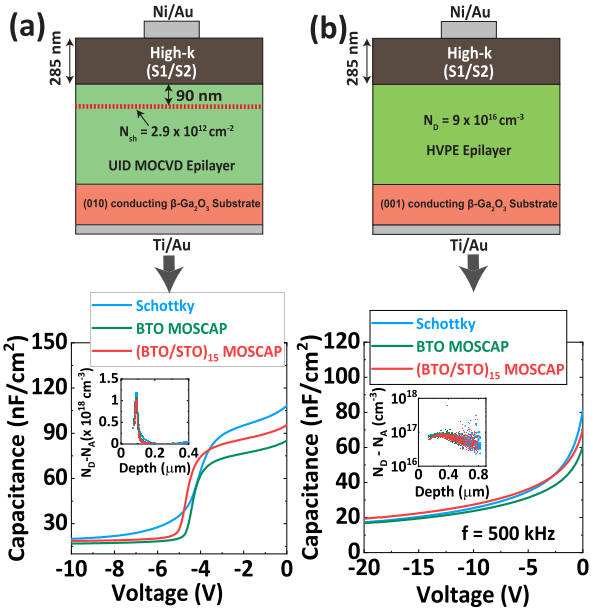

Fig. 2. (a) CV characteristics for an MOCVD grown delta doped sample with and without the dielectrics. (b) CV characteristics for the actual samples with and without the dielectrics. The inset of (a) and (b) shows the apparent charge density for the two samples.

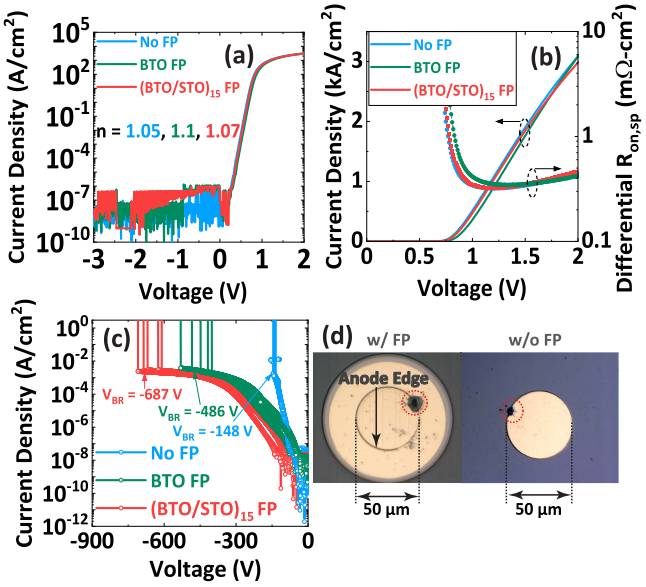

Fig. 3. (a) Log scale, & (b) linear scale IV characteristics of non-FP SBD, BTO FP SBD, and (BTO/STO)$_{15}$ FP SBD. (c) Breakdown characteristics of the three different SBD structures, and (d) Microscope image of the fabricated device showing breakdown location for the representative SBDs with and without FP.

and $SrTiO_3$ (BTO/STO)$_{15}$ (Measured total ~285 nm) were sputter deposited on the sample in oxygen ambient at room temperature. After the dielectric deposition, the sample was annealed at 700 °C in oxygen ambient for 30 minutes to increase the dielectric constant. The sample was then patterned using standard photolithography and the active regions were opened-up using SF_6/Ar dry etching. About 50 nm of overetching is performed to ensure the complete removal of the dielectrics which was confirmed using transmission electron microscope imaging (Fig. 1). EDS chemical map of the (BTO/STO)$_{15}$ dielectric layer indicated intermixing of Strontium and Barium, possibly due to the high temperature annealing. Ni/Au (20/40 nm) metal stacks were then deposited on the sample using e-beam evaporation. Finally, Ti/Au (50/100 nm) ohmic contacts were sputter deposited on the back side of the sample. Additional samples with $BaTiO_3$ (BTO) dielectric as field plate oxide and a reference SBD with no FP were also fabricated for comparison using the process flow described above.

III. Results And Discussions

Dielectric constants of the deposited (BTO/STO)$_{15}$ and BTO layer were extracted by depositing the dielectrics on an MOCVD grown (010) β-Ga_2O_3 with a δ-doped layer [21] using the method reported by Xia *et al.* [10]. The capacitance of the dielectrics were calculated by comparing the capacitance corresponding to the peak of the δ-doped layer with and without the dielectrics as shown in Fig. 2(a). The capacitance per unit area of the dielectric ($C_{dielectric}$) can be written as, $C_{dielectric} = (C_{ds}C_{dM})/(C_{ds}\text{-}C_{dM})$, where C_{ds} is the capacitance per unit area corresponding to the peak of the δ doping without the dielectric and C_{dM} is the capacitance per unit area corresponding to the peak of the δ doping with the dielectric. Using $\epsilon_r = C_{dielectric} \times t_{dielectric}/\epsilon_0$, the dielectric constant is extracted to be ~325 and ~142 for the (BTO/STO)$_{15}$ and BTO layer respectively, where ϵ_r is the dielectric constant of the dielectrics, $t_{dielectric}$ is the thickness of the dielectrics, and ϵ_0 is the permittivity of free space.

To understand effects of the dielectric deposition and the thermal annealing on the apparent charge density, capacitance voltage (CV) measurements were performed on the actual samples using the extracted dielectric constants as shown in Fig. 2(b) for the schottky diode, BTO MOSCAP, and (BTO/STO)$_{15}$ MOSCAP. A net doping concentration of 8-9 $\times$ 10^{16} cm^{-3} is extracted from the CV plot as shown in the inset of Fig. 2(b).

The typical current voltage plots in log and linear scale are shown in Fig. 3(a) and 3(b) respectively. The ideality factor (n) is extracted to be 1.04, 1.1 and 1.07 for the non- field plated SBD, BTO FP SBD, (BTO/STO)$_{15}$ FP SBD respectively. The normalized current is calculated by considering the area of the anode active region for the non-field plated and the field plated SBD since the current through the dielectric is found to be negligible for the operating voltage range (0-2 V) in the MOSCAP structures. The $R_{on\text{-}sp}$ for the non-field plated, BTO FP, and (BTO/STO)$_{15}$ SBDs from the linear fit of the IV characteristics are extracted to be 0.33, 0.34, and 0.35 mΩ-cm^2 respectively and the lowest differential $R_{on\text{-}sp}$ are 0.32, 0.34, and 0.32 mΩ-cm^2 respectively. Nominally similar values of ideality factor and on-resistance measured in all the three samples indicates that the dielectric deposition and the dry etching process of the dielectric did not degrade the drift layer and the metal/semiconductor interface.

The reverse breakdown characteristics for the SBDs measured using Keysight B1505A with no FP, BTO FP, and (BTO/STO)$_{15}$ FP are shown in Fig. 3(c). The destructive breakdown voltages for the three devices are extracted to be 148 V, 486 V and 687 V respectively. The breakdown craters were observed at the anode edges as shown in the optical microscope image of Fig. 3(d) for the FP and non-FP SBDs

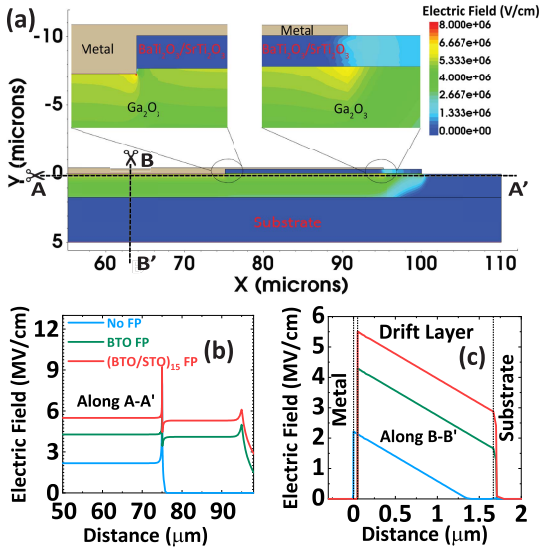

Fig. 4. (a) Electric field contour plot of the $(BTO/STO)_{15}$ FP SBD, (b) & (c) Simulated electric field profile for the three different SBDs for cutlines along the lateral and vertical directions respectively.

indicating the location of the breakdown. The increase in breakdown voltages for the high permittivity dielectric field plate oxide suggests the effectiveness of the edge termination and reduction in field crowding at the device edges due to the high permittivity of the FP dielectric.

The electric field simulations for the three SBD structures are also performed using Sentaurus TCAD software [22] and results are plotted in Fig. 4(a), (b), and (c). Except for the non-field plated SBD, the other two devices reach PT condition at breakdown as can be seen from Fig. 4(c). The calculated surface electric field (E_{surf}) for the non-punch-through (NPT) and punch-through devices can be calculated as $E_{surf-npt} = \sqrt{\frac{2qN_D V_{br}}{\epsilon}}$ and $E_{surf-pt} = \frac{V_{br}}{t_{drift}} + \frac{qN_D t_{drift}}{2\epsilon}$ respectively, where q is the electron charge, N_D is the donor concentration, ϵ is the permittivity of the dielectric, and t_{drift} is the thickness of drift layer. Using the above two expressions, the surface electric fields can be calculated for SBD with no FP as 2.2 MV/cm, with BTO FP as 4.2 MV/cm, with $(BTO/STO)_{15}$ FP as 5.42 MV/cm. The calculated values for electric field match exactly with the simulation values as can be seen in Fig. 4(b). This maximum surface electric field at hard breakdown of 5.45 MV/cm for SBD with $(BTO/STO)_{15}$ FP is the highest value reported to date for all the Schottky barrier diodes. A peak electric field of 8-9 MV/cm was estimated at anode edges suggesting the location of the breakdown, thus, confirming the weak points for each type of device as seen in the microscope images shown in Fig. 3(d).

If a perfect etching control is achieved, then based on simulations of the identical structure with no 50 nm over etching, we expect the peak electric field to be 6.1 MV/cm at the anode edge, with $(BTO/STO)_{15}$ FP at the anode bias of −687 V (32% reduction compared to the structure with etched Ga_2O_3). The edge termination efficiency ([Real V_{br}/Ideal V_{br}] × 100%) increases from 43.2% for the BTO FP to 61% for $(BTO/STO)_{15}$ FP, where Ideal V_{br} is calculated as $V_{BR,Ideal} = E_C t_{drift} - \frac{qN_D t_{drift}^2}{2\epsilon}$, where E_C is the predicted critical electric field for β-Ga_2O_3 (8 MV/cm).

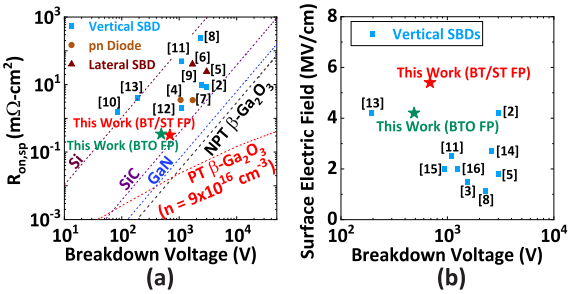

Fig. 5. Benchmark plot for (a) R_{on-sp} vs V_{br} and (b) Surface electric field vs V_{br} comparing our device with other reported vertical and lateral diodes.

The extremely low R_{on-sp} of 0.32 mΩ-cm^2 (0.35 mΩ-cm^2 from linear fit) and the breakdown voltage of 687 V for the $(BTO/STO)_{15}$ FP SBD results in a record high figure of merit of 1.47 GW/cm^2 (1.34 GW/cm^2 for the linear fit R_{on-sp} = 0.35 mΩ-cm^2). Fig. 5(a) shows the benchmark plots of R_{on-sp} and breakdown voltage comparing performance of the $(BTO/STO)_{15}$ FP SBD with the existing literature reports. The performance metrics of our device is significantly better compared to the other reported devices. The surface breakdown electric field of 5.45 MV/cm is the highest electric field reported to date for β-Ga_2O_3 based SBDs as can be seen from Fig. 5(b). It should be noted that E_{surf} extraction depends on the exact doping profile. For uniform doping in the range of 6 × 10^{16} cm^{-3} to 1 × 10^{17} cm^{-3}, the calculated E_{surf} is 4.96 to 5.57 MV/cm and the simulated E_{surf} is 4.97 to 5.6 MV/cm. Clearly the results demonstrated here represents the highest E_{surf} achieved in any SBD.

The demonstrated device structure can be designed for high voltage applications by appropriately choosing the thickness and doping concentration of the drift layer. If the surface breakdown electric field of 5.45 MV/cm is maintained as demonstrated for the high-k FP SBD, then using a drift layer thickness of 36 μm and doping concentration of 8.2 × 10^{16} cm^{-3}, the breakdown voltage can be extended to 10 kV. For such voltage ranges, β-Ga_2O_3 based devices have significant advantages compared to SiC based devices as SiC based devices require more than 100 μm of drift layer thickness for 10 kV breakdown voltages [23], [24], which in turn increases the on-resistance of the SiC devices.

IV. Conclusion

In summary we have demonstrated a vertical (001) oriented β-Ga_2O_3 SBD with high permittivity dielectric field plate oxide showing extremely low R_{on-sp} of 0.32 mΩ-cm^2 and a high breakdown voltage of 687 V resulting in a BFOM value of 1.47 GW/cm^2 surpassing all the reported SBDs. The extracted surface breakdown electric field of 5.45 MV/cm is the highest electric field reported to date for β-Ga_2O_3 SBDs. This demonstration indicates that the use of such high-k dielectric field-plated structure enables high edge field termination efficiency and also enable studying the intrinsic critical field limits of ultra-wide band-gap semiconductors.

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