Linearity-Enhanced Quasi-Balanced Doherty Power Amplifier With Mismatch Resilience Through Series/Parallel Reconfiguration for Massive MIMO

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***Abstract*— A reconfigurable series/parallel quasi-balanced Doherty power amplifier (QB-DPA) is presented with a unique capability of maintaining high linearity and high efficiency against load mismatch, which is highly desirable for massive multiple-input–multiple-output (MIMO) and active array applications. Based on the new QB-DPA topology derived from an ideal balanced amplifier, it is, for the first time, discovered that QB-DPA can be reconfigured between series- and parallel-DPA modes by setting the isolation-port loading to the ground and open circuit, respectively, and exchanging the roles of main and auxiliary amplifiers. Expanding from the ideal Doherty modes, the isolation port can be loaded with small reactance (susceptance) for linearity enhancement of series (parallel) QB-DPA. Furthermore, by leveraging the symmetry of series and parallel modes with complementary sensitivities to load impedance/admittance, it is theoretically proved that the QB-DPA can be strongly mismatch-resilient. Based upon the comprehensive and conclusive theoretical analysis, a physical prototype demonstration is practically presented using the GaN technology at 3.5 GHz. In modulated measurement using Long-Term Evolution (LTE) signals, the developed QB-DPA exhibits excellent linearity, e.g., < 1.6% error vector magnitude (EVM) and high average efficiency of 45% at the rated averaged power in the nominal 50-Ω condition, which compares favorably with state of the art. More importantly, through only a two-state adaption (using silicon-on-insulator (SOI)-based switches) of reactive loading at the output isolation port together with optimized gate biasing, the high linearity (< 4% EVM) and average efficiency (> 31%) can be experimentally maintained up to 2.5 : 1 of voltage standing wave ratio.**

***Index Terms*— Balanced amplifier, Doherty power amplifier (DPA), linearity, load mismatch, reconfigurable.**

I. Introduction

THE evolution of modern wireless communications, featured as ever-increasing user capacity and spectral efficiency, has triggered the development of advanced modulation techniques, including higher order quadrature amplitude modulation (e.g., 1024 QAM) and orthogonal frequency-division multiplexing (OFDM). These complex modulation schemes have been extensively utilized to increase the bit/symbol rate and mitigate the exacerbating spectrum congestion. Besides the benefits, one of the byproducts is the large peak-to-average power ratio (PAPR) of signals, which require the power amplifiers (PAs) to operate efficiently and linearly across a large power back-off range. The Doherty PA (DPA) has been the most widely adopted technique in the modern wireless communication systems due to its capability of significant back-off efficiency enhancement [1]–[11]. Despite the nonlinear nature of DPA because of the load modulation, external linearization techniques, such as digital predistortion (DPD), can be applied at the digital backend to ensure a good signal fidelity and to suppress the out-of-band spectrum regrowth for meeting the emission requirements of the emerging wireless communication standards. The recently reported load-modulated balanced amplifier (LMBA) [12]–[20] and quasi-balanced Doherty power amplifier (QB-DPA) in [21]–[23] have also been demonstrated as effective platforms to perform load modulation with $\geq$ 9-dB power back-off range.

On the other hand, to expand the user channel capacity, radiation coverage, and overall system capability, the spatial multiplexing and combining techniques, i.e., massive multiple-input–multiple-output (MIMO) based on active antenna arrays, have been widely deployed in the emerging communication systems [24], [25]. Massive MIMO offers significantly enhanced spectral efficiency to accommodate the ever-growing number of subscribers within the highly congested sub-6-GHz spectrum. However, with high density of antennas in a massive MIMO array, the mutual coupling between adjacent elements is sufficiently strong to engender dynamic variations of the antenna impedance at very short beam scanning periods [26]–[28], and therefore, the antenna presents a suboptimal loadline to the associated PA instead of a matched 50-Ω, as shown in Fig. 1(a). Consequently, the PA as a load-sensitive device can suffer from drastic performance degradation during massive MIMO operations. Moreover, the impedance variations of different antenna elements are inhomogeneous among the entire array, leading to major difficulty and complexity in performing DPD on the large number of massive MIMO PAs [29]–[32].

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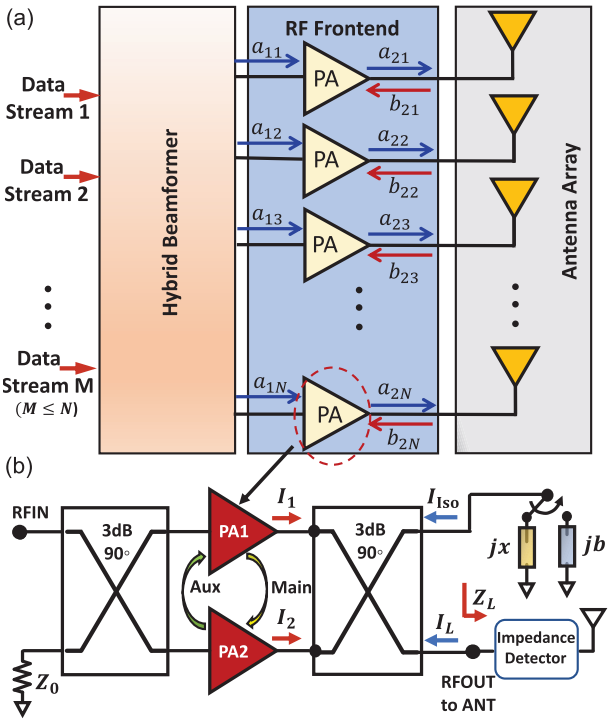

Fig. 1. Conceptual illustration. (a) MIMO antenna array with mutual coupling affecting the PA loading. (b) Proposed reconfigurable series/parallel QB-DPA for load mismatch resilience.

Therefore, the PAs in future communication systems are expected to maintain efficient and linear operations when exposed to substantial load mismatch. Available solutions are mostly based on discrete antenna tuners on mobile platforms and PA-antenna isolators/circulators in the base stations. The former method is bottle-necked by the tuning speed, which is insufficient to track the fast antenna impedance variations in MIMO operations; the latter one is bulky, nonlinear, expensive, and lossy, inhibiting its feasibility for the massive-scale array integration [33]–[35]. Recently, new attempts targeted to recover the mismatch directly at the PA stage have demonstrated promising potential [36]–[39]. In [38], a Doherty-like PA uses a multiport network synthesis approach to restore the voltage standing wave ratio (VSWR)-induced degradation by largely compromising output power and linearity, while only selected measurement performance of VSWR points are presented. In [39], a parallel/series switchable DPA is reported with reconfigurable weighting of main/auxiliary-PA currents and phase offset to recover the linearity and efficiency up to 3 : 1 VSWR, but this method has not been systematically and analytically studied. Meanwhile, the low-power implementation in silicon at mm-Wave frequencies is very different from the prevailing GaN technology mainly adopted in base stations where the massive MIMO is primarily deployed.

The balanced-to-Doherty mode-reconfigurable PA presented in the authors' previous works [21], [22] analytically proves that the QB-DPA functionally is equivalent to an ideal DPA. This discovery enables the PA reconfiguration between Doherty and balanced modes to counteract the performance impairment introduced by load mismatch. However, the efficiency at balanced mode is significantly degraded since no load modulation is performed. In this article, it is for the first time discovered that the QB-DPA is reconfigurable between series mode and parallel mode [40] through reciprocally exchanging the main and auxiliary amplifiers and alternatively terminating the isolation port of the output coupler to a small reactance (close to short circuit) and susceptance (close to open circuit), respectively. Compared with [22], a novel linearity-enhanced combiner is proposed for nominal 50-Ω load to improve the linearity at both series and parallel modes. Furthermore, the reconfiguration between series and parallel operations significantly alleviates the performance degradation [e.g., error vector magnitude (EVM) and drain efficiency (DE)] when suffering a load mismatch condition. Based on the circuit architecture conceptually shown in Fig. 1(b), this article systematically establishes the linearity-enhanced QB-DPA theory for both series and parallel modes with the elegant mathematical symmetry. Moreover, the QB-DPA theory reveals that the series and parallel modes have different sensitivities to load mismatch in a complementary way. Therefore, a hybrid operation over two modes can be utilized to counteract the arbitrary load mismatch up to 2 : 1 of VSWR, as normally expected in massive MIMO operations [33], [34]. Based on the established theory, a prototype developed at 3.5 GHz demonstrates excellent performance at matched load with the lowest EVM (1.5%) compared to the state of the art of linear GaN PAs [41]–[45], while the efficient and linear DPA operation can be maintained against substantial load mismatch up to 2.5 : 1 VSWR.

In a realistic system, the PA load impedance can be monitored in real time using the impedance sensors. For open-loop operation, the optimal setting of DPA mode, gate biasing, and impedance can be precharacterized and stored in a lookup table (LUT) so that the reconfiguration is triggered according to the sensing results and LUT. For closed-loop operation, the output signal is also monitored besides the load impedance, and a few iterations may be conducted until the output signal fidelity meets the specs. Once the load mismatch is detected for a specific antenna condition, this mismatch can then be transferred to the local PA load through the interconnections to further process. The length of the feeding line between PA and antenna can induce considerable delay that affects the system response time. However, in the latest massive MIMO systems, e.g., 5G base stations, the antenna array and PAs are integrated within the same module, known as active antenna unit (AAU), where the PA-antenna interconnection is minimized.

II. Series and Parallel QB-DPA Theory and Linearity Enhancement

The concept of series/parallel reconfigurable QB-DPA through the switching of short-/open-circuit loading of isolation port of the output 90° coupler and the role exchanging of main and auxiliary PAs is presented in the following analysis. Originated from the recently reported ideal QB-DPA [21], [22] (equivalent to the conventional series DPA), this theory is not only generalized by incorporating an arbitrary reactive isolation-port loading for analog linearization but also

dualized with a symmetrical mode, linearity-enhanced parallel QB-DPA.

A. Transistor Modeling

The analytical study begins with the transistor model establishment. Following the widely adopted paradigm [46], a simplified but general model is set up with the following assumptions.

1) The transistors are considered as piecewise linear transconductive current sources with zero knee voltage and zero output reactance (i.e., package and device parasitics).
2) The transistors' harmonic currents are properly short-circuited to achieve the maximum fundamental efficiency according to the theory [46] and optimal loads are presented to the Class-B and Class-C cells.

Besides the above assumptions, as the driving stimulus, the drain current is defined only with the magnitude information at this stage, and the phase relationship will be considered when analyzing the load-modulation behaviors. Therefore, the main current can be expressed as

$$I_{\text{main}}(\beta) = \begin{cases} \beta I_{\max} \cos\theta, & -\dfrac{\pi}{2} \le \theta \le \dfrac{\pi}{2} \\ 0 & \text{otherwise} \end{cases} \tag{1}$$

where β ($0 \le \beta \le 1$) is the normalized magnitude of the input voltage drive and $I_{\max}$ is the maximum channel current that can be supported by the transistor device. Subsequently, by using the Fourier transform, main transistor's fundamental and dc currents are given by

$$I_{\text{main}}[0] = \frac{\beta}{\pi} I_{\max} \tag{2}$$

$$I_{\text{main}}[1] = \frac{\beta}{2} I_{\max}. \tag{3}$$

Based on Assumption 2, both the main and auxiliary transistors maintain full voltage and current swings at the peak power level. Assuming that the auxiliary transistor remains turned-off in the low-power region ($\beta < \beta_{\text{th}}$) and the same $I_{\max}$ as the main transistor can be achieved at peak-power level, the auxiliary fundamental current can be expressed as follows:

$$I_{\text{aux}}[1] = \begin{cases} \dfrac{\beta - \beta_{\text{th}}}{1 - \beta_{\text{th}}} I_{\max}, & \beta_{\text{th}} \le \beta \le 1 \\ 0 & 0 < \beta < \beta_{\text{th}} \end{cases}. \tag{4}$$

In the conventional DPA configuration, β_{th} defines the threshold for the auxiliary amplifier turn-on point. In practice, different β_{th} values indicate the back-off levels. Specifically, for $\beta_{\text{th}} = 0.5$, it corresponds to a 6-dB power back-off range for a classical DPA. Fig. 2 exhibits the current and voltage profiles for an ideal DPA, in which the output RF voltage swings are normalized to V_{DD}.

B. QB-DPA Theory: Series and Parallel Topologies

A conceptual model shown in Fig. 3(a) illustrates the block schematic of the conventional series DPA proposed in [1]. It has been theoretically verified that the generic series QB-DPA in Fig. 3(b) is functionally equivalent to the conventional series DPA [21]–[23]. This generic QB-DPA architecture is developed from an ideal balanced amplifier with the isolation port of output branch-line quadrature coupler terminated to the ground. Ideally, the main and auxiliary amplifiers are sized symmetrically inheriting the nature of balanced amplifier topology. The phase of main amplifier in this configuration is in $+90^\circ$ offset to auxiliary one, which is necessary to ensure an in-phase combination of the main and auxiliary signals at the output. It is interesting to note that the generic series QB-DPA in Fig. 3(b) can be treated as a special case, where the isolation port of the quadrature coupler in Fig. 3(c) is loaded with a reactive termination, jx.

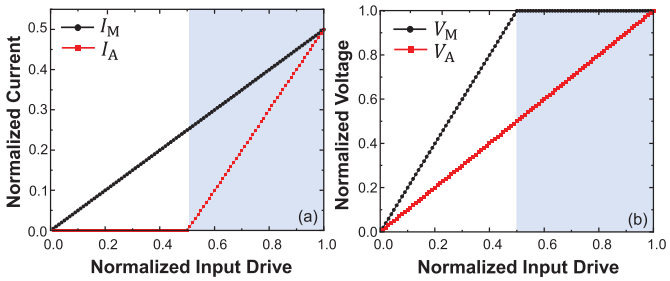

Fig. 2. Fundamental current and voltage profiles for the ideal DPA.

To simplify the analysis, the main and auxiliary PA cells are represented with two current sources I_{M} and $-jI_{\text{A}}$, respectively. Therefore, in a system with characteristic impedance Z_0 (non-50-Ω of Z_0 may be used in practical designs as part of transistor matching), the voltage and current relationship on the output coupler can be expressed as

$$\begin{bmatrix} V_0 \\ -jXI_{\text{Iso}} \\ V_{\text{A}} \\ V_{\text{M}} \end{bmatrix} = \hat{\boldsymbol{Z}}_{\text{coupler}} \begin{bmatrix} I_0 \\ I_{\text{Iso}} \\ -jI_{\text{A}} \\ I_{\text{M}} \end{bmatrix} \tag{5}$$

where V_0 and I_0 denote the output voltage and current when the load port Z_0 is matched and $jx = jX/Z_0$ is the normalized reactance value. The generic series QB-DPA in Fig. 3(b) can be expressed with (5) as $jx = 0$ with the expression of $\hat{\boldsymbol{Z}}_{\text{coupler}}$ for the ideal 3-dB quadrature coupler matrix as presented in the following:

$$\hat{\boldsymbol{Z}}_{\text{coupler}} = Z_0 \begin{bmatrix} 0 & +j & -j\sqrt{2} & 0 \\ +j & 0 & 0 & -j\sqrt{2} \\ -j\sqrt{2} & 0 & 0 & +j \\ 0 & -j\sqrt{2} & +j & 0 \end{bmatrix}. \tag{6}$$

It is further discovered that by leaving the output coupler's isolation port open-circuited and swapping the roles of main and auxiliary amplifiers as shown in Fig. 3(e), the ideal balanced amplifier can be converted into another DPA configuration equivalent to the conventional parallel DPA of Fig. 3(d) first introduced in [40]. Thus, this new DPA mode is named parallel QB-DPA. Similarly, a generalization in Fig. 3(f) with the isolation termination jb under the stimulus current sources

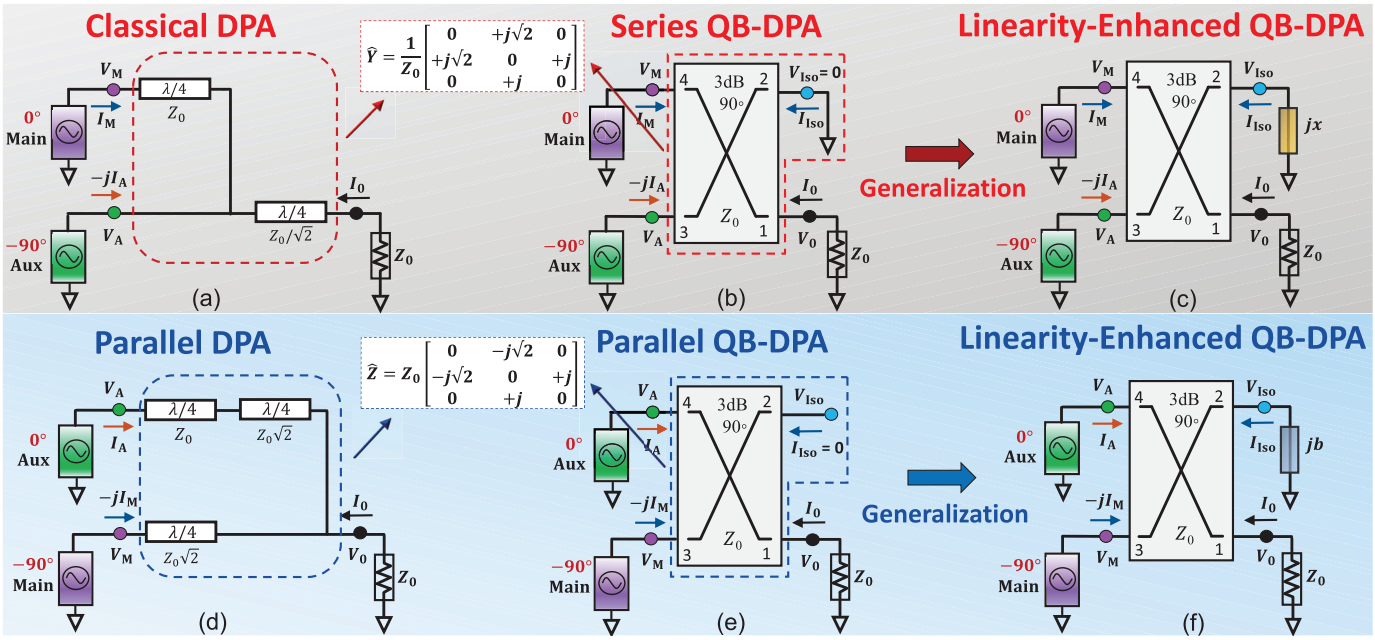

Fig. 3. Derivation of DPA architectures. (a) Classical DPA. (b) Series QB-DPA. (c) Linearity-enhanced series QB-DPA. (d) Parallel DPA. (e) Parallel QB-DPA. (f) Linearity-enhanced parallel QB-DPA.

$-jI_M$ and I_A can be formulated as

$$\begin{bmatrix} V_0 \\ V_{Iso} \\ V_M \\ V_A \end{bmatrix} = \hat{\mathbf{Z}}_{\mathbf{coupler}} \begin{bmatrix} I_0 \\ -jBV_{Iso} \\ -jI_M \\ I_A \end{bmatrix}. \tag{7}$$

Likewise, V_0 and I_0 represent the output voltage and current as well at the nominal load Z_0 condition and $jb = jBZ_0$ denotes the normalized susceptance, where $jb = 0$ corresponds to the generic parallel QB-DPA.

One can find the symmetry from (5) and (7) that the load-modulation profiles of the main and auxiliary amplifiers for generic series and parallel QB-DPA modes can be obtained as

$$Z_{M,bo} = 2Z_0 \ \& \ Z_{A,bo} = \infty \tag{8}$$

$$Z_{M,sat} = Z_0 \ \& \ Z_{A,sat} = Z_0. \tag{9}$$

The subscripts "bo" and "sat" specify the variable evaluated at the back-off and saturation regions, whereas "M" and "A" represent the main and auxiliary transistors, respectively. Based on the load-modulation behaviors given by (8) and (9), it is interesting to note that the generic series/parallel QB-DPA with the isolation port short-/open-circuited is mathematically equivalent to a classical/parallel DPA through the three-port Y/Z-matrix analysis, as shown in Fig. 3.

Furthermore, as derived from (5) and (7), the output voltage V_0 of both generic typologies ($jx = 0, jb = 0$) can be expressed with the same form as

$$V_0 = -Z_0 I_0 = -\sqrt{2} I_M Z_0. \tag{10}$$

Since the magnitude and phase of V_0 represent the AM-AM and AM-PM of the overall system, (10) reveals a fact that the overall linearity of the QB-DPA is directly determined by the main amplifier's distortion. As reported in [41] and [42], the nonlinearity of the transistor mainly lies in the AM-PM distortion due to the strongly nonlinear parasitic capacitors (e.g., C_{DS}). In other words, if a complementary phase characteristic can be properly designed to compensate for the main transistor's AM-PM behavior, the overall system AM-PM will be improved.

C. Linearity-Enhanced Series and Parallel QB-DPAs

Multiple methodologies have been proposed to minimize the overall AM-PM distortion through generating a predefined AM-PM characteristic of the DPA combiner that is complementary to the main transistor [41], [42].

As previously mentioned, the generic QB-DPA, which can be switched between series and parallel modes gracefully, presents identical characteristics with standard DPAs in terms of the active load-modulation behaviors and inducement of PA nonlinearity. In this section, further exploration is presented on the feasibility and versatility of the reconfigurable QB-DPA for linearity enhancement. In order to generate the desired AM-PM at the combiner stage to compensate for the main transistor's nonlinearity, the quadrature coupler with reactive loading of the isolation port as shown in Fig. 3 is thereby investigated. In the series mode, instead of directly short-circuited to ground, the isolation port is terminated with a small reactance (jx), as shown in Fig. 3(c). When the QB-DPA is reconfigured to the parallel mode, the isolation-port loading is switched to a small susceptance (jb) slightly deviated from the ideal open circuit together with the role exchange of main and auxiliary PAs in Fig. 3(f).

It is discovered that the reactive loading of isolation port changes the combiner characteristics, which can be leveraged for QB-DPA linearization. From (5) and (7), this

load-modulation behaviors for main and auxiliary cells can be obtained as

$$Z_{\mathrm{M_{SE}},\mathrm{bo}} = \frac{2}{jx+1} Z_0 \;\&\; Z_{\mathrm{A_{SE}},\mathrm{bo}} = \infty \tag{11}$$

$$Z_{\mathrm{M_{SE}},\mathrm{sat}} = Z_0 \;\&\; Z_{\mathrm{A_{SE}},\mathrm{sat}} = Z_0 \tag{12}$$

where "SE" specifies the series operation mode.

As for the linearity-enhanced parallel QB-DPA with the susceptance loading of jb, shown in Fig. 3(f), the load modulation seen for the main and auxiliary amplifiers are formed by

$$Z_{\mathrm{M_{PL}},\mathrm{bo}} = \frac{2}{jb+1} Z_0 \;\&\; Z_{\mathrm{A_{PL}},\mathrm{bo}} = \infty \tag{13}$$

$$Z_{\mathrm{M_{PL}},\mathrm{sat}} = Z_0 \;\&\; Z_{\mathrm{A_{PL}},\mathrm{sat}} = Z_0 \tag{14}$$

in which "PL" represents the parallel operation mode.

Comparing two sets of the above equations, i.e., (11) and (12) and (13) and (14), one can recognize that the load-modulation behaviors of the series and parallel linearity-enhanced QB-DPA are perfectly symmetrical in math, if the values of jx and jb are equalized. This graceful duality can be further verified with the analytical expressions of the main and auxiliary voltages, V_{M} and V_{A}, derived from (5) and (7) as well

$$V_{\mathrm{M_{SE}}} = \frac{2I_{\mathrm{M}} + jxI_{\mathrm{A}} - I_{\mathrm{A}}}{jx+1} Z_0 \tag{15}$$

$$V_{\mathrm{A_{SE}}} = -j\frac{I_{\mathrm{M}} - jxI_{\mathrm{M}} + j2xI_{\mathrm{A}}}{jx+1} Z_0 \tag{16}$$

$$V_{\mathrm{M_{PL}}} = -j\frac{2I_{\mathrm{M}} + jbI_{\mathrm{A}} - I_{\mathrm{A}}}{jb+1} Z_0 \tag{17}$$

$$V_{\mathrm{A_{PL}}} = \frac{I_{\mathrm{M}} - jbI_{\mathrm{M}} + j2bI_{\mathrm{A}}}{jb+1} Z_0. \tag{18}$$

It is interesting to note that the formulas of V_{M} and V_{A} not only indicate the retained symmetry between series and parallel modes for their magnitudes but also reflect the relative phase offsets between the main and auxiliary PAs in both modes, respectively. Moreover, the output voltages of the linearity-enhanced QB-DPAs can be obtained as

$$V_{0_{\mathrm{SE}}} = \frac{-\sqrt{2}I_{\mathrm{M}} - j\sqrt{2}xI_{\mathrm{A}}}{jx+1} Z_0 \tag{19}$$

$$V_{0_{\mathrm{PL}}} = \frac{-\sqrt{2}I_{\mathrm{M}} - j\sqrt{2}bI_{\mathrm{A}}}{jb+1} Z_0. \tag{20}$$

Again, the symmetrical output voltage profiles unveil a remarkable fact that the equalized reactance/susceptance loading (i.e., $jx = jb$) at the isolation port functions equivalently to engender the predefined AM-PM characteristic in series and parallel linearity-enhanced QB-DPA modes, respectively.

Based on the solid mathematical derivations of load modulation together with the driving current expressions of (1) and (4), the theoretical models of series and parallel QB-DPAs are established using MATLAB to verify the linearity enhancement in a graphical method. Theoretical calculation results will be presented to intuitively visualize the theory. Fig. 4(a) shows that the QB-DPA generates dedicated AM-PM profiles corresponding to different values of $|jx|$ ($|jb|$), and

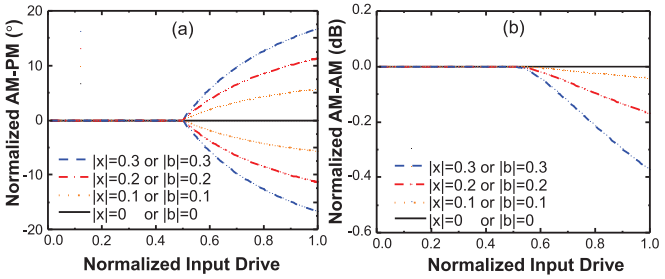

Fig. 4. Calculated dynamic PA behaviors of the linearity-enhanced architecture. (a) AM-PM profiles. (b) AM-AM profiles.

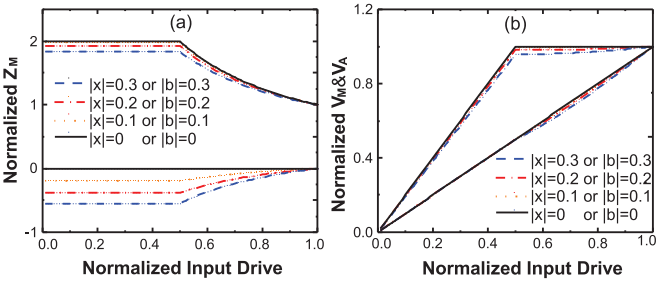

Fig. 5. (a) Load and (b) voltage behaviors of the symmetric series and parallel QB-DPA modes.

these predefined AM-PM characteristics can be used to counteract the phase distortions exhibited by the main transistor. Ultimately, this will lead to an overall linear AM-PM when the two nonlinearity mechanisms coexisting in the DPA are complementary. Moreover, as shown in Fig. 4(b), the linearity compensation for AM-PM profiles using the reactance (susceptance) loading only induces a limited AM-AM distortion of 0.2 dB when generating a 10° AM-PM profile. This feature significantly alleviates the gain compression during load modulation even for a large 15° AM-PM compensation, exhibiting clear advantage compared to the decibel-level gain droop for the same compensation strength as reported in [41] and [42].

Fig. 5 shows the calculated drain load and the voltages under various jx (jb) induced phase offset values between 0° and 20°. As shown in Fig. 5(a), the value of jx (jb) may also affect the extent of load modulation. Unlike the generic QB-DPA, the load behavior of the main transistor in linearity-enhanced QB-DPA is not a purely resistive profile, which means that the main transistor experiences a continuous load trajectory in the Smith chart. This engenders a slight degradation of V_{M} and V_{A} less than V_{DD} over the Doherty region when jx (jb) is varied, as is presented in Fig. 5(b). It is worthy to note that the incorporation of the reactance (susceptance) tuning significantly relieves the potential of stronger voltage swing over the entire Doherty region, whereas with minor back-off efficiency sacrifice, and consequently, peak efficiency operation is maintained for the Doherty region, as shown in Fig. 6. Based on the above analysis, the synthesis network of an AM-PM with up to 15° distortion to compensate for an AM-PM characteristic of the main transistor brings in slight influence on back-off efficiency and limits AM-AM compression to a few decibels (0.4 dB).

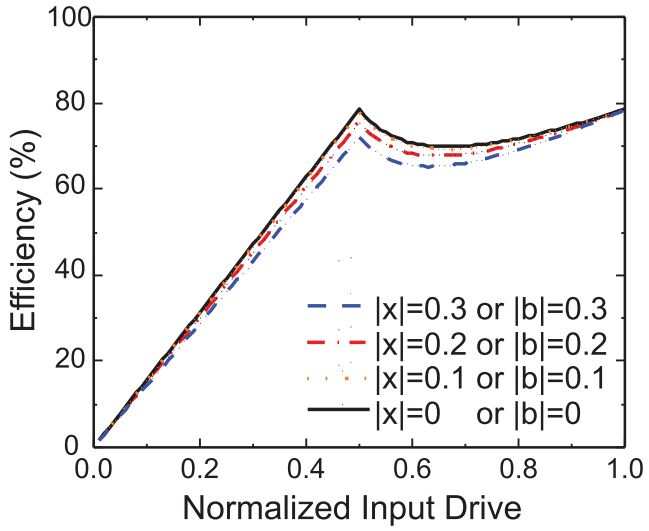

Fig. 6. Efficiency calculation based on the proposed reconfigurable QB-DPA.

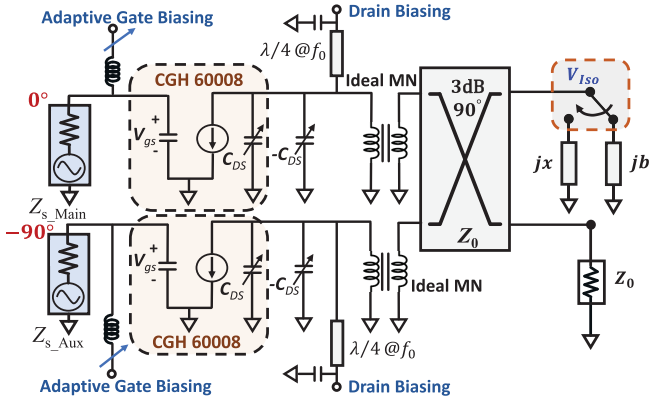

Fig. 7. Setup of the emulated QB-DPA model.

In summary, the proposed linearity-enhanced reconfigurable QB-DPA relies on reactance/susceptance loading at the isolation port of the output quadrature coupler, which is a generalized architecture compared with [21] and [22] in terms of performance and design freedom.

D. Verification Using Emulated QB-DPA Model

The derivation described in Section II-C demonstrates the possibility of utilizing reconfigurable reactive tuning at isolation port to enhance the overall QB-DPA linearity. To verify the theory, an emulated model of linearity-enhanced QB-DPA is established using bare-die GaN transistors, as shown in Fig. 7. The CGH60008 model from Wolfspeed is employed for the main and auxiliary transistor cells. The source impedances for main and auxiliary transistors are set equally based on the source-pull results to suit the symmetry of two modes in reconfiguration. Two ideal transformers are utilized to provide optimal loadline impedances for main and auxiliary transistors, respectively. A compensation $-C_{\mathrm{DS}}$ is utilized to deembed the parasitic capacitance of the transistor, and the second harmonic impedance termination is set to short circuit by the quarter-wave bias line. Finally, the reconfigurable reactive loading is connected to the isolation port of the coupler for linearity enhancement.

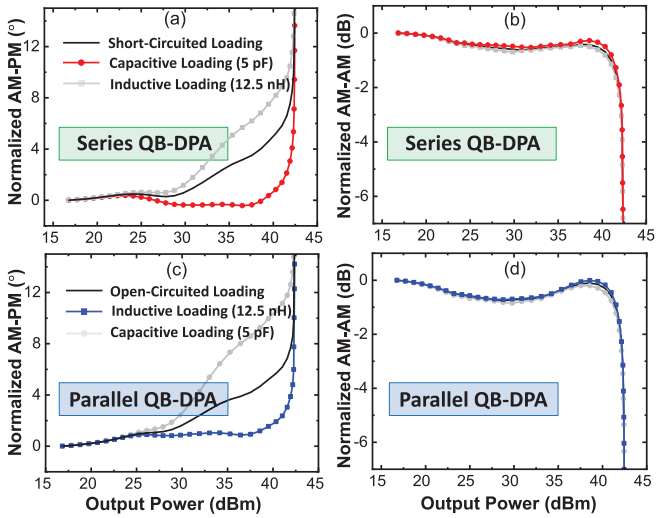

Fig. 8. Simulated AM-PM and AM-AM profiles of emulated QB-DPA model in series mode (a) and (b), and parallel mode (c) and (d), respectively.

The main amplifier is biased in Class-AB mode to better mimic the realistic case. Fig. 8 shows the AM-PM and AM-AM behaviors of the QB-DPA emulated mode. The AM-PM variation induced by (primarily) the power-dependent C_{DS} and (secondarily) the Class-AB biasing of main PA can be substantially restored at load-modulation region. For the series mode shown in Fig. 8(a) and (b), a 5-pF capacitor ($x = -0.18$) loading at isolation port offers the optimal compensation effect leading to a flat AM-PM profile with meanwhile negligible impact on AM-AM property. Similarly, for the parallel mode in Fig. 8(c) and (d), a symmetric inductance of 12.5 nH ($b = -0.18$) is loaded at the isolation port that leads to the same AM-PM distortion cancellation. The simulation results agree well with the mathematical derivation and results in Secstions II-B and II-C, which solidly prove the theory.

III. Series/Parallel Mode Reconfiguration for Mismatch Recovery

The ability for series/parallel reconfiguration of linearity-enhanced QB-DPA can be utilized to counteract the load impedance mismatch effects. As the conceptual illustration shown in Fig. 1(a), antenna impedance variations can severely affect the desired PA operation and degrade its output power, efficiency, linearity, and reliability. In this section, the mechanism of mismatch recovery through series/parallel DPA reconfiguration will be analytically formulated for the first time. As a specific case study, the mismatch compensation on the 2 : 1 VSWR circle will be presented based on the established theoretical model.

A. Analysis of Impedance Mismatch Effects

For simplicity, the load-mismatch effects will be first studied for the generic series and parallel QB-DPA modes with ideal isolation-port loading ($jx = 0$, $jb = 0$). Using the conditions given by (5) and (7) and based on the voltage/current dependence of load ($Z_{\mathrm{L}} = V_0/I_0$), the load impedances observed by

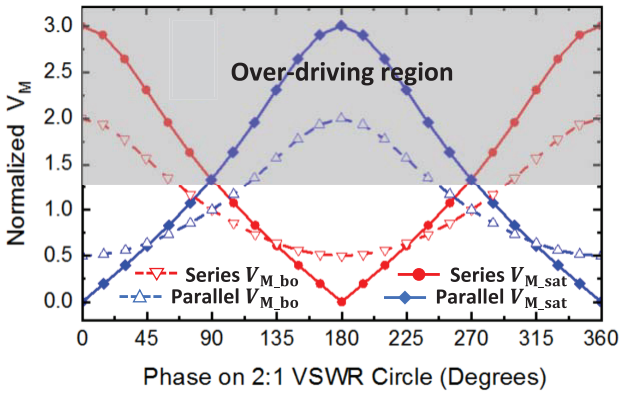

Fig. 9. Sketch of main amplifier voltage at series/parallel modes due to load mismatch.

main and auxiliary PAs of series QB-DPA are derived as

$$Z_{M_{SE},bo}(z_L) = 2z_L Z_0 \;\&\; Z_{A_{SE},bo} = \infty$$
$$Z_{M_{SE},sat}(z_L) = (2z_L - 1)Z_0 \;\&\; Z_{A_{SE},sat} = Z_0 \qquad (21)$$

where z_L denotes the normalized value of Z_L. Likewise, for parallel mode, the main and auxiliary impedances due to the current/voltage dependence ($Y_L = I_0/V_0$) are formed as

$$Z_{M_{PL},bo}(y_L) = 2y_L Z_0 \;\&\; Z_{A_{PL},bo} = \infty$$
$$Z_{M_{PL},sat}(y_L) = (2y_L - 1)Z_0 \;\&\; Z_{A_{PL},sat} = Z_0 \qquad (22)$$

in which y_L represents the normalized value of Y_L. The magnitude and phase of main and aux voltages due to load mismatch can be obtained as

$$V_{M_{SE}}(z_L) = (2I_M z_L - I_A)Z_0 \;\&\; V_{A_{SE}} = -jI_M Z_0$$
$$V_{M_{PL}}(y_L) = -j(2I_M y_L - I_A)Z_0 \;\&\; V_{A_{PL}} = I_M Z_0. \qquad (23)$$

Remarkably, the mathematical symmetry between series and parallel modes is derived from the main and auxiliary voltages (in magnitude) as well as the load-modulation behaviors, by exchanging z_L and y_L. In other words, under the mismatched loads when $z_{L,SE} = y_{L,PL} = 1/z_{L,PL}$, the series and parallel QB-DPA are functionally equivalent. The phase difference of V_M and V_A between series and parallel modes is due to the interchanged positions of main and auxiliary amplifiers. It is also important to note that the voltage of auxiliary amplifier (V_A) is independent of the load mismatch that can be seen from (23), and thus, only the main amplifier of both modes will be analyzed under different load conditions. The V_M magnitude over the full VSWR 2 : 1 circle of back-off and saturation is shown in Fig. 9. If an upper limit of $V_M \le 1.25V_{DD}$ (slight voltage overdriven) is set in order to avoid reliability issues, the mismatch-induced voltage overdriving is inevitable in either series mode (for large z_L) or parallel mode (for large y_L). Given the fact that z_L and y_L ($= 1/z_L$) normally complement each other, a reconfiguration between series/parallel modes in different mismatched loads can maintain the main amplifier voltage below the highest acceptable value, i.e., $1.25V_{DD}$, as shown by the unshaded region of Fig. 9.

Overall, to avoid the voltage overdriving of the main amplifier as indicated by (23), the QB-DPA should operate in series mode for the left half-plane of the Smith chart, whereas the parallel mode is desired in the right half, as shown in Fig. 10(a). To better present the load modulation of both modes under mismatch, the DPA operation behaviors are extracted using the theoretical model for several special and representative loads on the 2 : 1 VSWR circle, as shown in Fig. 10(a). The associated efficiency profiles of these four sample cases are plotted in Fig. 10(b). The reflection coefficient of load is represented as $\Gamma_L = |\Gamma_L|\angle\phi$, where $|\Gamma_L| = 0.33$ and $\phi \in [0°, 360°]$.

1) *Resistive Loads*: For the load impedance corresponding to $\Gamma_L = 0.33\angle 0°$, i.e., $z_L = 2$, $|V_M|$ of the series mode exceeds the predefined limit and reaches to $3V_{DD}$, as shown in Fig. 10(c). This leads to hard compression of the PA, which strongly degrades the fidelity of waveform for radio transmission and causes reliability issues such as breakdown of the main device. However, if the QB-DPA is reconfigured to parallel mode at $z_L = 2$, $|V_M|$ can be well maintained below V_{DD}, as shown in Fig. 10(c), because of the respective $y_L = 0.5$ applied to the $|V_{M_{PL}}|$ expression in (23). For the symmetric resistive load, i.e., $z_L = 0.5$ and $\Gamma_L = 0.33\angle 180°$, the series mode is selected in which the main voltage $|V_M| < V_{DD}$ is enforced for the entire operation region, as shown in Fig. 10(d).
2) *Complex Loads*: For the conditions of $\Gamma_L = 0.33\angle 90°$ and $\Gamma_L = 0.33\angle 270°$, which correspond to the two reactive points $z_L = 0.8 + j0.6$ and $z_L = 0.8 - j0.6$, the main voltage profiles of series mode are the same for both loads, as shown in Fig. 10(e) and (f), respectively. Meanwhile, $|V_M|$ increases beyond V_{DD} after the auxiliary amplifier is turned on, but it remains $< 1.25\ V_{DD}$ toward the peak power. By replacing z_L with y_L, the above analysis can be repeatedly applied to the parallel mode. As a result, either series or parallel mode can be selected for these two sample complex loads, which are actually on the boundary of triggering mode reconfiguration, as shown in Fig. 10(a).

In addition to the voltage profiles, the symmetry between series and parallel modes is reflected with calculated efficiency in Fig. 10(b) as well. The efficiency can exceed 100%, which is realistically impossible due to the unlimited voltage overdriving (in the theoretical model) in certain load conditions, such as $Z_L = 2Z_0$ for series mode and $Y_L = 2Y_0$ for parallel mode. As a result, the selection of PA mode in a specific load condition should be prioritized for maintaining a nonoverdriven $|V_M|$. This is depicted with green tick in Fig. 10(c)–(f) as well, where for complex loads, both modes can be activated in view of the threshold of $|V_M|$. It is also interesting to note that, in both of the series and parallel configurations, $|V_A|$ remains below than V_{DD} and is independent of the load mismatch, as verified in (23).

B. Performance Enhancement for Mismatch Conditions: Analog Approach

As discussed in Section III-A, series/parallel mode reconfiguration can be leveraged to avoid the overdriving of the main amplifier device, but the efficiency is considerably degraded,

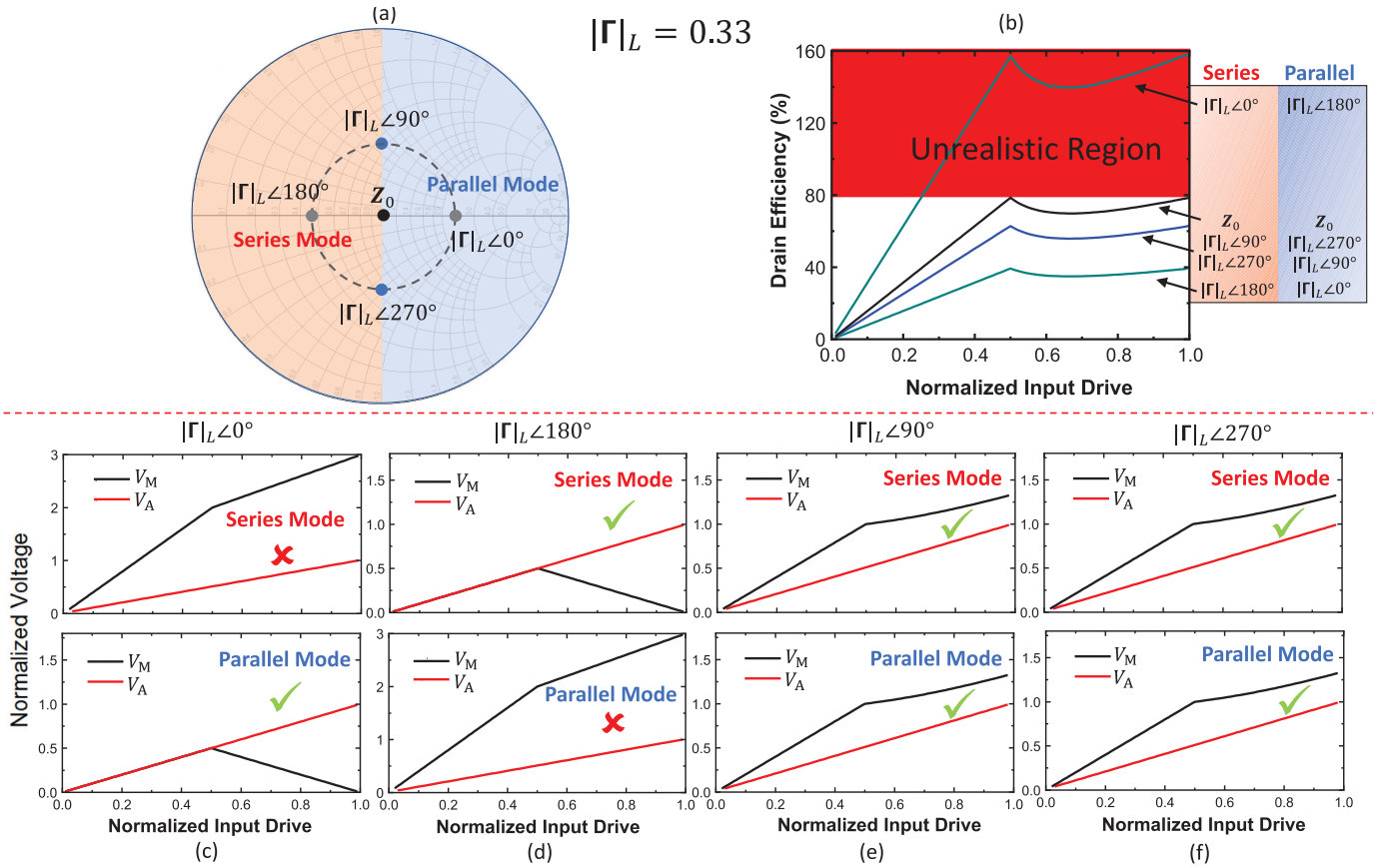

Fig. 10. Load mismatch analysis. (a) Representative cases on VSWR 2 : 1 circle. (b) DE profile induced by the mismatched load and voltages at series/parallel modes for the corresponding loads. (c) $|\Gamma_L|\angle 0°$. (d) $|\Gamma_L|\angle 180°$. (e) $|\Gamma_L|\angle 90°$, and (f) $|\Gamma_L|\angle 270°$.

especially for the resistive loads, as shown in Fig. 10(b). It is discovered that such a degradation can be mitigated by changing the gate bias of auxiliary amplifier and reactance/susceptance loading of the coupler at output. Expanding the ideal series/parallel modes in mismatch conditions described in (21)–(23), the detailed theoretical derivations with jx (jb) loading are derived and provided in the Appendix.

Graphical illustrations in Figs. 11 and 12 describe the effects of auxiliary gate biasing and jx (jb) loading on the QB-DPA operation under mismatch conditions. For the resistive mismatched loads, parallel mode for $z_L = 2$ ($\Gamma_L = 0.33\angle 0°$) and series mode for $y_L = 2$ ($\Gamma_L = 0.33\angle 180°$) are selected for avoiding the overdriving. With the ideal gate bias setting [corresponding to the driving currents in Fig. 2(a)], the auxiliary amplifier turns on when the voltage swing of the main amplifier is only half of saturation, while the load modulation further degrades the RF voltage to zero toward the maximum input driving level. Consequently, as indicated by the blue lines in Fig. 11(a) and (b), the overall DPA efficiency remains low. By increasing the auxiliary threshold (late turn-on), i.e., β, the main amplifier voltage can continue increasing toward the full saturation, leading to a enhanced efficiency (i.e., $>$ 60%) over the entire dynamic range, as indicated by the red lines in Fig. 11(a) and (b). Moreover, an appropriately small reactance (susceptance) at isolation port can be utilized to further shape the main voltage and efficiency profiles of series (parallel) mode, but an excessively large jx (jb) can lead to failure of the load modulation, as shown in Fig. 11(a) and (b).

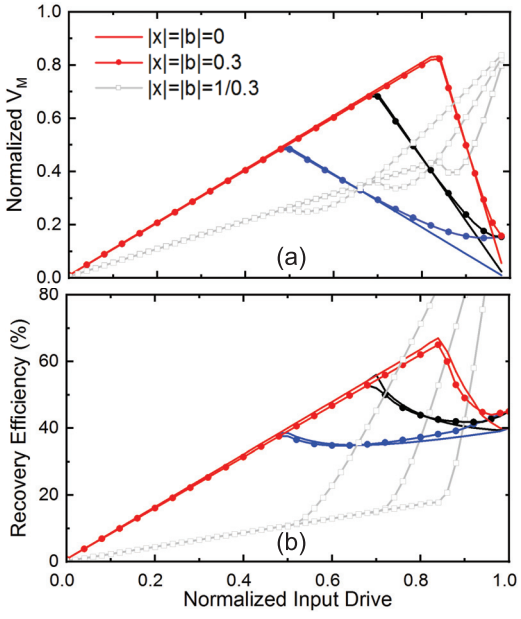

Fig. 11. Illustration of (a) voltage and (b) efficiency recovery for $\Gamma_L = 0.33\angle 0°$ at parallel mode and $\Gamma_L = 0.33\angle 180°$ at series mode, respectively.

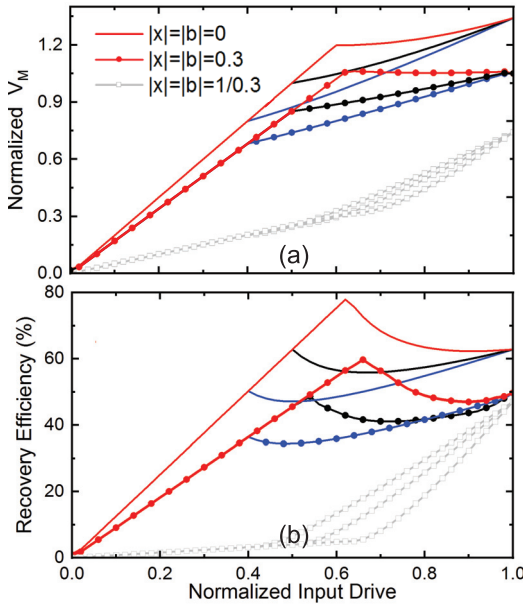

Fig. 12. Illustration of (a) voltage and (b) efficiency recovery for $\Gamma_L = 0.33\angle 90°$ and $\Gamma_L = 0.33\angle 270°$ at both series and parallel modes.

For the complex mismatched loads of $z_L = 0.8 \pm j0.6$, the main voltage is slightly overdriven for ideal series/parallel QB-DPA mode, i.e., $|V_M| = 1.25|V_{DD}|$ around saturation point. Though this is possibly tolerable with harmonic tuning, the reactance/susceptance loading at the isolation port can be leveraged to mitigate this overdriving issue, as shown in Fig. 12(a). In series mode for example, by setting $|x| = 0.3$ and slightly increasing the turn-on threshold to $\beta = 0.6$ as the red dotted line shown in Fig. 12, the profile of $|V_M|$ can be flattened throughout the load-modulation region and maintained below $|V_{DD}|$, leading to enhanced QB-DPA efficiency of up to 60% correspondingly. Due to the symmetrical distribution of the complex loads in the Smith chart, the effects of the performance recovery is identical for $\Gamma_L = 0.33\angle 90°$ and $\Gamma_L = 0.33\angle 270°$, while either series or parallel mode can be selected with the same performance.

To sum up, it is proved feasible to exploit adaptive gate biasing synthesis of auxiliary amplifier in conjunction with reactance (susceptance) loading at isolation port for compensating the efficiency and linearity under a certain extent of load mismatch, e.g., VSWR 2 : 1 loads. It is also important to point out that this quasi-short/quasi-open loading resonates perfectly with the linearity-enhanced QB-DPA theory presented in Section II-C. In practical designs, the jx (jb) loading and gate biasing can be utilized as tuning knobs for optimizing the efficiency and linearity for both matched and mismatched conditions.

IV. Prototype Design and Demonstration

Based on the linearity-enhanced QB-DPA theory and the mismatch-resilient series/parallel mode reconfiguration, the practical design methodology is presented. A physical prototype is designed and implemented using GaN devices and branch-line quadrature couplers operating at a center frequency of 3.5 GHz.

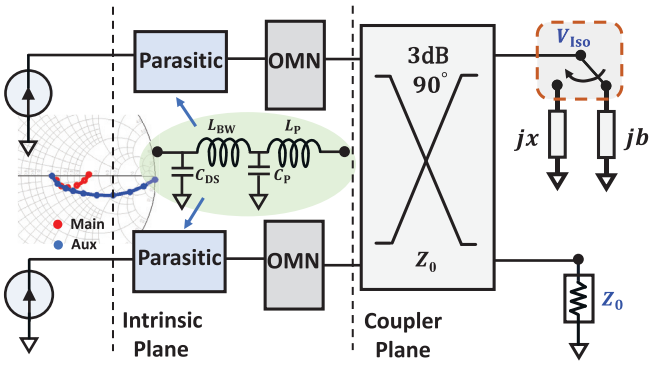

Fig. 13. Symmetrical series and parallel load-modulation behaviors at device plane in realistic design.

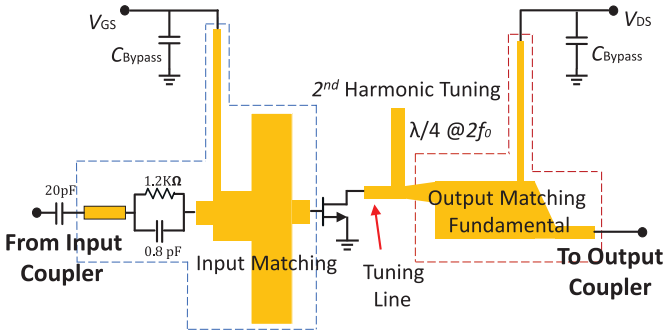

Fig. 14. Schematic of the designed IMN and OMN of standalone PA.

A. Design of Linearity-Enhanced QB-DPA at Nominal Condition

Fig. 13 shows the output combiner of the linearity-enhanced QB-DPA including the parasitics of the transistors contributed by the GaN chip and package. The output matching network (OMN) of the two paths is designed with identical topology for maintaining the consistent QB-DPA behavior over series/parallel alternation. Moreover, the reconfiguration for series/parallel linearity-enhanced QB-DPA can be realized through adaptive gate biasing and switching the isolation-port loading of output quadrature coupler. Practically, the RF switch can be implemented with a commercial SPDT silicon-on-insulator (SOI)-based (SKYA21003), which consists of three ports: antenna (ANT), RF1, and RF2. The analysis of the switch implementation has been thoroughly elaborated in [21] and [22]. The symmetry between series and parallel QB-DPAs is still valid (from the coupler plane to intrinsic drain plane), if two sub-PAs are designed identically, as shown in Fig. 13.

The OMN is devised to offer linearity-prioritized matching at both fundamental and second harmonic frequencies, as shown in Fig. 14. A tuning line lays between the drain term and second-order frequency stub can supply an optimal imaginary part for the transistor while ensuring the fundamental output matching presenting minimum influence with the harmonic matching [47]. Meanwhile, the design of input matching network (IMN) provides a certain mismatch for perfecting the linearity with slightly AM-AM compression

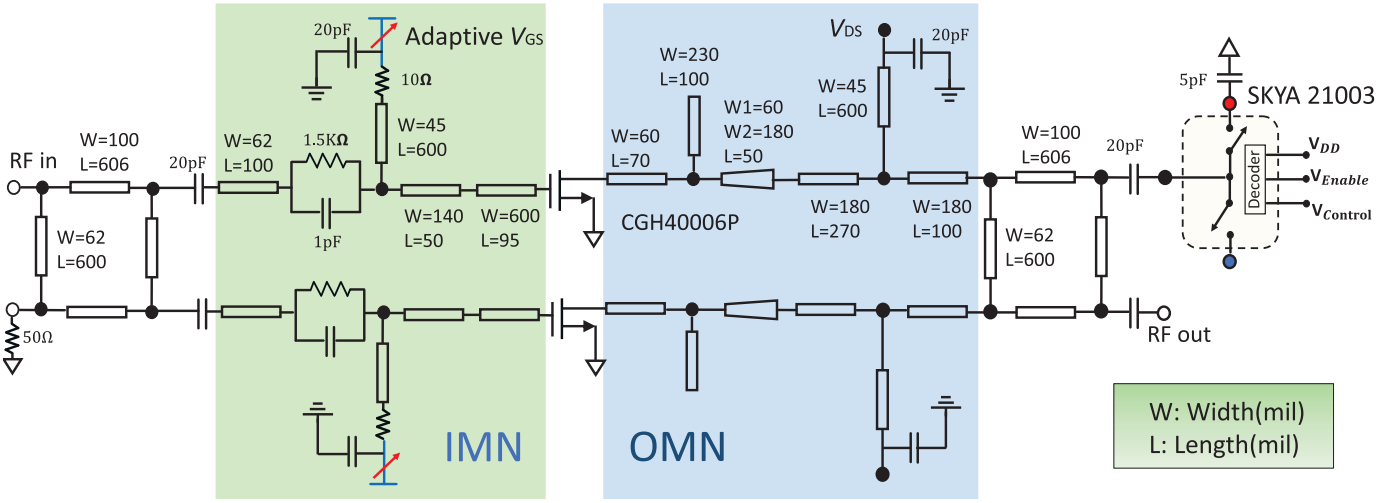

Fig. 15. Full schematic of the designed reconfigurable QB-DPA with an SOI-based SPDT switch.

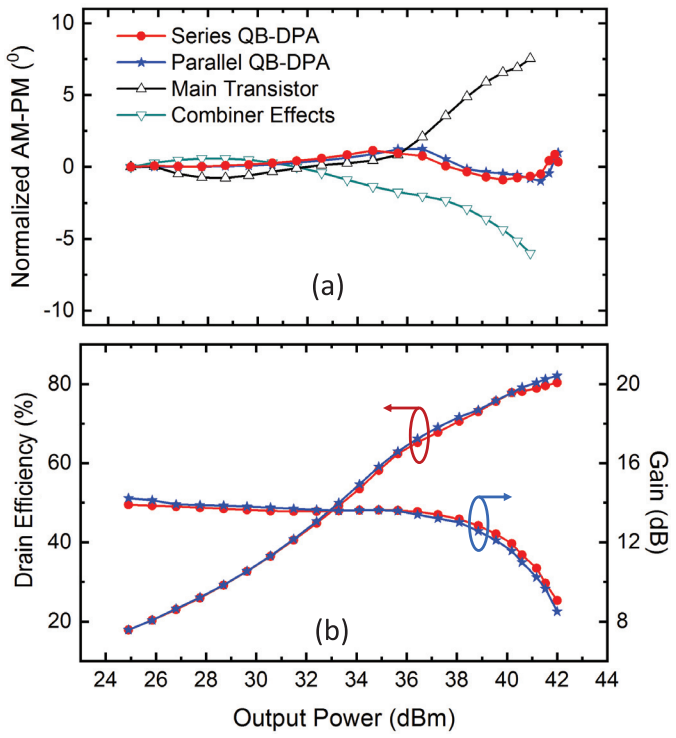

Fig. 16. Simulation results of the QB-DPA at 3.5 GHz. (a) AM-PM. (b) DE and gain.

using the similar approach presented in [22], which is not discussed in detail here.

According to the above design considerations, the entire circuit is cosimulated with the circuit models and electromagnetic (EM) model of layout using Keysight ADS. The overall schematic is presented in Fig. 15 with the switchable loading at the isolation port of output coupler. Fig. 16 shows the simulated AM-PM, DE, and gain of the proposed DPA at 3.5 GHz. By terminating the isolation port of the output coupler to a large shunt capacitor of 5 pF, the proposed reactance combiner network provides a complementary AM-PM response to that of the main transistor with around 6°, leading to effective compensation of the overall phase distortion, as shown in Fig. 16(a). Interestingly, through extensive optimization, a quasi-open-circuited isolation-port loading (0.1–0.2 pF of capacitance) is found to generate the best AM-PM compensation of parallel QB-DPA shown in Fig. 16(a). This capacitive loading can be physically realized by the OFF-state parasitics (C_{OFF}) of the CMOS SOI switch with the corresponding port (RF2) in floated connection, as shown in Fig. 15. It is worthy to note that the value of jx (jb) loading is determined through the overall circuit simulation, and the discrepancy from theory and emulation is mainly due to the use of realistic matching circuits. Similar to the series mode, the parallel mode also presents minimized distortion of the AM-PM profile in Fig. 16(a). Overall, the AM-PM variation is maintained within ±1° across the entire dynamic power range for both series and parallel modes. Meanwhile, an 80% saturation efficiency and a 60% efficiency at 6-dB power back-off are simultaneously achieved, as shown in Fig. 16(b), while achieving a flat AM-AM response for both modes.

B. Mode Reconfiguration for VSWR Resilience

As discussed earlier, the PA linearity can be enhanced in either series mode or parallel mode at nominal 50-Ω load, especially in the load-modulation region. For an arbitrary mismatched load, Z_{L} (or Y_{L}), a proper operational mode (series/parallel) should be configured in order to optimize the DE, linearity, and output power. Fig. 17 shows how the mismatch-induced degradation is mitigated through mode reconfiguration and adaptive biasing over the entire 2 : 1 VSWR circle. Since the mismatch effects on series and parallel modes are symmetrical to z_{L} and y_{L}, respectively, the simulation results presented in each of the subfigures from Fig. 17(a)–(d) correspond to a pair of loads that are symmetric with respect to the origin of Smith chart.

Specifically, for the mismatched resistive loads $|\Gamma_L|\angle 0°$ and $|\Gamma_L|\angle 180°$ in Fig. 17(a), with the modes reconfiguration,

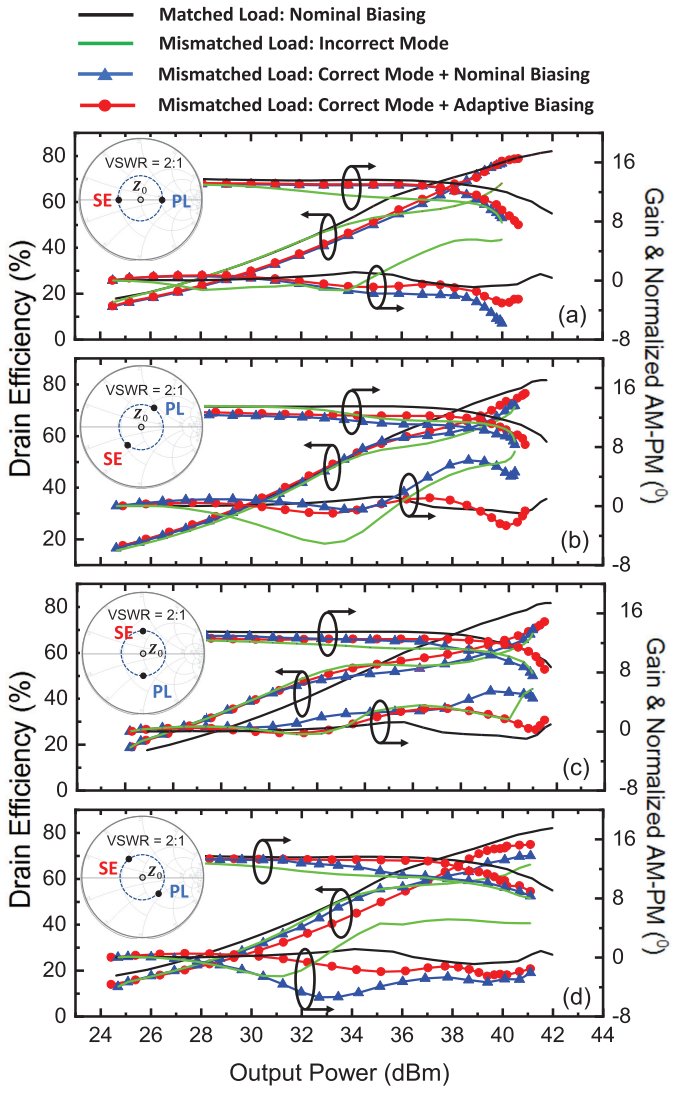

Fig. 17. Simulated gain, DE, and AM-PM recovery for the illustrative mismatched loads. Minor differences in results between symmetrical conditions, i.e., SE mode @z_L and PL mode @$1/z_L$, are omitted for clarity of plotting.

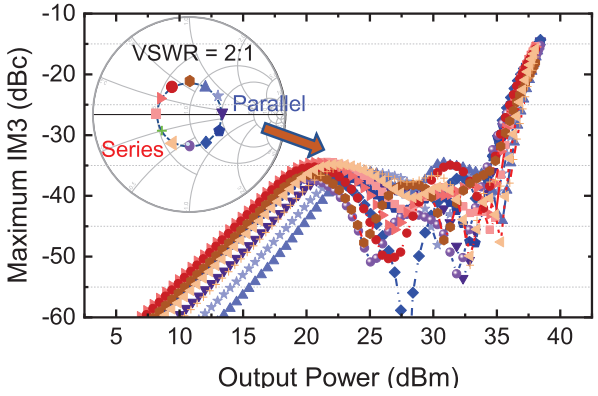

Fig. 18. Two-tone simulation to verify IM3 recovery through reconfiguration of series/parallel modes.

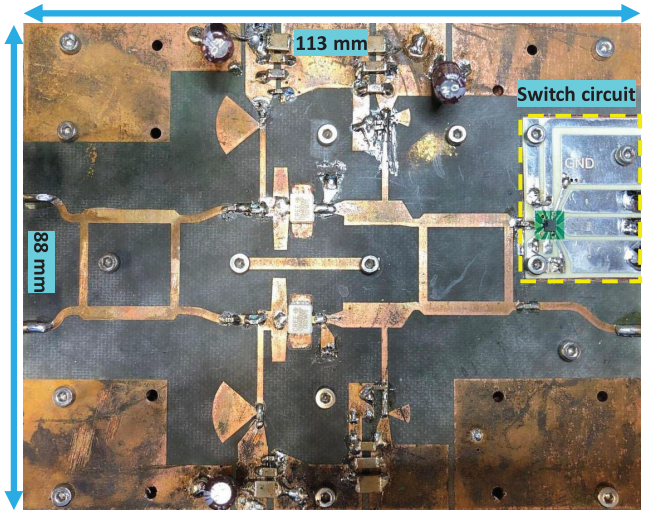

Fig. 19. Top view of the fabricated circuit board.

the efficiency can be well recovered at saturation and 6-dB back-off regions along with an improved gain profile (early compression modified), which effectively compensates for the incorrect-mode-induced degradation. Moreover, the AM-PM distortions are significantly mitigated to $< \pm 2.8°$ for the load-modulation region, which varies only $< \pm 1°$ in the matched load scenario due to the adaptive gate biasing. Complex loads in Fig. 17(b) and (d) exhibit the corresponding improvements as well, while both modes can be applied for the mismatched loads of $|\Gamma_L| \angle \pm 90°$ in Fig. 17(c), which agrees with the theoretical illustration in Fig. 10(e) and (f).

To further evaluate the linearity of reconfigurable QB-DPA, a two-tone simulation with frequency spacing of 10 MHz centered at 3.5 GHz is conducted to extract the third-order intermodulation (IM3) under load mismatch at 2 : 1 VSWR circle. The simulated maximum IM3 is plotted in Fig. 18. With the mode reconfiguration and the bias voltage adjustment of main/auxiliary PAs, the IM3 level can be kept consistently below −35 dBc (before compression) all over the entire 2 : 1 VSWR circle.

V. Fabrication and Measurement Results

The overall layout is generated from the circuit schematic, and it is electromagnetically modeled using the ADS Momentum simulator. The EM model is then cosimulated with active components, and the layout is optimized until the cosimulation results match the schematic-only case. The fabricated QB-DPA is shown in Fig. 19, which is developed on the Rogers 5880 substrate, and the entire PCB is mounted on a copper substrate and fastened using screws. The RF switch module is placed on another small PCB board, and it is mounted on the same copper substrate with RF connection to the isolation node of the output quadrature coupler. By applying different bias setting of the switch control, the ANT port of the SPDT switch can be routed to RF1 (5 pF) and open circuit (both RF1 and RF2 are OFF via the enable function of switch) alternatively. The design implemented with two identical transistor devices for main and auxiliary PAs. To experimentally demonstrate the reconfig-

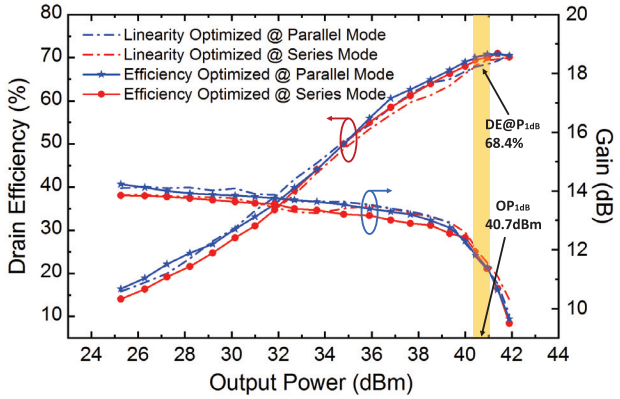

Fig. 20. Measured DE and gain versus output power centered at 3.5 GHz.

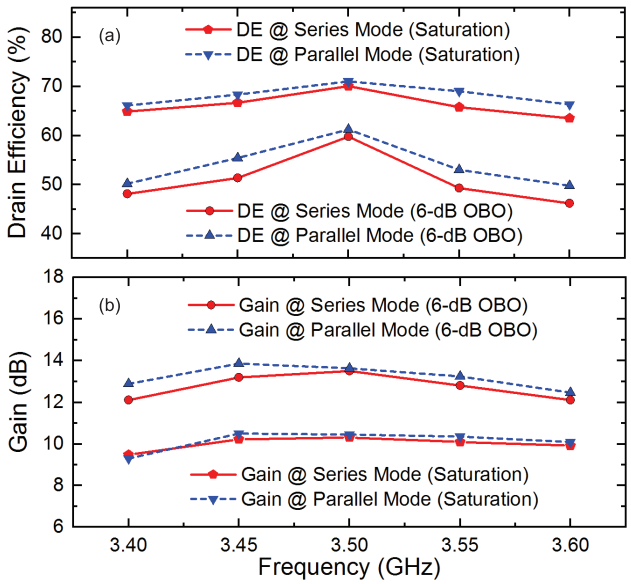

Fig. 21. Measured frequency response at peak and 6-dB OBO for series and parallel modes: (a) DE and (b) gain.

urable operation, the designed QB-DPA is evaluated with both the continuous waveform and Long-Term Evolution (LTE) modulated signal at series and parallel modes, respectively.

A. Continuous-Wave Measurement

In the series QB-DPA mode measurement, the gate bias of the main device is primarily set to −2.55 V in Class-AB in order to improve the linearity at low-power range. The auxiliary is set to class-C type with gate bias voltage as −4.55 V to compensate for overall AM-PM. In the parallel QB-DPA mode measurement, the gate biases of two PAs are exchanged and slightly adjusted with V_{GS} set as −4.65 V for the auxiliary device and −2.5 V for the main cell, respectively.

Fig. 20 shows the measured DE and gain versus the output power driven by a power-swept continuous-wave (CW) stimulus at both series and parallel mode. The desired Doherty profile is experimentally obtained with efficiency-optimized bias in both modes. It is important to note that the designed QB-DPA presents a high low-power gain around 14 dB at the center frequency of 3.5 GHz, and it remains flat up to P_{1dB} region. Such a linear AM-AM behavior agrees well with

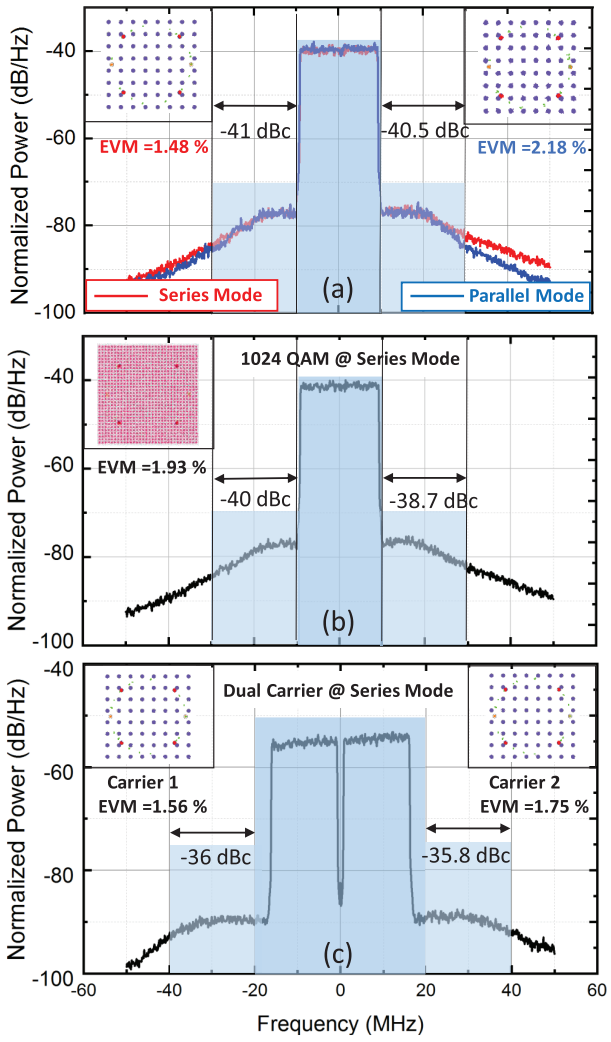

Fig. 22. Measured PSD, Adjacent Channel Power Ratio (ACPR), and EVM at 3.5 GHz without DPD. (a) At series/parallel modes under a 20-MHz modulated signal with 64-QAM. (b) At series mode under a 20-MHz modulated signal with 1024-QAM. (c) At series mode under dual-carrier 40-MHz modulated signal for 64-QAM.

the simulation results in Fig. 16(b). The measured efficiency at P_{Max} is almost the same for both modes at the operating center frequency attributed to the identical loadline at a saturation region, while a higher DE profile at 6-dB back off region is presented at parallel mode due to a smaller current consumption. Meanwhile, the frequency response of the PA is evaluated across 3.4–3.6 GHz, as shown in Fig. 21. In the series mode, the measured DE is 63.5%–70.1% at the peak output power, and the gain is 9.4–10.3 dB. At 6-dB output back-off (OBO), the measured gain and DE are 12.1–13.5 dB and 46.2%–59.8%, respectively. The realistic parallel mode is not exactly symmetrical to the series mode, which presents a comparatively higher performance in terms of DE and gain over the entire dynamic power range. This is mainly due to the fabrication tolerance and part-to-part variation of two GaN transistors.

B. Modulated Measurement With Nominal 50-Ω Termination

The efficiency and linearity of the reconfigurable series/parallel QB-DPA were assessed under various

TABLE I
COMPARISON WITH STATE OF THE ART OF RECENTLY REPORTED LINEAR GaN PAs

Ref.	f_0 (GHz)	Architecture	Technology	P_{avg} (dBm)	Mod. BW (MHz)	Average DE (%)	ACPR w/o DPD (dBc)
[22]	3.5	B2D PA†	GaN/Hybrid	34.5	10	42.4	−37
[41]	5	2-Way Doherty	GaN/Hybrid	32	120	42	−43.1
[42]	2.14	2-Way Doherty	GaN/Hybrid	35.5	20	44	−40.5
[43]	0.8	DPA w Linearizer	GaN/Hybrid	33	20	33.2	−42.5
[44]	7	2-Way Doherty	GaN/MMIC	27.7	20	43	−41
[45]	7	2-Way Doherty	GaN/MMIC	32	56	41	−36
[48]	3.5	2-Way Doherty	GaN/Hybrid	35.8	20	62	−27.9
[49]	2.3	2-Way Doherty	GaN/MMIC	35.2	10	46	−35.6
[50]§	5	2-Way Doherty	GaN/Hybrid	36	5	57.8*	−30
[51]	2.0	2-Way Doherty	GaN/Hybrid	33	5	54	−30
[52]	2.1	2-Way Doherty	GaN/Hybrid	40	5	55	−30
This Work	3.5	SE/PL QB-DPA **	GaN/Hybrid	35	20	45	−41

† QB-DPA mode. § Measured using two-tone signal with 5-MHz tone spacing. ∗ Maximum CW PAE at an IMD3 of -30 dBc.
∗∗ Series QB-DPA mode.

modulation bandwidth (e.g., 20 and 40 MHz) and QAM formats (e.g., 64 QAM and 1024 QAM) using an LTE signal with 9.6-dB PAPR. The measured power spectral density (PSD) and the error vector magnitude (EVM) are shown in Fig. 22. At series mode, the designed QB-DPA PA presents an average efficiency of 45% and ACPR around −41 dBc at a rated average output power of 35 dBm without any DPD applied. A low corresponding EVM of 1.48% is measured in this condition, as shown in Fig. 22(a), whereas an EVM of 2.18% at parallel mode is obtained corresponding to a −40.1 dBc ACPR at 33.8-dBm output power region. The measurement results under 20 MHz with 1024 QAM at series mode are expressed in Fig. 22(b). A decent linearity of 1.93% EVM and −40 dBc is achieved. Furthermore, the designed PA is evaluated under carrier-aggregated 40-MHz modulated signal, and the EVM of 1.56% and 1.75% and the ACPR of −36 and −35.8 dBc are recorded at adjacent power channels, respectively.

The PA is further tested using a power-swept LTE signal with the same 20-MHz bandwidth and 64 QAM modulation, and the DE and gain versus the average output power are plotted in Fig. 23(a). The profiles of EVM and ACPR are presented as well in Fig. 23(b). Based on the measurement in Fig. 23, at both series/parallel modes, the designed QB-DPA maintains a low EVM less than 4.2% and a raw ACPR between −30.6 and −41 dBc below 37.2-dBm output power area, while the corresponding average efficiency can be up to 47.3%.

Table I summarizes the state of the art of series/parallel QB-DPA compared to other contemporary linear GaN-based PAs published recently. The proposed QB-DPA offers a very competitive design achievement in terms of the maximum rated output power, average DE, and raw ACPR. Specifically, compared with the designs in [22] and [42]–[45], the proposed QB-DPA exhibits the lower ACPR evaluated with the same modulation bandwidth while maintaining larger DE. Meanwhile, excellent output power and average DE are obtained with an impressive ACPR comparable to [41] and [48]–[52], which clearly exhibits better linearity–efficiency and well verifies the effectiveness of the proposed theory.

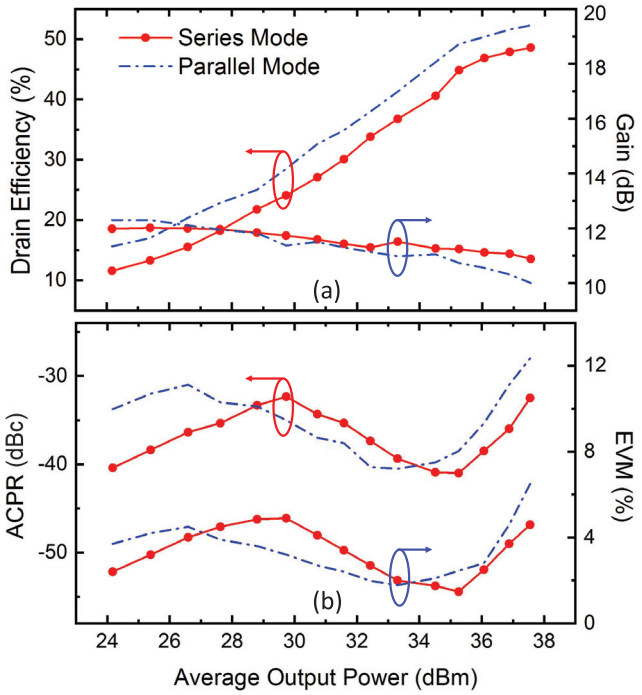

Fig. 23. (a) DE and gain and (b) EVM and ACPR versus average output power under modulated signal with 20-MHz modulation bandwidth and 64 QAM.

C. Reconfigurable-Mode Measurement Under Load Mismatch

The designed QB-DPA is evaluated with CW as well as single-carrier 64 QAM 20-MHz bandwidth modulated signal (used in Sec. V-B) under load mismatch at various VSWRs up to 2.5 : 1 to demonstrate the reconfigurable operation. A functional configuration of the measurement system setup is shown in Fig. 24. A driver stage (ZHL-5W-422+) provides power level, and a directional coupler after isolator is used to accurately sample and measure the input power. The DUT output, at this stage, is connected to a mismatched load where VSWR > 1 spanning the 360 phase with the designed impedance transformer. Finally, a Keysight PXIe

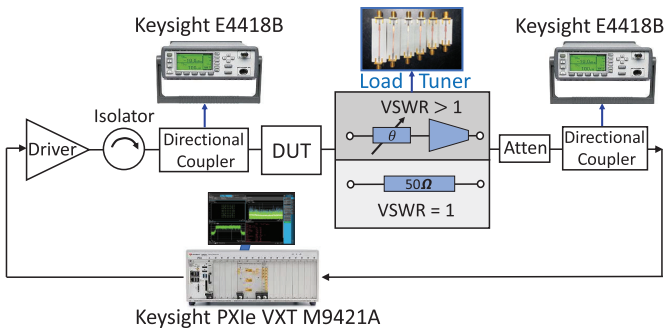

Fig. 24. Measurement setup for characterization of the series/parallel QB-DPA under nominal 50-Ω and mismatch loading (VSWR > 1) conditions.

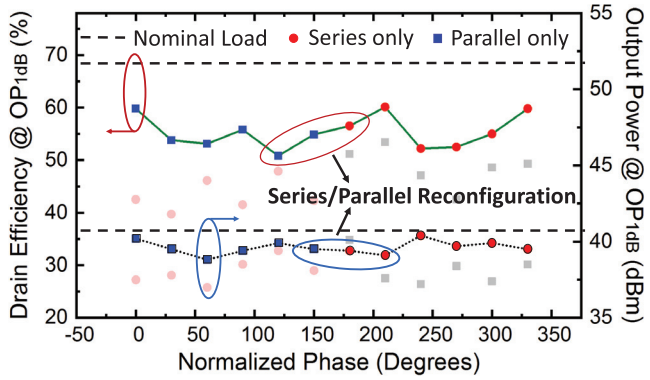

Fig. 25. Measured DE and $OP_{1\,dB}$ over 2:1 VSWR with CW signal.

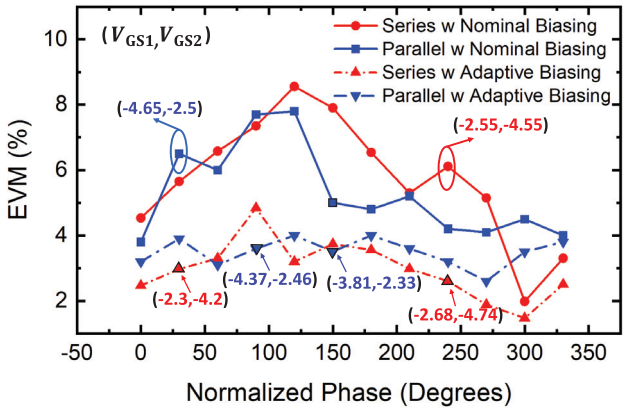

Fig. 26. EVM at 2:1 VSWR with modulated signal under nominal biasing and adaptive biasing.

vector transceiver (VXT M9421) is used as CW/modulated signal generator and analyzer.

The designed QB-DPA is first characterized with a CW signal covering 2:1 VSWR circle with a 30° step of the phase swept. The load tuner as shown in Fig. 24 is physically realized using an impedance transformer in series to a set of transmission lines with different electrical lengths. As shown in Fig. 25, with reconfiguration, the DE at the 1-dB compression point ($OP_{1\,dB}$) can be significantly improved over entire 2 : 1 VSWR. Moreover, a consistent $OP_{1\,dB}$ of 38.8–40.4 dBm is maintained guaranteeing a stable output power to mitigate

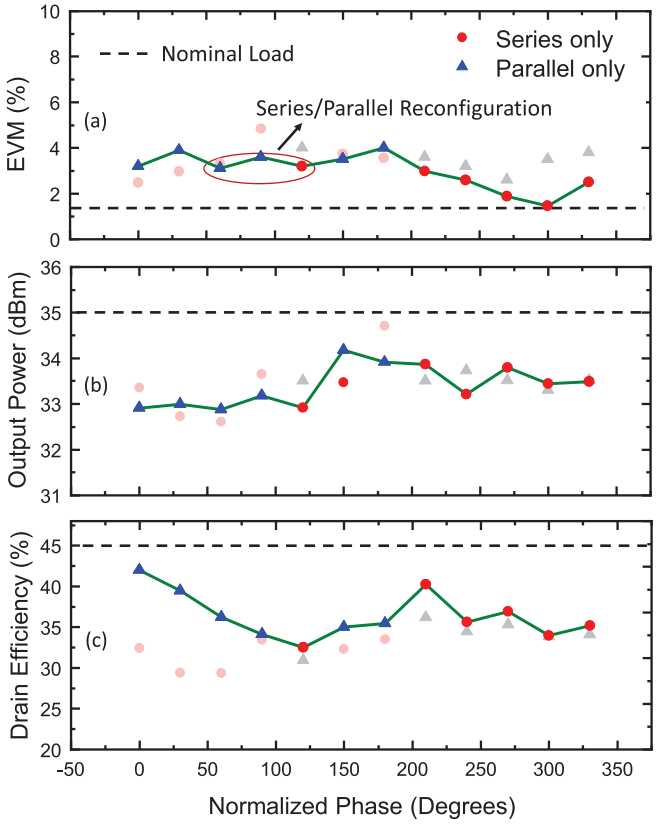

Fig. 27. Modulation signal measurement of reconfigurable series/parallel PA under 2 : 1 VSWR over entire phase range: (a) EVM, (b) output power, and (c) average DE.

the impedance mismatch-induced power degradation. Then, the modulation measurement is conducted, which begins with series/parallel modes of QB-DPA under 2 : 1 VSWR. An EVM comparison between the nominal biasing (retained biasing setting as in Fig. 22 for certain realistic scenarios with fixed biasing) and adaptive biasing (biasing recombination for best EVM at the same input power level) is shown in Fig. 26, where the bias voltages are indicated for certain points to show the linearity enhancements obtained. It should be noted that the above results along with the following varied VSWR test are driven with a constant input power of 21 dBm for a fair and meaningful comparison.

Fig. 27 shows the EVM, output power, and DE versus the varying phase along the 2 : 1 VSWR circle. A < 4% of EVM is set as a specific benchmark in this design, which can be respecified based on the various communication standards. In Fig. 27(a), at series mode, a low EVM (< 4%) can be achieved for the majority of phases on the 2 : 1 VSWR circle, with the corresponding output power between 32.6 and 34.5 dBm shown in Fig. 27(b). For the rest of the phases not meeting the linearity spec, the parallel mode is activated through the switching between the main and auxiliary biasing and coupler isolation ports at out-end via the SPDT switch. It is worthy to point out that an efficiency priority is targeted for certain phase points that EVM is comparable between series/parallel modes, which can be seen in Fig. 27(c). The EVM of parallel

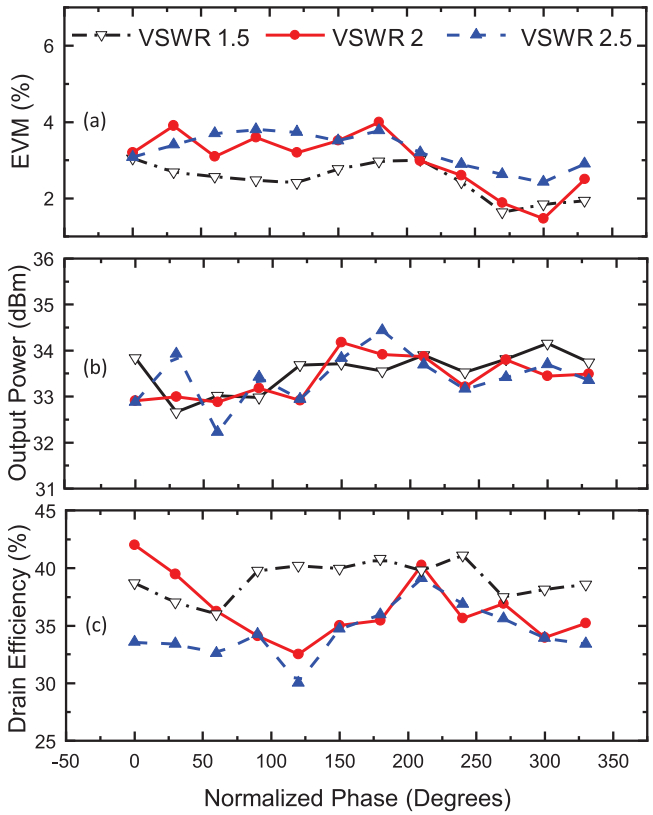

Fig. 28. Modulation signal measurement of series/parallel QB-DPA under variable VSWR over entire phase range: (a) EVM, (b) output power, and (c) average DE.

mode slightly degrades, while a significant improvement of efficiency can be observed. To further experimentally demonstrate the reconfigurable operation, the designed QB-DPA is evaluated under variable VSWR up to 2.5 : 1. Note that a fine adjustment of gate biasing is implemented to optimize the linearity of the dedicated QB-DPA modes toward different mismatch conditions. Fig. 28 shows the optimal results obtained via series/parallel reconfiguration on the full VSWR circle of 1.5 : 1, 2 : 1, and 2.5 : 1. The proposed series/parallel QB-DPA presents the capability to constantly maintain a low EVM, stable output power, and substantially recover the DE when subjected to the load mismatch.

VI. Conclusion

In this article, a series/parallel mode-reconfigurable QB-DPA is proposed and analyzed. It is for the first time theoretically verified that a QB-DPA can be reconfigured between series and parallel modes by switching the roles of main and auxiliary amplifiers along with the isolation loading of output coupler. Furthermore, the theory of linearity-enhanced series/parallel QB-DPA is analyzed as an extension from generic QB-DPA. Moreover, by leveraging the symmetry of series/parallel modes with complementary sensitivities to load impedance/admittance, the QB-DPA is analytically proved to be VSWR-resilient. A reconfigurable QB-DPA prototype is implemented to verify the proposed concept at 3.5 GHz. In the nominal case driven with the LTE modulated signal with 20-MHz bandwidth, the measured PA exhibits −41-dBc ACPR at series mode, allowing it to achieve 1.48% EVM at the maximum $P_{\text{rated}} = 35$ dBm without any additional digital linearization performed. In the parallel mode, a 2.18% EVM corresponding to −40.1-dBc ACPR is obtained at $P_{\text{rated}} = 33.8$ dBm. Meanwhile, when suffering from the load mismatch, the designed QB-DPA also maintains the high linearity and efficiency up to 2.5 : 1 VSWR circle via the two-state reconfiguration of the loading capacitor and optimized gate biasing. Overall, the proposed reconfigurable QB-DPA offers a compelling solution for realizing energy efficient and highly robust massive MIMO system.

Appendix

In Section III-A, when the output coupler driven with a mismatched load (z_{L} or y_{L}) and reactance/suscpetance (jx or jb) at the isolation port, the impedance observed by the main and auxiliary transistors has the following solutions at series mode:

$$Z_{\text{M}_{\text{SE}},\text{bo}} = \frac{2}{jx + \frac{1}{z_{\text{L}}}} Z_0 \;\&\; Z_{\text{A}_{\text{SE}},\text{bo}} = \infty \tag{24}$$

$$Z_{\text{M}_{\text{SE}},\text{sat}} = \frac{2z_{\text{L}} - 2}{jxz_{\text{L}} + 1} Z_0 + Z_0$$

$$Z_{\text{A}_{\text{SE}},\text{sat}} = \frac{2x - 2xz_{\text{L}}}{xz_{\text{L}} - j} Z_0 + Z_0. \tag{25}$$

Meanwhile, the voltages V_{Main} and V_{Aux} can be expressed as

$$V_{\text{M}_{\text{SE}}}(x, z_{\text{L}}) = \frac{2I_{\text{M}}z_{\text{L}} + jxI_{\text{A}}z_{\text{L}} - I_{\text{A}}}{jxz_{\text{L}} + 1} Z_0 \tag{26}$$

$$V_{\text{A}_{\text{SE}}}(x, z_{\text{L}}) = -j\frac{I_{\text{M}} - jxI_{\text{A}}z_{\text{L}} + j2xI_{\text{A}}}{jxz_{\text{L}} + 1} Z_0. \tag{27}$$

Furthermore, the output voltage of the proposed QB-DPA represented by the following equation:

$$V_{\text{L}_{\text{SE}}}(x, z_{\text{L}}) = \frac{-\sqrt{2}I_{\text{M}}z_{\text{L}} - j\sqrt{2}xI_{\text{A}}z_{\text{L}}}{jxz_{\text{L}} + 1} Z_0. \tag{28}$$

Similarly, at parallel mode

$$Z_{\text{M}_{\text{PL}},\text{bo}} = \frac{2}{jb + \frac{1}{y_{\text{L}}}} Z_0 \;\&\; Z_{\text{A}_{\text{PL}},\text{bo}} = \infty \tag{29}$$

$$Z_{\text{M}_{\text{PL}},\text{sat}} = \frac{2y_{\text{L}} - 2}{jby_{\text{L}} + 1} Z_0 + Z_0$$

$$Z_{\text{A}_{\text{PL}},\text{sat}} = \frac{2b - 2by_{\text{L}}}{by_{\text{L}} - j} Z_0 + Z_0. \tag{30}$$

Also, the voltages V_{Main} and V_{Aux} can be shown to be

$$V_{\text{M}_{\text{PL}}}(b, y_{\text{L}}) = -j\frac{2I_{\text{M}}y_{\text{L}} + jbI_{\text{A}}y_{\text{L}} - I_{\text{A}}}{jby_{\text{L}} + 1} Z_0 \tag{31}$$

$$V_{\text{A}_{\text{PL}}}(b, y_{\text{L}}) = \frac{I_{\text{M}} - jbI_{\text{A}}y_{\text{L}} + j2bI_{\text{A}}}{jby_{\text{L}} + 1} Z_0 \tag{32}$$

$$V_{\text{L}_{\text{PL}}}(b, y_{\text{L}}) = \frac{-\sqrt{2}I_{\text{M}} - j\sqrt{2}bI_{\text{A}}}{jby_{\text{L}} + 1} Z_0. \tag{33}$$

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