Digital Defect Based Built-in Self-Test for Low Dropout Voltage Regulators

Mehmet Ince and Sule Ozev
School of Electrical, Computer, and Energy Engineering Arizona State University

***Abstract*—With the increasing complexity of electronic components in critical applications, pressure on single components to have zero defects is also increasing. Thus there is a need to explore built-in self-test and other non-traditional test techniques for mixed-signal circuits, such as data converters, phase locked loops and power converters. In this paper, we present an extremely low cost, digital built-in self-test methodology for Low Dropout Regulators (LDO), specifically used for defect detection. The technique relies on perturbing the LDO loop at the reference voltage input via pseudo random binary sequence which has white noise characteristics and cross correlating the output of LDO with input excitation using only digital circuits, thus inducing low power and area overhead. The built-in self-test technique together with an LDO is designed using 65nm TMSC technology. Transistor level structural fault simulations display that all inserted faults can be detected even if they do not change the DC level of the LDO output.**

I. Introduction

Pseudo Random Binary Sequence (PRBS) based cross-correlation ideally can be used in any circuit architecture which can be modelled as a Linear Time Invariant (LTI) system [1]. However, PRBS-based BIST has generally been used in switched mode coverters due to the already digital nature of the designs

Applying cross correlation based system identification method for LDOs is more challenging since unlike switch-mode DC-DC converters, LDOs are in continuous time domain. In [2], a BIST method based on cross-correlation is implemented for LDOs to measure their phase margin from impulse response. In [2], the continuous LDO output is integrated and cross-correlated in the analog domain using an analog multiplier. Then, the integrated signal is sampled and converter into the digital domain via an ADC to obtain the final output. While this technique enables very accurate characterization of the LDO phase margin, it requires extensive analog circuit design expertise and is not easily portable to new designs. Moreover extensive use of analog circuits makes the technique not scalable. Recently, a fully digital BIST technique using PRBS based cross correlation is applied to PLLs [3] which alleviates the problems posed by analog implementation. However, PLLs contain digital signals that can be directly manipulated to obtain the cross-correlation and therefore the design process presented in [3] is not directly applicable to LDOs since all the signals in their loop are still in the analog domain. In this paper, we propose an all-digital cross-correlation based system identification method for defect based testing of LDOs. The proposed defect-oriented LDO BIST technique utilizes the PRBS injection at one location and cross-correlation with the output response in the digital domain without breaking the LDO loop. The proposed method presents with numerous advantages over previously proposed methods in terms of scalability, design re-use, fully digital output, and extremely low area overhead.

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II. Proposed Method

The proposed BIST technique is based on exciting the loop of LDO at the reference voltage input with a small magnitude, digital white noise surrogate and observing the response at the output [2], [4]. The excitation signal is a digital PRBS, which is chosen because of its white noise-like characteristics. The use of PRBS allows us to capture the impulse response and also loop transfer function within the bandwidth of the PRBS, namely $f_{PRBS}/2$, where f_{PRBS} is the bit rate of the PRBS stream. By adjusting the bit rate, we can observe as large or small frequency slice as needed.

The main concept of using this method for defect-based testing is that any particular defect in the loop will alter the response of the block it is in and eventually the loop transfer function of the LDO. Loop responses can be calculated between random two nodes in a closed loop system. Since block responses change with the defects regardless of the nodes selected for the calculation, defect will alter the measured loop response.

When V_{ref} of LDO is modulated by PRBS, the output will swing on top of the set DC value. Cross-correlation of this small AC voltage swing with the PRBS will yield the impulse response of the LDO loop. For cross-correlation, we propose converting this small AC signal to a 1-bit digital signal and observe it for a long PRBS sequence. While the information content for each PRBS bit will be small, it will accumulate over time via the cross-correlation and will provide comparably accurate results to executing cross-correlation in the analog domain.

Analog correlation requires integration of the AC swing at the output node. To accumulate the AC signal, the DC component needs to be removed via a high pass filter with a very low cut-off frequency. The accumulated signal needs to be converted to the digital domain after the correlation, which requires an ADC with a much higher resolution. In [2] for example, an 8 bit ADC is used. The problem with high resolution requirement can be solved by converting the output swing to the digital domain for a longer observation duration. Thus, a 1-bit ADC (simple comparator) can capture the information at the output. This process is similar to how a random sequence with a 1-bit resolution (PRBS) has the properties of a white noise.

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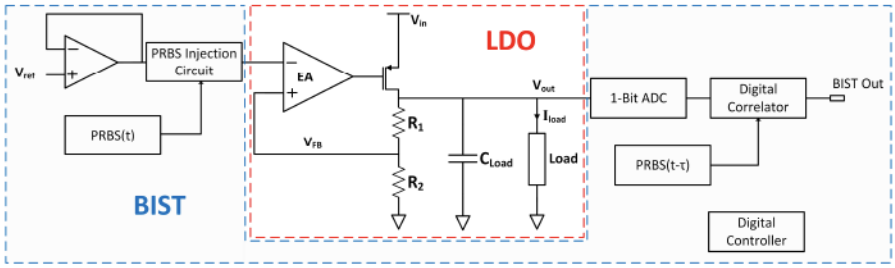

Figure 1: Block diagram of proposed LDO BIST architecture

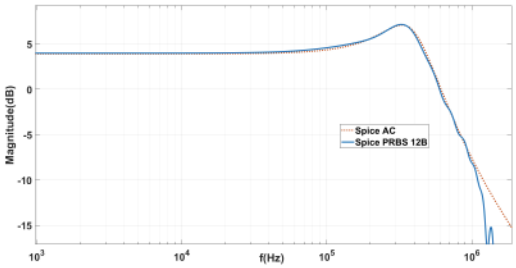

Figure 2: Transfer Function comparison between AC analysis in Spice and BIST

Therefore, the proposed BIST system for the LDO using the PRBS-based cross-correlation concept is shown in Figure 1. In summary, the voltage reference at the input of the LDO is modulated with a PRBS signal. Then, the output AC swing is converted to a 1-bit digital sequence which is cross-correlated with the delayed version of the PRBS in the digital domain. The node *BIST out* in Figure 1 represents samples of the impulse response as digital signals.

III. Experimental Results

In order to evalaute the proposed defect based digital BIST, an LDO together with the proposed BIST circuit (Figure 1) are designed using the 65nm TSMC technology. We first compare the transfer function obtained through the BIST with the one obtained through spice simulation. The PRBS length in this design is 12 bits and PRBS frequency is 4MHz. The PRBS pattern is injected through the reference voltage node of the LDO and the impulse response is obtained via the digital cross correlation method as explained in the previous sections.

In Figure 2, the transfer function obtained from the proposed method is compared against the one obtained through Spice simulation. The BIST result is in very good agreement with AC analysis in Spice. In this figure, most important parameters are peaking magnitude and maximum peak frequency. These are relative measurements, meaning neither the magnitude of the PRBS nor the output affect these parameters. Thus, we can use these parameters as basis for comparison in order to detect defects. When the system is over-damped for some of the load conditions, peaking in the magnitude cannot be observed. In this case, we can define and use the cut-off frequency as a parameteric measurement to detect defects.

Corner responses of the defect free circuit is set to be conservative limits for fault detection. In Table I, we compare the results from the BIST method to corner simulations of SPICE circuit. We observe that even at process corners, the BIST results are in good agreement with Spice simulations. It should be noted that for defect detection, this need not be the condition as the BIST results from the corner would be taken as reference for pass/fail limit setting. However, this close agreement between the functional transfer function and the transfer function obtained from the BIST circuit builds confidence that the BIST method can indeed detect defects that alter the system transfer function.

Table I: Transfer function for process corners

	f_{cutoff} (KHz)	w_p (KHz)	M (dB)
Spice SS	244	365	2.3
Spice FF	187	216	1.45
BIST SS	251	345	1.71
BIST FF	192	198	1.07

Next, we insert structural faults into the LDO consisting of open and shorts for all transistors (including D-S short, D-G short, G-S short, D open, G open, and S open), as well as resistors and capacitors [3], [5]. For the shorts, a small resistor of 1 $1K\Omega$ and for the opens, $500K$ $10M\Omega$ resistors are utilized. There are total 102 faults. However, as expected, the majority of these faults are catastrophic, meaning they causes complete failure of the LDO operation, which is straightforward to detect by any means of testing. There are also hard-to-detect faults, which are defined as faults that shift the LDO operation marginally and do not cause a complete failure of the LDO functionality. We have identified 24 defects where LDO loop continues to work; for 12 of these faults, the DC value at the output does not change at all, which means that these faults cannot be detected by the DC measurement of the LDO output. On the other hand, the proposed BIST methodology can detect every one of the these inserted faults making the fault coverage %100 for the LDO with the given fault models.

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