A New High Step-Up DC-DC Topology with Zero DC Magnetizing Inductance Current and Continuous Input Current

Mohsen Mahmoudi
Department of Electrical Engineering
Azarbaijan Shahid Madani University
Tabriz, Iran
m.mahmoodi@azaruniv.ac.ir

Ali Ajami
Department of Electrical Engineering
Azarbaijan Shahid Madani University
Tabriz, Iran
ajami@azaruniv.ac.ir

Ebrahim Babaei
Department of Electrical Engineering
University of Tabriz
Tabriz, Iran
e-babaei@tabrizu.ac.ir

Nima Abdolmaleki
Department of Electrical Engineering
Wayne State University
Detroit, U.S.
nima.maleki@wayne.edu

Caisheng Wang
Department of Electrical Engineering
Wayne State University
Detroit, U.S.
cwang@wayne.edu

***Abstract*—A new high-voltage-gain non-isolated dc-dc topology for applications in renewable energies is proposed. A coupled inductor with three windings is used to increase the proposed topology voltage gain. In addition to increasing the voltage gain, the proposed topology also has other prominent features including continuous input current and zero dc magnetizing inductance current, which reduces the losses and size of coupled inductor core. Furthermore, the continuous input current guarantees a low-volume input filter, which is essential for renewable energy applications. The leakage inductor stored energy is recycled via the diode and capacitor and transferred to the converter output for increasing the efficiency and reducing voltage stresses on the converter components.**

Keywords—turns ratio, continuous input current, high voltage dc-dc converter, three-winding coupled inductor

I. INTRODUCTION

The increasing use of fossil fuels in recent decades has resulted in various problems for humankind including environmental pollutions and climate changes. Researchers have been making efforts to present strategies for decreasing the use of fossil fuels. The progress in field of power electronics has reduced the production costs associated with renewable energy resources such as solar cells and wind.

The maximum produced voltage for some of renewable energy resources, like individual solar cells is between 15-40 volts depending on varying factors like temperature and emitted radiation. An input dc link voltage of about 380 volts is required for the inverter to connect the solar cells to the grid or an ac load. Therefore, dc-dc converters with high step-up capability are necessary to increase the output voltage level of these renewable resources without having to put a large number of cells in series.

The conventional boost converter is the simplest topology for increasing the voltage level. This converter is only capable of delivering high voltage gain in theory. In practice, however, multiple factors limit its voltage gain, such as diode reverse recovery, switch and power diode losses, and equivalent series resistances of capacitors and inductors.

Another method for increasing the voltage gain is the use of coupled inductors on which vast research has been carried out [1, 2]. Using this approach, the leakage inductance stored energy can be recovered through a combination of coupled inductors and other elements [3-6]. However, use of coupled inductors alone cannot provide the high enough voltage gain necessary for grid integration and other applications. Through combined use of diodes and capacitors or inductors, we can reach some techniques to increase output voltage. These techniques include voltage multiplier, switched capacitor, and switched inductor methods.

Low input current ripple is very important for a dc-dc converters. However, the coupled inductor windings currents in coupled-inductor-based converters are discontinuous due to multiple operation modes in a switching period; Additionally, increasing turns ratio as a means for achieving higher voltage gains results further increases the primary winding current ripple. Generally, topologies in which the primary winding is in series with the input source have high input current ripple [5]. Another problem associated with dc-dc converters using coupled inductors is large dc magnetizing inductor current i_{Lm} that results in utilizing only half of the core B-H curve. Additionally, this high magnetizing current i_{Lm} increases the core losses [8].

Lately, researchers have proposed topologies based on three-winding coupled inductors for increasing the voltage gain of dc-dc converters. In [9], a high-voltage-gain converter is presented. However, the power switch and the output diode have high voltage stresses. The topology in [10] has discontinuous input current. Furthermore, the magnetizing inductance currents in [9,10] are not zero; and they suffer from disadvantages associated with common coupled-inductor-based converters mentioned above.

In this paper, a high-efficiency high-voltage-gain dc-dc topology with only one switch is introduced. The proposed topology is three-winding-coupled-inductor-based and has the below characteristics:

1) Input current continuity High voltage gain, 2) High voltage gain, 3) zero dc magnetizing inductance current, 4) the leakage inductor stored energy recovery, and 5) low switch voltage stress, which results in selection and use of lower-voltage-rated switch with smaller On resistance r_{ds} (on).

II. The Proposed Converter Operating Principles

Fig. 1 displays the proposed topology. This topology consists of a three-winding coupled inductor with turns numbers n_1, n_2, and n_3, one inductor, four capacitors C_1, C_2, C_3, C_4, three diodes D_1, D_2, D_3, and one power switch S.

For the coupled inductor, we have:

$$n_1 i_1 = n_3 i_3 + n_2 i_2 \Rightarrow i_1 = N_3 i_3 + N_2 i_2 \quad (1)$$

where

$$\frac{n_2}{n_1} = N_2 \quad , \quad \frac{n_3}{n_1} = N_3 \quad (2)$$

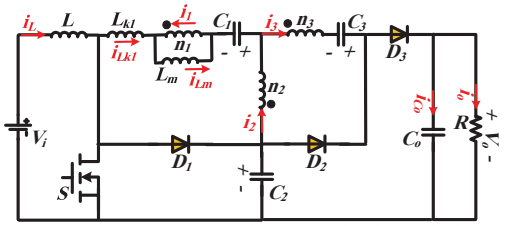


Fig. 1. Proposed three winding coupled-inductor dc-dc converter

For simplification of the suggest converter analysis, the parasite components of elements, namely the parasite resistances of the inductors, capacitors, and the switch, and the threshold voltage of diodes and the switch are ignored, except for the leakage inductance. Moreover, the values of capacitors are assumed to be high.

According to the voltage balance law in steady state, the average voltage over the inductor in one period is zero. Applying this rule to magnetizing inductor L_m gives:

$$\frac{(V_{C1}-V_{C2})}{1-N_2} D + \frac{V_{C1}}{1-N_2}(1-D) = 0 \Rightarrow V_{C1} = DV_{C2} \quad (3)$$

Also, applying the voltage balance law on the input inductor yields (4):

$$V_i D + (V_i - V_{C2})(1-D) = 0 \Rightarrow V_{C2} = \frac{V_i}{1-D} \quad (4)$$

Thus, the voltage of capacitor C_1 is given as (5) by replacing (4) in (3):

$$V_{C1} = \frac{D}{1-D} V_i \quad (5)$$

The analysis of the presented converter gives the voltage of capacitor C_3 and the voltage gain for the proposed converter as (6) and (7), respectively.

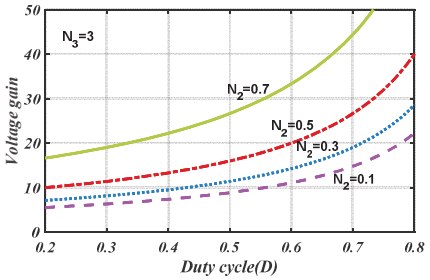


Fig. 2. Voltage gain of proposed converter at CCM operation

$$V_{C3} = \frac{(N_2+N_3)D}{(1-N_2)(1-D)} V_i \quad (6)$$

$$\frac{V_o}{V_i} = \frac{N_3+1}{(1-N_2)(1-D)} \quad (7)$$

Fig. 2 shows the proposed topology voltage gain versus the duty cycle. Assuming $N_3 = 3$, the closer the turns ratio of N_2 to 1, the higher the voltage gains that can be reached.

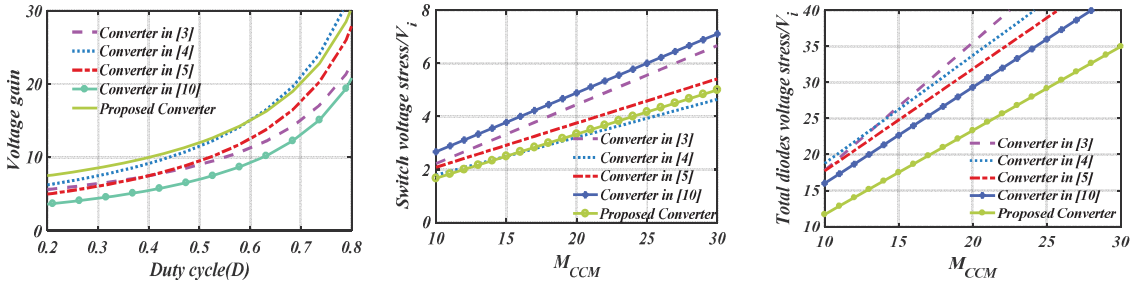
III. Performance Comparison

A comparison is conducted in this section to evaluate the proposed converter. All compared converters are coupled-inductor-based and have one power switch. The converters presented in [3-5] possess two-winding coupled inductors, and the converter proposed in [10] has a coupled inductor with three windings. The comparison criteria are switch voltage stress, total diodes voltage stress, and the voltage gain.

The turn ratios N_2, N_3, and N, are respectively assumed to be 0.5, 2, and 2.5. The turns ratio N has been used for the two-winding converters in [3-5].

The proposed converter can reach its maximum voltage gain in duty cycles less than 0.6. In duty cycles higher than 0.6, the proposed topology voltage gain is slightly lower than [4] as displayed in Fig. 3(a). Of course, the converter introduced in [4] has one more diode than the proposed converter and its input current is discontinuous. In accordance with Fig. 3(b), the proposed topology and the topology provided in [4] have the lowest switch voltage stresses. Therefore, they allow for selecting a switch with lower ratings.

The total diodes voltage stresses for the selected converters are displayed in Fig. 3(c). The suggested topology has the smallest value in this criterion as well.



(a) Voltage gain various duty cycles

(b) Switch voltage stress various voltage gains

(c) Total diodes voltage stress various voltage gain

Fig. 3. The proposed dc-dc topology comparison with [3-5,10]

The average magnetizing inductor current is only equal to zero in the proposed topology and the converter [3] amongst the compared topologies. This leads to the storage of no energy in the coupled inductor cores of these converters, which in turn results in increased converter efficiency.

IV. Efficiency Calculation

The parasitic elements in the efficiency calculation of the proposed converter including r_s, r_D, r_n, r_L and r_c are on-state resistance of power switch, diode, ESR of transformer's winding, inductor and capacitor, respectively.

The amount of diodes average current is equal to the output current. Therefore, total conduction power losses of the diodes we have:

$$P_{VF} = 3V_F I_o \tag{8}$$

The effective currents of diodes will be obtained as bellow:

$$i_{D1_{rms}} = I_L\sqrt{\frac{D_1}{3}} \tag{9}$$

$$i_{D2_{rms}} = I_{D2p}\sqrt{D' - \frac{2}{3}D_1} \tag{10}$$

$$i_{D3_{rms}} = I_{D3p}\sqrt{\frac{D}{3}} \tag{11}$$

Where

$$I_{D2_p} = \frac{I_o}{D'-0.5D_1} \tag{12}$$

$$I_{D3_p} = \frac{2I_o}{D} \tag{13}$$

The current of diode D_1 has the same average value as the output current I_o, and its peak value is equal to I_L, so variable D_1 can be calculated as

$$D_1 = \frac{2I_o}{I_L} \tag{14}$$

Also, the effective currents of windings and switch can be calculated as follows:

$$i_{n1_{rms}} = i_{Lk_{rms}} = \sqrt{\frac{(N_2+N_3)^2}{(1-N_2)^2}I_{D3p}^2\left(\frac{D}{3}\right) + I_L^2\left(D' - \frac{2}{3}D_1\right)} \tag{15}$$

$$i_{n2_{rms}} = \sqrt{\frac{(1+N_3)^2}{(1-N_2)^2}I_{D3p}^2\left(\frac{D}{3}\right) + \left(I_{D2p} - I_L\right)^2\left(D' - \frac{2}{3}D_1\right)} \tag{16}$$

$$i_{n3_{rms}} = \sqrt{I_{D3p}^2\left(\frac{D}{3}\right) + I_{D2p}^2\left(D' - \frac{2}{3}D_1\right)} \tag{17}$$

$$i_{S_{rms}} = \sqrt{\left(I_L\left(I_L + \frac{N_2+N_3}{1-N_2}I_{D3p}\right) + \frac{(N_2+N_3)^2 I_{D3p}^2}{3(1-N_2)^2}\right)D} \tag{18}$$

The current of capacitors C_1 and C_3 are equal to the current of windings n_1 and n_3, respectively. Consequently, their effective values are also the same. The effective values of the current of capacitors C_2 and C_o, can be written as:

$$i_{C2_{rms}} = \sqrt{\frac{(1+N_3)^2}{(1-N_2)^2}I_{D3p}^2\left(\frac{D}{3}\right) + I_L^2 D'} \tag{19}$$

$$i_{Co_{rms}} = \sqrt{I_o^2 + \left(\frac{1}{3}I_{D3p}^2 - I_o I_{D3p}\right)D} \tag{20}$$

Switching losses can be calculated as:

$$P_{Sw} = V_S^2 C_{out} f_s \tag{21}$$

Where V_s is the switch voltage, C_{out} is the switch output capacitance, and f_s is switching frequency.

According to the given formulation for effective current values of the switch, windings, inductor, diodes, and capacitors, the ohmic power dissipated can be calculated through multiplying the square of the effective current of each element by its resistance. Finally, the proposed converter total loss is yielded as:

$$P_{loss_t} = \sum_{x=1}^{3} P_{rn_x} + \sum_{x=1}^{3} P_{rC_x} + \sum_{x=1}^{3} P_{rD_x} + 3P_{VF} + P_{rS} + P_{sw} + P_{rL} \tag{22}$$

Where, $P_{rn_{1,2,3}}, P_{rC_{1,2,3}}, P_{rD_{1,2,3}}, P_{rS}, P_{rL}$ are the ohmic losses of windings n_1, n_2, n_3, capacitors C_1, C_2, C_3, diodes D_1, D_2, D_3, the power switch, and the inductor, respectively.

Therefore, the proposed converter efficiency will be calculated according to equation (23).

$$\eta = \frac{P_o}{P_o + P_{loss_t}} \tag{23}$$

V. Simulation Results

The simulation data for operation verification of the presented converter is presented in this section. The proposed converter specifications are given in Table I.

Table I. Specification of the experiment

Specifications	Values
Input/ output DC voltage (V_i/V_o)	30/300V
Output Power (P_o)	200W
Switching frequency (f_s)	50kHz
Input inductor	n_1=16 L: 330 µH Ferrite core EE40
Coupled inductor	L_m: 300 µH n_1:n_2:n_3=12:6:24, Ferrite core EE40
Capacitors C_1, C_2, C_3, C_o	100, 100, 47, 100 µF 100, 100, 200, 400 V
Diodes (D_1, D_2, D_3)	U1560
Power Switch (MOSFET)	IRFP260

The input inductor current, voltage, and power switch current are shown in Fig. 4-a. The switch maximum voltage stress is 54V. The power switch voltage is equal to the capacitor C_2 voltage and can be calculated as:

$$V_S = \frac{V_i}{1-D} = \frac{30}{1-0.4} = 50V \tag{24}$$

The diodes currents are given in Fig. 4-b. By calculating the voltage of the capacitor C1-C3 using (4)-(6), the capacitor voltages equal 20, 50 and 100 volts, respectively. Figure 4-c shows the values of capacitor voltages are respectively about 25, 55 and 92 volts. The output voltage of converter which equals voltage of capacitor C_o is also shown to equal 275.

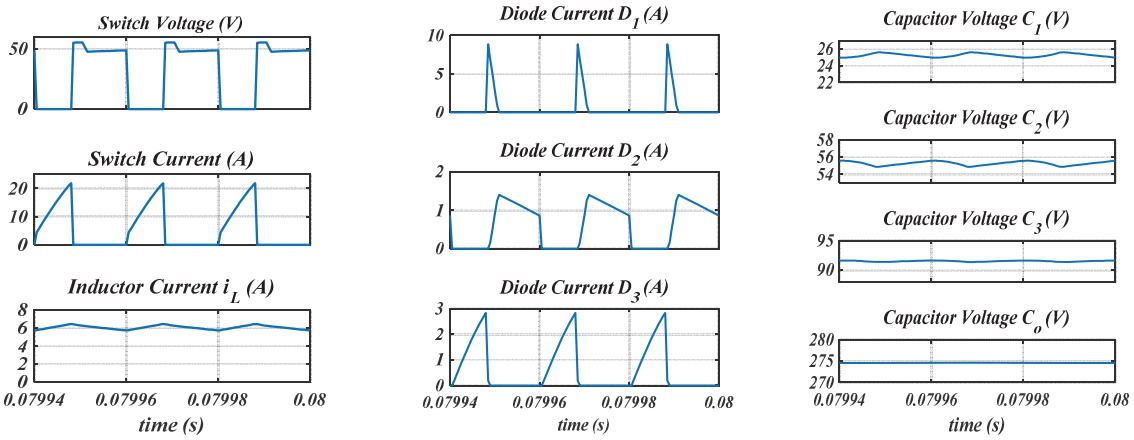


Fig. 4. The proposed topology simulation data

VI. Experimental Results

A 200W prototype was developed for further verification of theoretical calculation and simulation results, as shown in Fig. 5. The prototype specifications are the same as table I. Fig. 6 shows the measured gate voltage, input current, and input voltage. Fig. 7 displays the measured Capacitors C_1-C_3 voltages along with capacitor C_o voltage, which equals the output voltage. It can be observed that experimental results prove the theoretical calculations and simulations results and verify the presented topology operation.

Fig. 5. The implemented prototype

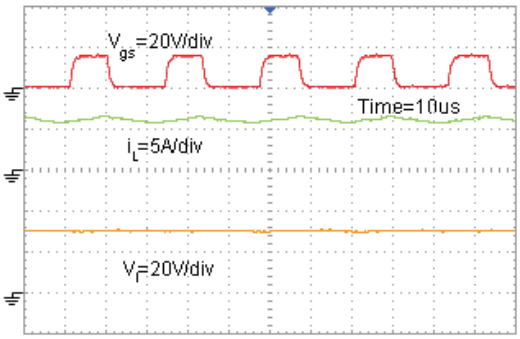


Fig. 6. Power switch Gate-Source voltage, converter input current, and input voltage

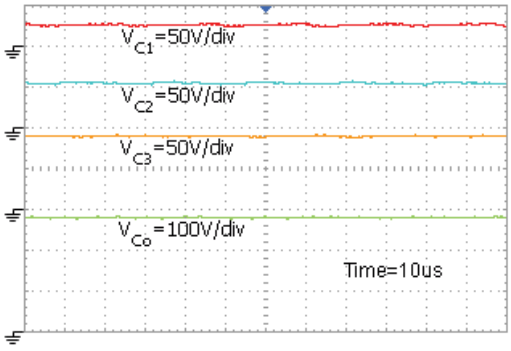


Fig. 7. Capacitors voltages

VII. Conclusion

A three-winding-coupled-inductor-based dc-dc converter has been presented in this article. A high voltage gain can be achieved by selecting appropriate turns ratios of the coupled inductor. The best range for the second winding turns ratio (N_2) has been obtained between 0.5 and 0.7 for obtaining high voltage gain and keeping the voltage drop across the parasitic elements of the converter at a reasonable level. An increase in the voltage gain has been achieved with fewer elements compared to the predecessors. The simulation and experimental implementation have been carried out and the corresponding results have verified the theoretical calculations. Some of the most significant advantages of the proposed topology are zero average magnetizing inductor current and the continuity of the input current, which decreases the size of output filter.

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