A High Gain DC-DC Topology Based on Two-Winding Coupled Inductors Featuring Continuous Input Current

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***Abstract*— A high-voltage-gain dc-dc converter topology is proposed for renewable energy applications. The proposed coupled-inductor-based high-gain dc-dc converter features reduced input current ripple. The semiconductor elements voltage spikes due to the leakage inductance are prevented through the use of a clamping circuit. The Clamping circuit helps recover the leakage inductance stored energy, which causes voltage spikes on the switch. This results in the selection of elements with lower voltage ratings. Power switches with lower voltage ratings lead to lower conduction losses and improved system efficiency. The DC component of the inductor magnetizing current is zero. Consequently, no energy is stored in the inductor core, and the losses are further reduced.**

***Keywords*— low input current ripple, high-gain dc-dc converter, coupled inductor**

The increase in energy demand and environmental pollution caused by fossil fuels has created a rapidly increasing interest in green energy sources, namely solar cells, wind, fuel cells with fuel generated from renewable sources, etc. Many renewable energy sources have low voltage levels and require high-voltage-gain converters to become consumable. Other applications of high-voltage-gain dc-dc converters include but are not limited to uninterruptable power supply (UPS) and power factor correction (PFC). Significant research has been conducted on dc-dc boost converters for a variety of applications having low input voltage. In these converters, in addition to the increase in voltage gain, the converter performance has been improved through the reduction of converter losses, voltage and current stresses of elements, weight, and volume.

Unfortunately, the voltage gain of a conventional non-isolated boost converter is limited by the parasitic elements present in the circuit. Isolated converters such as forward converter, flyback converter, half-bridge converter, and full-bridge converter have been proposed as solutions to this problem in order to achieve higher voltages. The voltage gain in the isolated converters has a direct relationship with their transformers turns ratios. However, the leakage inductance increases with the increases in the turns ratio as well. Therefore, increasing the turns ratio for achieving higher voltage gains would result in an increase of leakage inductance, which can, in turn, increase the voltage spikes over the power switches.

The use of coupled inductors is another method for implementing high step-up boost converters, which has attracted extensive research . In coupled-inductor-based converters, higher voltages can be achieved through increasing the turns ratio and some other boosting techniques, such as voltage multiplier, voltage lift, voltage doubling, switched capacitor, switched inductor, and the combination of switched capacitor and switched inductor [1-8]. The energy stored in the leakage inductance in the aforementioned converters can be restored using a clamping circuit. This circuit, in combination with other methods, namely, the switched inductor, voltage lift, voltage multiplier, etc., can help improve the voltage gain and efficiency of the converters [9-13].

However, there are some problems associated with the use of coupled inductors. Low input current ripple is considered an advantage for high-gain converters and beneficial to certain input power sources such as fuel cells [14,15]. However, the input current ripple in coupled-inductor-based converters is high. Furthermore, converters with high input current ripple normally require large input capacitances. Another problem of coupled-inductor-based converters proposed in the literature is the existence of a large dc magnetizing inductor current (i_{Lm}) in the coupled inductor, due to which only half of the core B-H curve loop is used. Consequently, the core utilization is lowe in coupled-inductor-based converters [16]. Additionally, the current i_{Lm} increases the core losses [17].

This paper presents a new non-isolated high-voltage-gain converter with zero dc magnetizing inductor current and no requirement for the use of high duty cycles. The proposed high-gain topology features lowered switch voltage stress, increased voltage gain, continuous front-end current, no coupled inductor energy storage, no need for high winding turns number, low leakage inductance that reduces the turns number, and recovery of the leakage inductor stored energy.

I. The Proposed Topology Analysis

Fig. 1 shows the presented topology. The circuit includes an inductor L, a coupled inductor with turns numbers of n_1, n_2, and the total leakage inductance L_{k1}, three diodes D_1, D_2, D_3, four capacitors C_1, C_2, C_3, C_o, and one power switch S.

The following simplifying assumptions are made in the steady-state operation analysis:

- The semiconductor elements are ideal.
- All parasitic elements except for the leakage inductance are ignored.
- The capacitors are assumed to be large and, therefore, regarded as voltage sources.

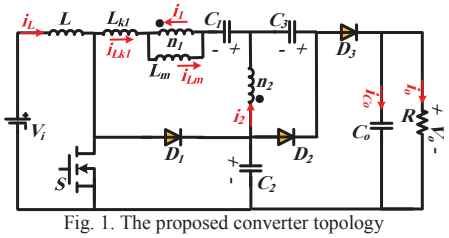


Fig. 1. The proposed converter topology

A. Steady State Analysis and Operating Principles

In this subsection, the principles of operation of the presented dc-dc converter are analyzed in steady state while the topology is in the continuous conduction mode (CCM).

The current paths in the presented topology and the CCM waveforms for all operation stages are displayed in Figs. 2 and 3, respectively. The proposed converter has 5 stages in each switching period. In all switching states, capacitors C_1, C_3 and the second winding are connected to each other. Since the average capacitor currents are zero in a switching period, the average of the second and primary winding currents are zero. Also, since no energy is stored in the magnetizing inductor, its average current is zero, and the primary and secondary windings are similar. It is noteworthy that the amplitudes of the coupled inductor winding currents are not the same, and only their shapes are the same. Stages I and III can be ignored due to their small time frames. Also, the voltage drop on the leakage inductance is ignored due to its small value. The analysis of the rest of the stages is as follows.

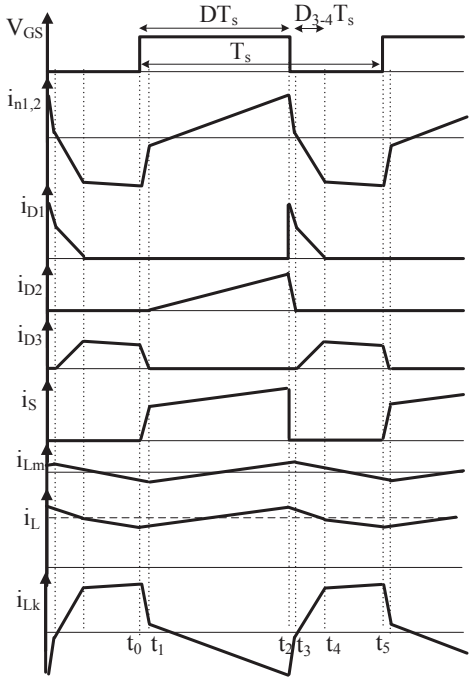


Fig. 3. Typical waveforms of the presented topology in CCM Operation

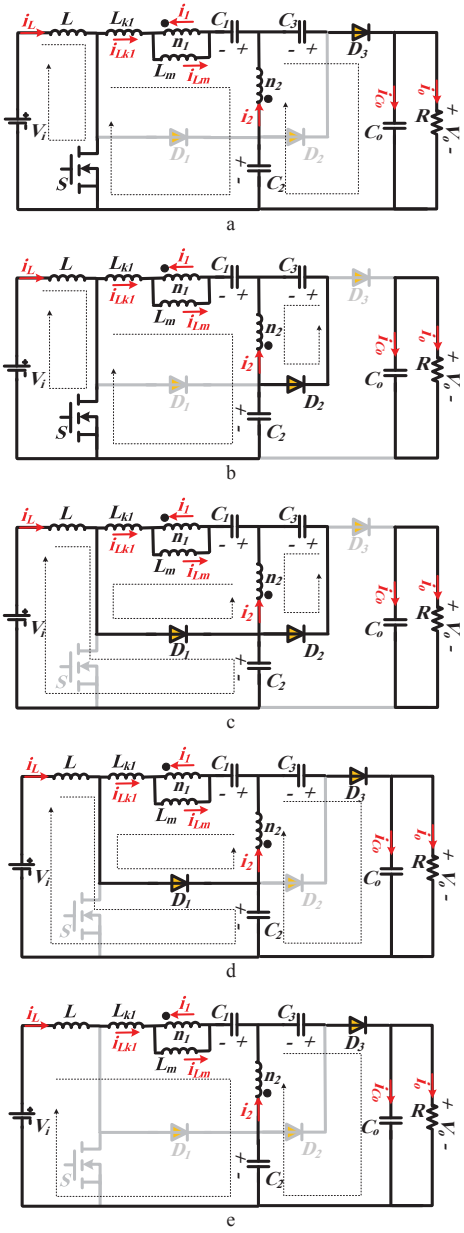


Fig. 2. Current flow paths for different CCM operation stages of the presented topology

Stage II ($t_1 < t < t_2$): In this stage, shown in Fig. 2b, the switch S and the diode D_2 are on, while the diodes D_1 and D_3 are off. The input source charges the front-end inductor L, and capacitors C_1 and C_3 get charged by capacitor C_2. Therefore, the magnetizing inductance is being charged to i_{Lm} in its positive direction specified in Fig. 2b. During this stage and until the switch turn-off, which marks the end of this stage, supplying the load is handled by the outer capacitor. It is worth noting that the outer capacitor C_o supplies the load during this stage.

Writing the KVL in Fig. 2b yields

$$V_L = V_i \tag{1}$$

$$V_{Lm} = \frac{V_{C1} - V_{C2}}{1 - N} \tag{2}$$

$$V_{C3} = \frac{N}{1-N}(V_{C1} - V_{C2}) \quad (3)$$

where N is the secondary to primary windings turns ratio.

Stage IV $[t_3 < t < t_4]$: The current paths for this stage are displayed in Fig. 2d. The switch S and the diode D_2 are off in this interval while the diodes D_1 and D_3 are on. The front-end inductor L and the capacitors C_1 and C_3 get discharged, while C_2 and C_o are charged. This interval continues until the diode D_1 turns off. Writing the KVL for Fig. 2d in the steady state gives

$$V_L = V_i - V_{C2} \quad (4)$$

$$V_{Lm} = \frac{V_{C1}}{1-N} \quad (5)$$

Stage V $[t_4 < t < t_5]$: During this interval, illustrated in Fig. 2e, all semiconductor devices are off except for the diode D_3. This stage continues until the switch turns on and a new operation cycle begins. Writing the KVL in Fig. 2e gives the output voltage as

$$V_o = V_{C3} - \frac{N}{1-N}V_{C1} + V_{C2} \quad (6)$$

The volt-second balance holds true for the magnetizing inductor. This gives the relation between voltages of capacitors C_1 and C_2.

$$\frac{V_{C1} - V_{C2}}{1-N}D + \frac{V_{C1}}{1-N}(1-D) = 0 \Rightarrow V_{C1} = DV_{C2} \quad (7)$$

Applying the same principle on the front-end inductor results in

$$V_i D + (V_i - V_{C2})(1-D) = 0 \Rightarrow V_{C2} = \frac{V_i}{1-D} \quad (8)$$

The voltage of capacitor C_1 is obtained by substituting (8) in (7) as

$$V_{C1} = D\left(\frac{V_i}{1-D}\right) \quad (9)$$

The substitution of (8) and (9) in (3) derives the voltage of capacitor C_3 as (10).

$$V_{C3} = \frac{N}{N-1}(V_i + (1-D)) \quad (10)$$

Next, the output voltage V_o can be calculated using (8), (9), (10), and (3) as

$$V_o = \frac{2N-1}{(N-1)(1-D)}V_i \quad (11)$$

Finally, the CCM operation voltage gain (M_{CCM}), considering the ideal coupled inductor ($V_{Lk2,4}$=0), is obtained.

$$M_{CCM} = \frac{V_o}{V_i} = \frac{2N-1}{(N-1)(1-D)} \quad (12)$$

Fig. 4 displays the voltage gain relation (12) for different duty cycles and windings turns ratios N. It can be seen that turns ratios closer to 1 correspond to higher voltage gains.

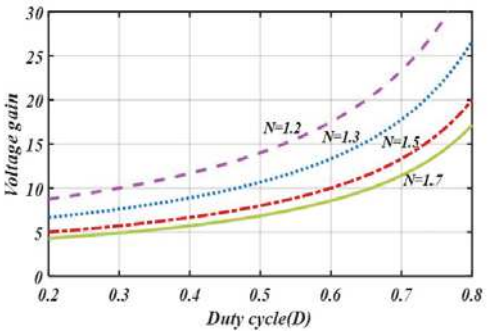


Fig. 4. The voltage gain of the presented converter versus duty cycle under different turns ratios.

B. Losses and Efficiency Analysis

The losses and efficiency calculations of the presented topology are provided in this subsection. The parasitic elements that need to be considered in the loss analysis are on-resistances of the switch and diodes, total ESR of the coupled inductor, and ESRs of the inductor and capacitor, which are commonly represented by r_S, r_D, r_n, r_L, and r_c, respectively. These parasitic resistances are used for conduction losses calculation.

According to subsection II.A., the RMS currents of diodes, windings, switch, and the capacitors can be calculated as (13)-(20).

$$i_{D1rms} = I_L\sqrt{\frac{D_{3-4}}{3}} \quad (13)$$

$$i_{D2rms} = I_{D2p}\sqrt{\frac{D}{3}} \quad (14)$$

$$i_{D3rms} = I_{D3p}\sqrt{D' - \frac{2}{3}D_{3-4}} \quad (15)$$

$$i_{n1rms} = i_{Lkrms} = \frac{N}{N-1}\sqrt{I_{D2p}^2\left(\frac{D}{3}\right) + I_L^2\left(D' - \frac{2}{3}D_{3-4}\right)} \quad (16)$$

$$i_{n2rms} = \frac{i_{n1rms}}{N} \quad (17)$$

$$i_{Srms} = \sqrt{\left(I_L(I_L + \frac{N}{N-1}I_{D2p}) + \frac{(I_{D2p}N)^2}{3(N-1)^2}\right)D} \quad (18)$$

Where D and $D_{3\text{-}4}$ are time-frame-to-operation-periods as shown in Fig. 3, and $D'=1-D$. The current of the capacitor C_1 is equal to the secondary winding current. Consequently, they have equal RMS values. The RMS values for the capacitors C_2 and C_3 would be obtained as

$$i_{C2rms} = \sqrt{\frac{N^2}{(N-1)^2}I_{D2p}^2\left(\frac{D}{3}\right) + I_L^2 D_{3-4} + (I_L - I_{D3p})^2 D'} \quad (19)$$

$$i_{C3rms} = \sqrt{I_{D2p}^2\left(\frac{D}{3}\right) + I_{D3p}^2\left(D' - \frac{2}{3}D_{3-4}\right)} \quad (20)$$

The diodes have the same average values as the output current. As a result, each diode conduction losses is given as

$$P_{cD} = V_F I_o \tag{21}$$

The conduction losses associated with the coupled inductor, inductor, power switch, and the capacitors can be obtained according to (13)-(21) through the multiplication of their RMS values and their corresponding parasitic resistances.

The switching losses play an important role in the efficiency of the DC-DC converters, which are controlled by hard-switched methods. Diodes switching losses are negligible and often ignored. Representing the switch blocking voltage, output parasitic capacitance of the power switch, and switching frequency by V_s, C_{oss}, and f_s yields the converter switching losses as

$$P_{Sw} = V_S^2 C_{oss} f_s \tag{22}$$

Using (13)-(22), the total converter losses can be calculated.

$$P_{loss_t} = P_{rn1} + P_{rn2} + P_{rC1} + P_{rC2} + P_{rC3} + P_{rD1} + P_{rD2} + P_{rD3} + 3P_{cD} + P_{rS} + P_{sw} + P_{rL} \tag{23}$$

Where P_{rnx} , P_{rCx} , P_{rDx} respectively represent the ohmic losses corresponding with the coupled inductor windings, capacitors, diodes, and finally, P_{rS} and P_{rL} represent the switch and inductor ohmic losses.

Using (23) and the output power, the converter efficiency is yielded as

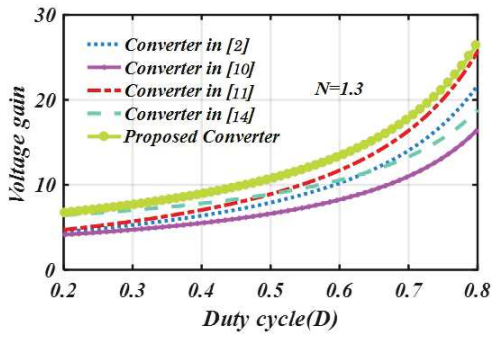
$$\eta = \frac{P_o}{P_o + P_{loss_t}} \tag{24}$$

II. Performance Comparison

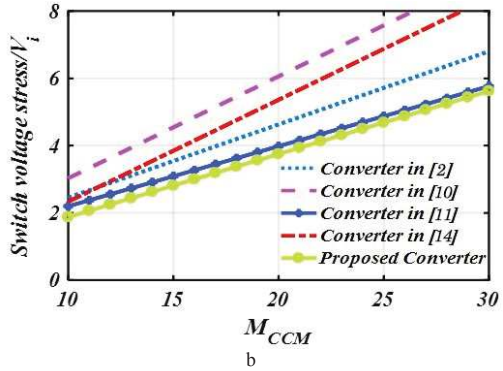
In this section, a comparison study is conducted to prove the superiority of the presented topology versus its recent two-winding predecessors. The voltage gain and voltage stresses of the switch and the diodes are selected as the comparison criteria. The results are shown in Fig. 5. The results reveal that the presented converter provides higher voltage gains for the same duty cycle compared to other converters. Additionally, Fig. 5b demonstrates that the proposed converter has the lowest switch voltage stress compared to its peers. While the presented topology has a lower diode voltage stress than that in [14], its total diode voltage stress is higher than the topologies in [2], [10], and [11]. The presented converter is compared to peers that are based on two-winding coupled inductors.

III. Simulation Results

In this section, the presented high-voltage-gain dc-dc topology is simulated at 200 W to verify the operation and presented analysis. Input and output voltages of 30 and 300 volts are selected, respectively. The switching frequency is 50 kHz, and the coupled inductor turns ratio N is chosen as 1.5. The values of capacitors C_1, C_2, C_3, C_o and inductors L, L_m are selected as 100 µF, 100 µF, 47 µF, 100 µF, 330 µH, and 300 µH, respectively. Figs. 6-9 show the simulation results.



a



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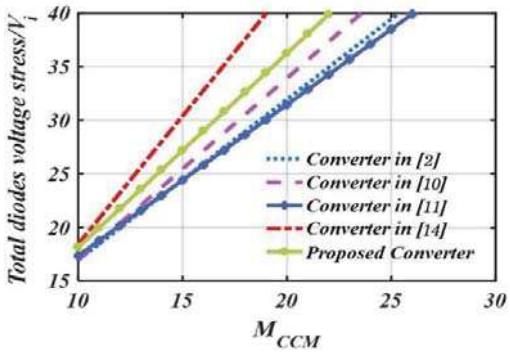

c

Fig. 5. Comparison of the presented topology with peers

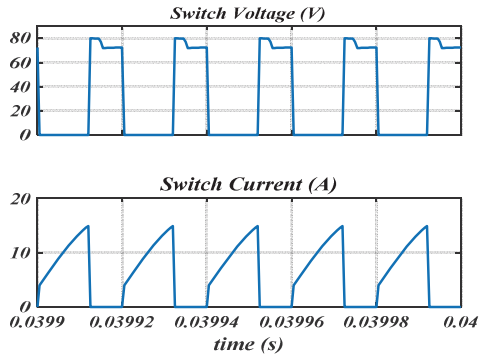

Fig. 6. Power switch characteristic profiles

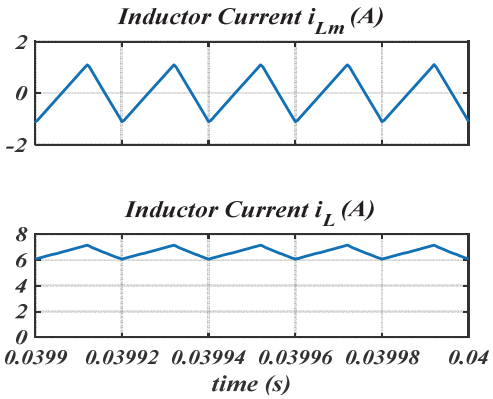

Fig. 7. Magnetizing and input inductor currents.

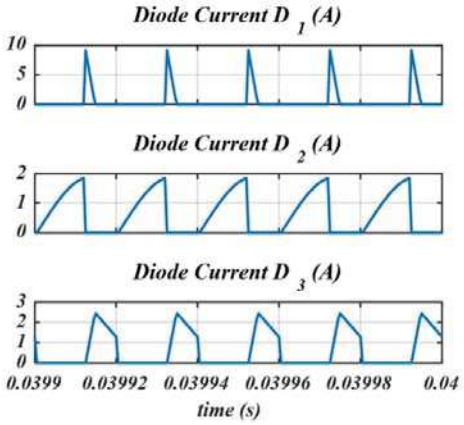

Fig. 8. Diode currents

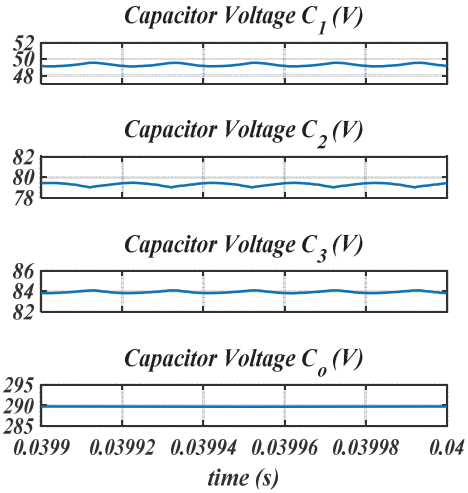

Fig. 9. Capacitor voltages.

IV. Experimental Results

A 200W prototype is developed for further verification of the presented converter, as shown in Fig. 10.

The input and output voltages of 30 and 300 volts are selected, respectively. The switching frequency is 50 kHz, and the coupled inductor turns ratio N is 1.5. The values of capacitors C_1, C_2, C_3, C_o and inductors L, L_m are

Fig. 10. The developed experimental prototype

selected as 100 µF, 100 µF, 47 µF, 100 µF, 330 µH, and 300 µH, respectively. Fig. 11 shows the switch voltage and the front-end inductor current. The switch voltage stress during the leakage inductance discharge is about 85 V and afterwards decreases to 73 V. Since the load current is 0.66 A and the voltage gain has been set to 10, the input inductor average current value is approximately 6.6 A. Capacitors voltages are displayed in Figs. 12 and 13. Finally, Fig. 14. shows the converter diodes voltages. The theoretical values of the capacitor voltages are 45 V, 75 V, and 90 V, respectively. These theoretical values are confirmed by the results in Figs. 9, 11, and 12.

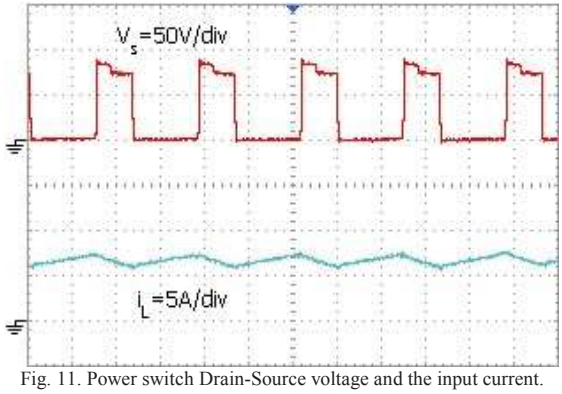

Fig. 11. Power switch Drain-Source voltage and the input current.

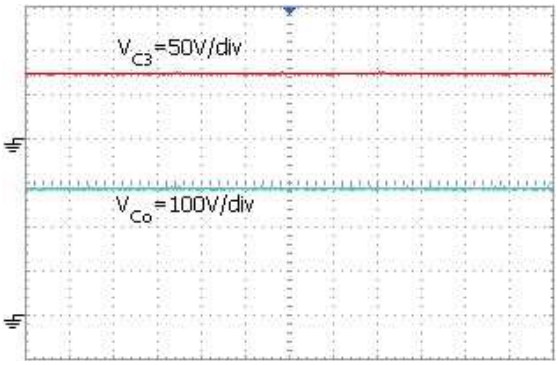

Fig. 12. Capacitor C_3 voltage and capacitor C_o voltage that equals the output voltage.

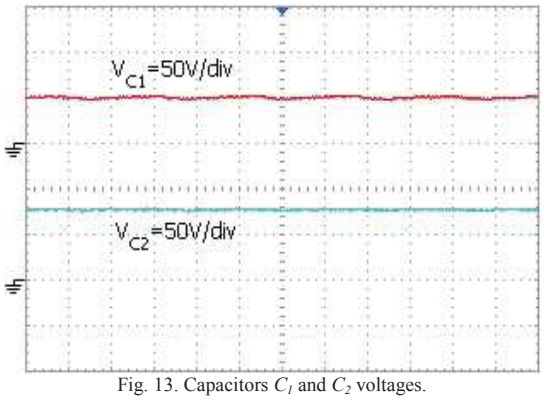

Fig. 13. Capacitors C_1 and C_2 voltages.

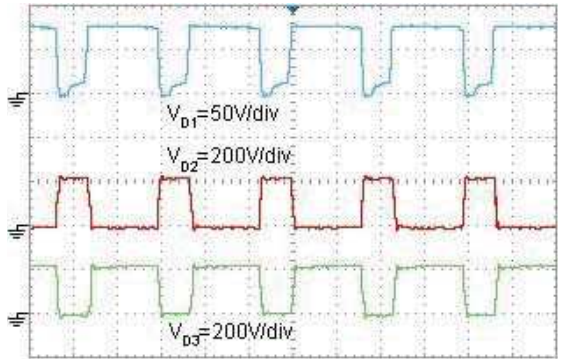

Fig. 14. Diodes voltages.

V. Conclusion

A non-isolated high-efficiency high-voltage-gain dc-dc converter was proposed in this paper. Adopting switched capacitor technique and high voltage gain, the presented topology has been proved to be capable of operating at high voltage gains without high windings turns ratios. A reduction in leakage inductance has been achieved by decreasing the number of windings turns. The switch voltage stress is decreased and, consequently, a lower-rated switch can be selected, and the converter cost and conductive losses are reduced. The very low input current ripple in the proposed converter has made it appropriate for green energy applications such as fuel cells and solar cells.

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