**Superior Growth, Yield, Repeatability, and Switching Performance in GaN-based Resonant Tunneling Diodes**

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We report the direct measurement of record fast switching speeds in GaN/AlN resonant tunneling diodes (RTDs). The devices, grown by plasma-assisted molecular-beam epitaxy (MBE), displayed three repeatable negative differential resistance (NDR) regions below a bias of +6 V. A room temperature peak-to-valley current ratio (PVCR) > 2 was observed, which represents a marked improvement over recent reports. Measurements carried out on hundreds of devices, of varying size, revealed a yield of ~90%. Repeatability measurements consisting of 3,000 sweeps resulted in a standard deviation, relative to the mean, of < 0.1%. Temperature dependent measurements combined with non-equilibrium Green's function (NEGF) based quantum transport simulations suggest the presence of both 3-dimensional (3-D) and 2-dimensional (2-D) emitters, giving rise to three NDR regions. Finally, a valley current density vs perimeter-to-area-ratio study indicates the presence of a surface leakage current mechanism which is reducing the PVCR.

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The demand for devices which can reliably operate at high power in the millimeter-wave (mm-wave) and terahertz (THz) spectrums continues to grow as applications in security, medicine, imaging, spectroscopy, and ultra-high speed wireless networks are realized. Unfortunately, for THz applications, compact, solid state devices remain a challenge to produce. Two possible candidates which are being considered are quantum cascade lasers (QCLs, multiple barriers) and resonant tunneling diodes (RTDs, double barrier), both of which are vertical, unipolar heterostructure devices that rely on ultra-fast electron transport via quantum mechanical tunneling. In 2012, a GaAs/AlGaAs QCL, which operated at an impressive 3.22 THz with 38 mW of peak power, was reported by Fathololoumi et al. [1] However, because of the low LO-phonon energy of GaAs (36 meV), these large area devices had to be operated under pulsed conditions and kept at temperatures below ~200 K, otherwise the thermal energy would be large enough to allow for non-radiative effects to degrade the population inversion. RTDs based in InAs/AlSb and InGaAs/AlAs have reached fundamental oscillations of 712 GHz [2] and 1.92 THz [3], respectively, at room temperature, but lack the significant output power required for many applications. Very recently, however, a group in Glasgow has reported 1 mW of output power at 260 GHz with InGaAs-based RTDs using on-chip biasing and power combining techniques. [4] One possible approach to improve upon the already reported QCLs and RTDs would involve switching to wider bandgap III-nitride based structures. The wide band gap of GaN-based devices has the potential to provide higher operating temperatures for QCLs and greater power output from high frequency RTDs.

The results from initial reports of GaN-based RTDs [5-8] were called into question by Belyaev *et al.* in 2003 [9]. Following this there were many other reports of NDR in a GaN-based RTD – all of which lacked room temperature hysteresis-free repeatable NDR. [10-17] It wasn't until recently that reports of GaN-based RTDs began displaying true negative differential resistance

(NDR) repeatability. [18-27] This was quickly followed up with increased peak current densities [20-25], as well as demonstrated microwave oscillations [21], light emission in a unipolar device [20,22], and the ability to successfully grow device structures on GaN-templated sapphire substrates [23,24], which have higher dislocation densities, but are more readily available and significantly less expensive. Despite reports of current densities from 100 kA/cm$^2$ to nearly 1 MA/cm$^2$ [20,21,23-25], the current available for switching applications, $\Delta I$ (peak current - valley current), is still rather low, as evidenced by the modest peak-to-valley current ratios (PVCRs) shown in these publications. To date, the largest reported room temperature, repeatable, PVCR for a GaN-based RTD is 1.6 [20]. While the PVCR does not directly translate to $\Delta I$, it is an indicator for the potential to generate greater $\Delta I$ as device area scales up, and provides an overall measure of device quality. As a result, PVCR is an important metric in RTD-based oscillators and switches for predicting the potential for high output power and fast switching speed.

In this letter, we report experimental measurements and theoretical analyses examining the various current mechanisms which may be limiting GaN/AlN RTDs. Statistical analysis of the dependence of the current density on device area and perimeter was enabled by the high yield and uniformity of working RTDs. We present simulation data based on a non-equilibrium Green's function (NEGF) formalism which, when combined with low temperature measurements, elucidates the mechanisms leading to the presence of three distinct NDR regions in individual devices. Furthermore, we use a previously developed method [26,27] to directly measure the switching speed of our GaN/AlN RTDs. These findings serve as a springboard for developing the compact, room-temperature GaN-based QCLs, and higher-power RTD oscillators necessary for mm-wave and THz applications.

The RTD structure, illustrated schematically in Figure 1(a) (inset), was grown by plasma-assisted MBE on a freestanding GaN substrate. An 18 × 18 $mm^2$ square GaN substrate was diced from a commercially-obtained 50-mm diameter, semi-insulating, Ga-polar GaN wafer. The Ga-polar (0001) surface of the substrate wafer was nominally on-axis with a maximum offcut of 0.5°. The wafer surface was finished on both sides with a chemical-mechanical polish. The density of threading dislocations was estimated to be $<5 \times 10^6$ $cm^{-2}$, and the root-mean-square (RMS) roughness of the as-grown sample surface was measured by atomic force microscopy to be 6 Å over a 20×20 $\mu m^2$ area. Immediately prior to loading into the ultra-high vacuum (UHV) MBE system, the GaN substrate was prepared using an aggressive, *ex situ* wet chemical clean, described in detail previously. [28,29] The substrate was then degassed in UHV for 30 minutes at 600 °C and transferred to the deposition chamber for growth.

Deposition of the epitaxial layers was performed in an Omicron/Scienta PRO-75 MBE chamber equipped with a Veeco Uni-Bulb™ plasma source to supply an active nitrogen (N*) flux, dual-filament effusion cells to supply elemental Ga and Al fluxes, and a single-filament effusion cell to supply Si dopants. The nitrogen plasma source was operated at 275 W and 0.80 sccm, resulting in a N*-limited growth rate of 3 nm/min. The Ga/N* flux ratio was held constant during the growth and was estimated to be ~1.3, while the Al/N* flux ratio was very nearly unity.

Growth was initiated by first exposing the GaN substrate surface to the N* plasma for two minutes, after which the Ga and Si source shutters were opened for growth of the $5\times10^{19}$ $cm^{-3}$ n-type GaN:Si emitter bottom contact layer. The structure was grown continuously and without interrupts. The growth temperature, which was monitored by a thermocouple mounted behind the wafer, was maintained at 810 °C from the initiation of growth until the completion of the active region [defined with the red box in Figure 1(a) inset], after which it was ramped to 900 °C for the

remainder of the growth. By comparison, the active region growth temperature in previous reports of nearly identical structures was ~50 °C hotter. [20,24] Inspection of the as-grown surface by optical microscopy revealed the absence of Ga droplets, indicating that any excess Ga desorbed from the surface during growth.

Following growth, RTDs of six different sizes (63, 30, 20, 12, 7.5, and 4 $\mu m^2$) were fabricated using maskless optical photolithography and standard device processing methods. Device mesas were dry-etched with a $Cl_2/BCl_3$/Ar-based inductively coupled plasma reactive ion etch (ICP-RIE) process. Top and bottom Ti/Al/Ti/Au metal contacts were patterned simultaneously and deposited by e-beam evaporation. Device isolation pads were patterned and etched with the same process used for the mesa etch. Plasma enhanced chemical vapor deposition (PECVD) was used to deposit 250 nm of SiNx for sidewall passivation and device encapsulation. The PECVD SiNx film stress was controlled using a previously-developed high/low frequency switching recipe. Contact vias were patterned and dry-etched by a $SF_6$-based ICP-RIE process. To facilitate switching speed measurements, thick Ti/Au (20/800 nm) ground-signal-ground (GSG) pads were patterned and deposited by e-beam evaporation.

DC current-voltage (I-V) measurements were performed on devices at room temperature using a Keithley 2400 source-measure unit. Linear and circular transmission line method (TLM) measurements were performed in order to determine the top and bottom contact resistance; both were found to be roughly between $1\times10^{-6}$ and $6\times10^{-6}$ $\Omega\cdot cm^2$. Temperature-dependent I-V measurements between 7 K and 290 K were performed on selected devices in vacuum using a Lakeshore CRX-VF variable temperature probe station. A Tektronix DPO77002SX 70 GHz real-time oscilloscope was used to measure the switching characteristics of typical devices.

Representative current density versus voltage curves (J-Vs) for each device area are displayed in Figure 1(a). Three resonant interactions were routinely observed below a bias of +5.5 V. Over 300 devices were tested, ~90% of which were operational, i.e., exhibited room-temperature NDR. Microscopic inspection indicated the non-operational devices exhibited signs of fabrication errors. The peak and valley current densities for the predominant ($2^{nd}$) NDR region, $J_p$ and $J_v$ respectively, were determined for all operational devices, with the mean and standard deviation (error bars) for each device area displayed in Figure 1(b). As can be seen in the figure, both $J_p$ and $J_v$ are effectively independent of device size for device areas greater than 10 $\mu m^2$. The small increase in current densities for device areas less than 10 $\mu m^2$ suggests the possible presence of a perimeter dependent leakage current mechanism.

The mean and standard deviation of the room temperature peak-to-valley current ratio (PVCR = $J_p/J_v$) for the $2^{nd}$ NDR region are shown for each device area in Figure 1(c). The PVCR exhibits very little dependence on device size, and is remarkably uniform over an order of magnitude range in device area. Furthermore, the minimal variability in PVCR across devices of the same size attests to the uniformity of the growth and device processing. A typical device on this sample exhibited a PVCR of ~1.85. The maximum PVCR observed was 2.03, which is the largest recorded PVCR for any nitride-based RTD to date.

As a measure of the stability of the room-temperature NDR, three thousand sequential I-V curves were measured for a 4×5 $um^2$ device between 0 and +6.0 V with a +50 mV step. Each voltage sweep took 10 seconds, with a 3 second wait period between successive sweeps. Selected I-V curves, as well as the mean and standard deviation of all curves, are shown in Figure 1(d). Relative to the mean, the standard deviation is typically ~0.1%. Of note, the standard deviation of the $2^{nd}$ NDR region's peak is only 600 nA [green circle in Figure 1(d)], indicating remarkable

stability across 3000 sweeps. Additionally, select IVs from an 800 sweep hysteresis study are illustrated in Figure 1(e). This device was measured by starting the bias voltage at -4 V and sweeping up to +5.75 V and then back down to -4 V. An obvious lack of hysteresis is observed in the main NDR region [Figure 1(e)]. Furthermore, the commonly reported asymmetry between positive and negative bias is present.

Temperature dependent I-V measurements were performed in order to learn more about the current mechanisms comprising each of the three NDR regions. Figure 2(a) displays semi-log I-V curves of a 12 $\mu m^2$ device at 7, 10, 25, 100, 150, 200, 250, and 290 K. As apparent in Figure 2(a), there is a sudden increase in the low-voltage current as the temperature is increased from 25 K to 100 K. Similar behavior was also reported by Encomendero et al. between 4.2 and 35 K, which they attributed to thermionic emission over the double AlN barrier active region. [19]

A quantum transport solver based on a non-equilibrium Green's function (NEGF) formalism was used to analyze the device structure in Fig. 1(a)(inset). This formalism involves a self-consistent 1-D Poisson–NEGF numerical calculation which utilizes a finite difference approximation of Schrodinger's equation as a resonance finder. [30] The readers can find more information on the simulation parameters in the supplemental section of Ref. 22 or in the appendix of Ref 31. The quasi-bound energy levels of the three states in the GaN quantum well and the single state in the emitter pre-well as a function of external bias, shown in Figure 2(b), were extracted from the simulation. The voltage values were then adjusted in order to account for contact resistance. The pre-well in a nitride-based RTD differs from that of traditional RTD material systems, i.e. arsenides or antimonides, in that it is present before a voltage is applied and much deeper as a result of the polarization found at its heterointerfaces. This effect results in a pre-well state that is ~0.25-0.30 eV below the Fermi level at a bias of 0 V.

Three regions of bias voltage [labeled i, ii, and iii in Figure 2(a)] were identified in the experimental I-Vs at which there consistently existed either NDR or an inflection. Comparison of Figures 2(a) and 2(b) reveal that the voltage biases corresponding to the three NDR regions roughly correspond to biases at which the quantum well energy levels align with $E_F$ or the pre-well quasi-bound state energy. Figures 2(c) and 2(d) show the temperature dependent I-V curves measured at the first NDR region and the simulated energy band diagram and quasi-bound states at that external bias, respectively. Data corresponding to the second and third NDR regions are plotted similarly in Figures 2(e) and 2(f) and Figures 2(g) and 2(h), respectively. Note that in the second NDR region [Figure 2(e)], $J_p$ does not vary in the temperature range investigated, whereas there is a clear dependence of $J_p$ on temperature in the first and third NDR regions [Figures 2(c) and 2(g)]. The temperature dependence of $J_p$ in the first and third NDR regions indicates a thermal enhancement of the population of electrons near $E_F$, which then tunnel resonantly through the active region. Furthermore, this indicates the sudden jump in low-voltage current is likely a consequence of a greater number of injected electrons gaining enough energy to surmount the small injection barrier which precedes the pre-well [illustrated on the emitter side of the band diagrams in Figures. 2(d), 2(f), and 2(h)], and then tunneling through the double AlN barrier active region. By contrast, the distribution of quantum states in the pre-well is largely independent of temperature, leading to the near-constant $J_p$ in the second NDR region. However, the PVCR of the second NDR region increased from 2.03 at RT up to 2.52 at 7 K, suggesting that the PVCR is being smeared significantly by a temperature dependent current mechanism in the valley.

Pulsed I-V measurements were also performed at room temperature, and the results (not shown) were very similar in character to the continuous-voltage measurements, indicating the

devices were not strongly affected by Joule heating. Minimal self-heating is to be expected, given the relatively low current density observed in these devices.

Figure 3(a) depicts the mean and standard deviation of $J_v$ for the predominant NDR region plotted against the device perimeter-to-area ratio. Examining the current density as a function of device perimeter-to-area ratio is a standard technique for distinguishing "bulk" current density, $J_B$, from "surface" or "edge" current density, $j_S$

$$J = \frac{I}{A} = j_S \frac{P}{A} + J_B \qquad (1)$$

where J is the total current density, and P and A are the device perimeter and area, respectively. In contrast to the valley current density vs A in Figure 1(b), Figure 3(a) shows that $J_v$ vs P/A exhibits a nearly linear trend for all but the largest devices (P/A > 0.75 $cm^{-1}$). This is likely because $J_B$ is not a true constant, but it instead depends on P/A due to thermal effects. After all, $J_B$ is the bulk current at the valley which is strongly temperature dependent as evidenced in the temperature dependent data displayed in Figure 2. However, for this study we shall assume it is a constant as the effects are minimal. A least-squares fit reveals $J_B$ = 12.04 kA/$cm^2$ and $j_S$ = 4.88 A/cm. The surface/edge current thus constitutes a non-negligible fraction of the overall valley current for the smaller devices. This current mechanism could be comprised of conduction directly through the SiNx passivation layer, corner effects, or leakage along the mesa sidewall surface [illustrated in Figure 3(b)]. Because the devices were grown on a semi-insulating substrate, isolation test structures were fabricated to determine if there was any leakage through the SiNx passivation layer. The test structures consisted of two 100×100 $\mu m^2$ mesas separated by 100 µm, which were etched down to the semi-insulating substrate prior to the SiNx deposition. After testing ten structures, an average current of +10 and -10 nA was observed at bias voltages of +20 and -20 V, respectively, indicating that the SiNx is not contributing to the observed perimeter-based current.

The as-designed devices are all rectangular, but during fabrication, the corners are rounded significantly; therefore, there should be no leakage contribution due to concentrated fields at the corners. This suggests that the perimeter dependent current is solely comprised of leakage along the mesa sidewall surface, which is likely caused by damage during the ICP-RIE mesa etch. Surface treatment studies to mitigate this sidewall leakage current are presently being conducted.

Measurement of the switching behavior of selected devices was carried out in the same manner as we have previously reported. [26,27] The DUT was biased through an Anritsu bias tee with a rise time of 7 ps, where rise and fall times are defined as the time duration between 10% and 90% of the stable levels before and after the switching waveform. The Tektronix real-time oscilloscope has 10%-90% rise times of 5.6 ps and 13 ps depending on which channel is used. The measurements displayed in Figure 4 utilized the 13 ps channel. Connected to the DC port of the bias tee was a ramp signal generator, which provided a DC offset and a 10 kHz triangular waveform to trigger the switching event. The ramp signal was monitored with a second oscilloscope. Finally, the fast Textronix real-time oscilloscope was connected to the RF port of the bias tee. Illustrated in Figures 4(a) and 4(b) are the waveforms measured at the RF port. The measured 10%-90% rise and fall times were 33 ps and 34 ps, respectively. In order to determine the intrinsic DUT rise and fall times, the contribution from the bias tee, $t_{bias}$, and the oscilloscope, $t_{scope}$, must be subtracted from the measured value, $t_{meas}$, with the relationship $t_{rise/fall} = \sqrt{t_{meas}^2 - t_{bias}^2 - t_{scope}^2}$. This results in $t_{rise}$ and $t_{fall}$ values of 29.5 ps and 30.6 ps, respectively. These are the fastest switching times reported to date for AlN/GaN RTDs.

In summary, we have observed record high PVCRs (>2.0) and record-fast switching speeds (<30 ps) in GaN/AlN RTDs. Room-temperature, continuous-voltage I-V characteristics

were repeatable, stable, and hysteresis-free over three thousand consecutive bias sweeps. Low temperature I-V measurements confirmed the presence of three distinct NDR regions, and simulations based on a NEGF formalism illuminated the origin of the temperature-dependent behavior of $J_p$ and $J_v$ in each region. The extremely high yield and remarkable uniformity of the device properties enabled statistical analysis of the peak and valley currents, which indicated there is a non-negligible contribution from surface leakage to the valley current. These results indicate the continued potential of AlN/GaN RTDs for high frequency devices and applications.

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Figure 1: (a) Representative J-V curves for each device size. Data from >300 devices displaying (b) peak and valley current density vs device area and (c) PVCR vs device area, both with standard deviation error bars. (d) IV curves from a 3000 sweep repeatability test (left axis) and the standard deviation at each bias point (right axis). (e) IV curves from an 800 sweep repeatability illustrating a lack of hysteresis in the NDR region regardless of sweep direction. Additionally, the asymmetry between positive and negative bias is displayed.

Figure 2: (a) Semi-log temperature dependent experimental IV curves for a 12 μm2 device. (b) Simulated data illustrating the overlap of the Fermi energy with the first and second quasi-bound states in the QW, as well as the overlap of the pre-well state with the first quasi-bound state in the QW versus bias voltage. The first (c), second (e), and third (g) NDR regions from the IV curve displayed in (a). The corresponding energy band diagrams around the peak voltage for NDR regions i (d), ii (f), and iii (h).

Figure 3: (a) Valley current density vs perimeter to area ratio. (b) Illustration of the possible perimeter-based leakage current sources in a vertical mesa structure. The red arrows indicate leakage through the SiNx layer, the blue arrows designate surface leakage, and the green arrows are corner effects.

Figure 4: The measured (a)10%-90% rise time and (b) 10%-90% fall time for a 20$\mu m^2$ RTD.

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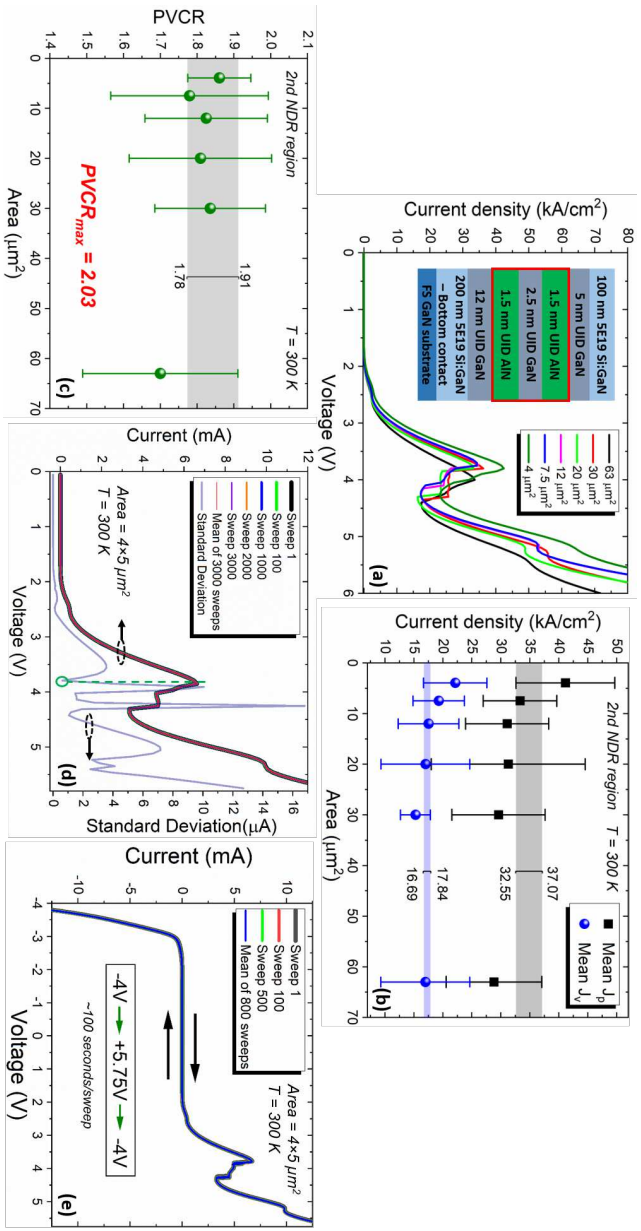

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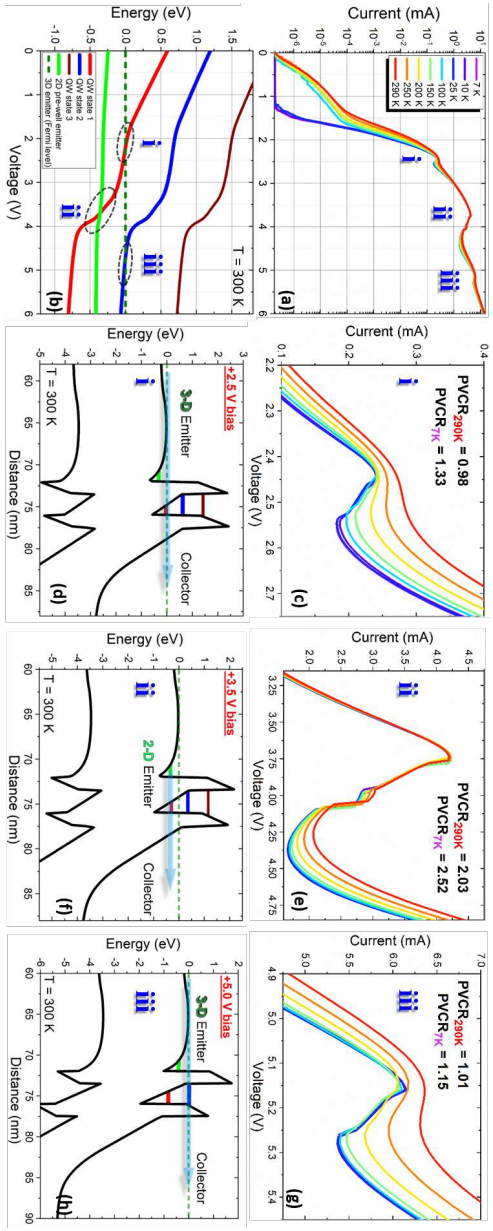

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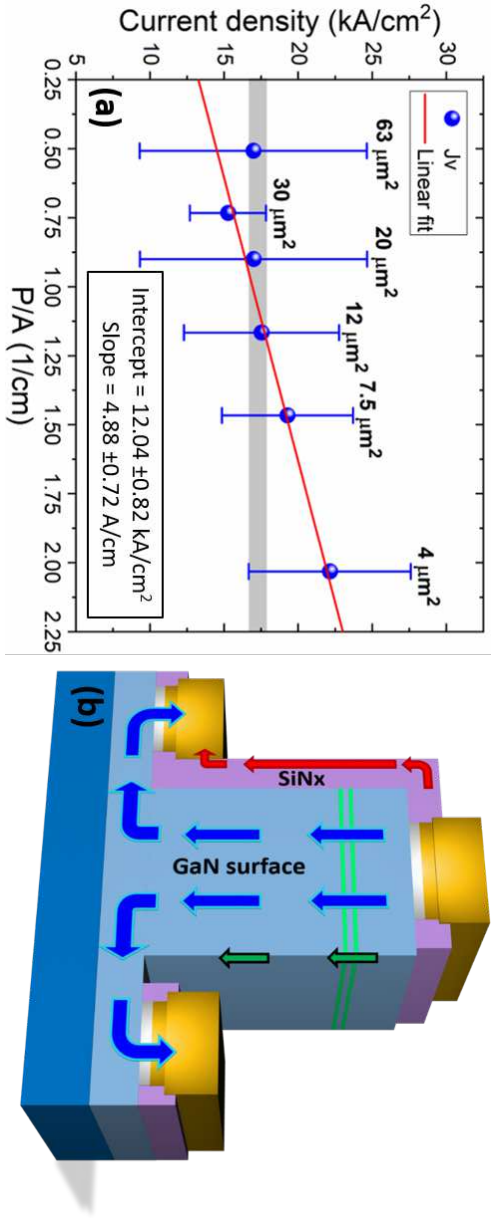

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