Carrier density-tunable work function buffer at the channel/metallization interface for amorphous oxide thin film transistors

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Abstract

With the capability to tune the carrier density of InZnO (IZO), a thin conducting IZO buffer at the channel/metallization interface is introduced to enhance the contact behaviors for amorphous IZO thin film transistors (TFTs). Photoelectron spectroscopic measurements reveal that the conducting IZO buffer, of which the work function (Φ) is *4.37 eV*, relaxes a relatively large Φ difference between channel IZO (Φ*=4.81 eV*) and Ti (Φ*=4.2-4.3 eV*) metallization. The buffer is found to lower the energy barrier for charge carriers at the source to reach the effective channel region near the dielectric. In addition, the higher carrier density of the buffer and favorable chemical compatibility with the channel (compositionally the same) further contribute to a significant reduction in specific contact resistance as much as more than 2.5 orders of magnitude. The improved contact and carrier supply performance from the source to the channel lead to an enhanced field effect mobility of up to 56.49 cm^2/Vs and a threshold voltage of 1.18 V, compared to 13.41 cm^2/Vs and 7.44 V of IZO TFTs without a buffer.

1. Introduction

Over the two decades, amorphous oxide semiconductors (AOSs) and their thin film transistor (TFT) channel application have been intensely explored to realize high performance, transparent and flexible displays. AOS materials, particularly based on indium oxide, demonstrate a high field effect mobility (μ_{FE}=5-20 cm^2/Vs, typically),[1,2] are optically transparent in the visible regime,[1] and can be processed at low temperatures (25-300 °C).[1-2] Significant progress to mitigate issues in AOSs and to obtain reliable TFT performance has been made. The metastable amorphous phase is to be maintained during operation by the addition of Zn and additional third cation species (e.g., Ga, Hf, or Al) as an amorphous phase stabilizer.[3-5] To limit TFT off-state currents, a thin channel layer (10-20 nm) was employed for InZnO (IZO)-based TFTs,[2] or third cations were added to suppress carrier generations in the TFT channel.[3-5] To resolve bias stress-induced instabilities in TFT performance, approaches to employ defect passivation layers or enhance channel/dielectric interfacial compatibility were demonstrated.[6-7]

Metallization contact is also a dominating factor that determines the performance of TFTs. Particularly, it has been reported that high electrical contact resistance significantly sacrifices drain bias applied to the channel, which leads to undesirable power loss during TFT operation and issues for the measurement of TFT field effect mobilities.[2, 8] However, few reports that suggest strategies to enhance contact behaviors are available in the literature. Xu *et al.* previously reported an enhancement of channel/metallization contacts of IZO-based TFTs by employing Ag nanoparticles at the contact interface, yet additional processing complications were inevitably added due to the evaporation of dissimilar materials and relatively high temperature annealing at 300 °C in N_2 required for the formation of Ag nanoparticles.[9] Oxide semiconductors were also employed as a buffer layer at the channel/metallization interface. Huang *et al.* reported the use of

ZnO buffer in IGZO TFTs to promote carrier supplying at the channel/metallization interface, where the carrier injection efficiency may be limited due to the relatively low carrier density of intrinsic ZnO.[10] UV- or plasma-treatments to alter the local carrier density and surface properties adjacent to the channel or underneath of the metallization were reported as an approach to enhance the channel/metallization contact properties.[11-13] However, all of these approaches (1) require an additional fabrication complexity due to the use of additional treatments at relatively harsh conditions such as UV, plasma, or high temperatures, and (2) may lead to adverse effects on the channel material attributed to the chemical incompatibility between dissimilar materials (e.g., Ag nanoparticles to IZO; ZnO to IGZO), and exposures to harsh environments. Therefore, a simple and easy but effective buffer strategy, which does not require any additional process complexities and not sacrifice chemical compatibility, needs to be established to mitigate the contact issues and therefore achieve high performance and low power consumption AOS TFTs. The present study aims to demonstrate an approach utilizing an interfacial buffer layer, which is compositionally homogeneous to the channel to better align work functions between channel and metallization without a significant fabrication complexity and harsh treatment conditions. The compositionally homogeneous interfacial buffer approach is enabled by the capability of tuning carrier density of a binary cation AOS of IZO and hence work function. A series of IZO channel TFTs were fabricated with Ti metallization, where a thin conducting IZO was employed as a buffer layer to relax the relatively large work function difference between channel IZO and metallization Ti, where all the fabrication processes were conducted at room temperature without any additional pre- or post-treatments. In addition, the high carrier density of the buffer IZO is expected to reduce the contact resistance at the channel/metallization interface. The favorable chemical compatibility between the buffer IZO and the channel IZO may further contribute to enhancing contact

properties. In order to identify the effect of compositionally homogeneous IZO buffer with high carrier density on the contact resistance, transmission line model (TLM) analysis was conducted. Photoelectron spectroscopic investigations were used to evaluate the work function of the channel IZO and the conducting buffer IZO, and the effect on the contact properties. The device performance and contact resistance, characterized by TFT/TLM measurements were compared as a function of buffer layer thickness. The present work is unique in that an approach to lower the potential barrier between the source and the effective channel region (located near the channel/dielectric interface, behaving similar to a buried-channel MOSFET[14]) by introducing a contact buffer layer that enhances the field effect mobility and facilitates carrier supply from the source to the effective channel region.

2. Experimental Section

Bottom-gated amorphous IZO-based TFTs were fabricated on SiO_2/Si substrates where thermally-grown 50 nm-thick SiO_2 and heavily-doped Si (0.003-0.005 Ωcm) were used as the gate dielectric and gate, respectively. Channel IZO (20 nm) was deposited using dc magnetron sputtering at a constant power of 20 W and a working pressure of 2×10^{-3} Torr from a procured sintered IZO target (90 wt% In_2O_3 – 10 wt% ZnO). During channel IZO depositions, a mixed gas of Ar/O_2 was used as the sputter gas with a gas volume ratio of 80/20. Source and drain metallization were also made using dc sputtering from a Ti target at a dc power of 40 W and a working pressure of 2×10^{-3} Torr in a pure Ar condition. The channel and source/drain regions were defined with *in-situ* shadow masks. Buffer IZO was prepared from the same IZO target at the same sputter conditions except the sputter gas of pure Ar in order to obtain highly conducting IZO contact buffer layers. The electrical properties (e.g., carrier concentration and Hall mobility)

of the conducting buffer layer were characterized from Hall Effect measurements in the van der Pauw configuration with a small specimen current (~1 nA) and a magnetic field of 5200 Gauss from a C-frame electromagnet (GMW Associates) with a bipolar power supply (KEPCO Inc.). The Hall Effect measurements were conducted in a dark ambient air condition. Prior to the depositions of channel and source/drain metallization, the sputter chamber was pumped down to a base pressure of approximately 3×10^{-7} Torr, and the targets were pre-sputtered for 5-10 mins to remove any surface contaminations on the target surface and achieve uniform gas flow and pressure of the chamber. A semiconductor parameter analyzer (Agilent 4155B) was used to evaluate the TFT device performance in a light-tight probe station under ambient conditions. More than 72 TFT/TLM devices were fabricated and tested for TFTs as a function of buffer thickness to gather reliable data and provide evidence of repeatability.

Chemical states of major elements and work function values were evaluated in an x-ray photoelectron spectrometer (XPS, Thermo Scientific K-Alpha) with focused monochromatic soft Al Kα x-ray radiation at 1486.6 eV under ultra-high vacuum at a pressure below 2×10^{-8} Torr. Prior to XPS measurements, the sample surface was cleaned by Ar cluster ions (Ar_n^+) to remove any surface contaminants where the cluster ion source was employed to limit any chemical damages such as reduction of the oxide due to, known as, preferential sputtering. The cluster ion cleaning was performed for 20 sec at an ion beam energy of 4 keV with a cluster size of 1000, resulting in a cluster energy per nucleon of 4 eV/nucleon. During the work function measurements, the IZO films were biased with respect to earth at a voltage of -30 V by the conducting sample stage, through which the emitted electrons are accelerated, and hence the onset of emission is detected. The spectrometer and the binding energy scale were calibrated with a reference gold specimen to ensure accurate determinations of onset energy and Fermi

level position. A multi-wavelength ellipsometer (FilmSense FS-1) was used to measure film thickness with an incident and detection angle of 65°.

3. Results and discussion

Figure 1 depicts schematics of bottom-gated IZO TFTs without (Figure 1a) and with (Figure 1b) the buffer layer. A highly conducting IZO is inserted as the buffer layer in between the semiconducting channel IZO and the metallization in Figure 1b, of which the compositionally homogeneous buffer is processed using the same IZO target for the channel IZO by only adjusting oxygen potential during the sputtering process. The elemental environment and valence states of the major elements of the buffer IZO are compared with those of the semiconducting channel IZO. The effect of the buffer on the TFT performance and channel/metallization contact behaviors are investigated in this report.

In order to compare the chemical environment and valence states of conducting buffer IZO with those of semiconducting channel IZO, XPS measurements were conducted and the results are shown in Figure 1c and d. Survey scans obtained from both the buffer and channel IZO films are exhibited in Figure 1c, where the spectra are similar to each other with characteristic peaks of major elements of O 1s (at binding energy, BE of 529.2 eV) and O 2s (at 17.5 eV), Zn $2p_{1/2}$ (at 1044.8 eV) and Zn $2p_{3/2}$ (at 1022.5 eV), and In 3d (at 445.1 eV). In the survey spectra, the spin-orbit double lets of In 3d are not prominently seen since the doublets are only spaced in approximately 7.6 eV; however, the core-level high resolution (HR) In 3d XPS plots in Figure S1a clearly show the doublets of In 3d3/2 at 452.3 eV and In 3d5/2 at 444.8 eV, respectively. In Figure S1a and b displaying HR XPS curves of the two cation elements of In (Figure S1a) and Zn (Figure S1b), no significant peak shifts or shape differences were observed between the buffer and channel IZO films. The core-level HR O 1s XPS investigations are

presented in Figure 1d with Gaussian fitting and peak deconvolution. The HR O 1s peaks are deconvoluted into two peaks of stronger O 1s-a at approximately 530.1 eV and weaker O 1s-b at ~531.5 eV, respectively. The stronger peak, O 1s-a at lower BE (on the right) is attributed to the stoichiometric oxygen (i.e., oxygen sufficient state) in IZO[15-17] while the weaker peak, O 1s-b at higher BE (on the left) is due to the oxygen-deficient states,[15-17] implying the presence of oxygen vacancies, known as native doping agents in indium oxide-based semiconductors.[18] In order to exclude any surface adsorption species due to the exposure to the air for the investigation, the surface of both buffer and channel IZO was cleaned with mild cluster Ar ions (Ar_n^+) prior to the XPS measurements. Therefore, hydroxyl groups or water molecules are not responsible for the O 1s-b peak. It should be noted that the areal ratio of the two oxygen components (O 1s-b/O 1s-a) of the conducting buffered IZO (66%) is significantly higher than 27% of the semiconducting channel IZO. According to the native defect-based doping mechanism via the relation $O_O^x = 1/2O_2 + V_O^{\bullet\bullet} + 2e'$, the higher oxygen-deficient component in the buffer IZO indicates the higher carrier density, compared to that of the channel IZO. The resulting carrier density of the buffer IZO is measured to be ~4.6×10^{20} /cm^3 from Hall Effect measurements and the channel carrier density is found to be ~6.7×10^{16} /cm^3 from TLM analysis that is further discussed later in this report.

Amorphous IZO-based TFT devices with and without the interfacial conducting buffer were fabricated to identify the effect of the buffer on the TFT performance. The output characteristics of IZO TFTs are shown in Figure 2 as a function of buffer layer thickness: (a) 0 nm (i.e., no buffer); (b) 10 nm; (c) 20 nm; and (d) 40 nm. The drain currents (I_D) were measured as drain bias (V_D) increases from 0 to 20 V and gate bias (V_G) ranges from -4 to 10 V in a 2 V step. All the output curves shown in Figure 2 exhibit strong drain current saturation with no

current crowding, particularly at the low drain bias regime, V_D<1 V. The saturation drain current of all the buffered TFTs is significantly higher, compared to that of TFTs without a buffer. As a figure of merit, output characteristics are plotted on the same I_D scale. For the TFT without a buffer (i.e., 0 nm-buffered TFT), due to the resulting smaller I_D than those with a buffer, an extended regime (dashed box) of the plot is shown as inset in Figure 2a. At a gate bias of 10 V, a drain current of approximately 0.04 mA was obtained for the 0 nm-buffered devices; increased to ~2 mA for the 10 nm-buffered; further enhanced to ~6 mA for the 20 nm-buffered; and then decreased to ~1 mA for the 40 nm-buffered TFT. This change in saturation current is obviously explained by the carrier injection capability, depending on buffer layer thickness. The buffer layer effect on the contact behavior and TFT performance is further discussed later with TLM analyses.

Figure 3 shows the transfer characteristics of the IZO TFTs with (a) no buffer layer (or 0 nm buffer), (b) 10 nm buffer, (c) 20 nm buffer, and (d) 40 nm buffer. Plots of I_D *vs.* V_G are presented on the left axis and plots of $(I_D)^{1/2}$ *vs.* V_G are displayed on the right axis of the figures. From the I_D-V_G plots (left), the drain current on/off ratio of the TFT devices was evaluated from the minimum and maximum currents. High on/off ratios, greater than 10^6 were obtained for all the TFTs and a maximum ratio of approximately 10^8 was obtained from the 40nm-buffered IZO TFTs. The device saturation field effect mobility (μ_{FE}) and the threshold voltage (V_T) of the IZO TFTs were estimated from the $(I_D)^{1/2}$-V_G plots (right) using the following equation, which relates the drain current to μ_{FE}, V_G, V_T, oxide capacitance (C_{ox}), and the device aspect ratio of channel width (W) to length (L):

$$I_D = \mu_{FE} C_{ox} \frac{W}{2L} (V_G - V_T)^2 \quad (1)$$

It should be noted that the field effect mobility of the IZO TFTs with buffer layers considerably increased, compared to 13.41 cm^2/Vs without a buffer layer: 41.74 cm^2/Vs for IZO TFTs with a 10 nm buffer; 56.49 cm^2/Vs for 20 nm-buffered devices; and 21.15 cm^2/Vs for 40 nm-buffered IZO TFTs. The threshold voltages of the IZO TFTs with a buffer layer were enhanced to much lower values (~1-3 V), compared to 7.44 V of un-buffered TFTs, which is attributed to the improved carrier supply from the source and hence higher carrier density in the channel of buffered TFTs[2]. The channel carrier density is quantitatively calculated by TLM measurements in the following paragraphs.

In order to investigate the effect of the buffer layer between channel and metallization on the channel/metallization contact properties, TLM measurements were made on sets of buffered IZO TFTs with different metallization spacing from 200 to 1000 μm at 200 μm steps, of which the TLM structure is presented in Figure S2. The TLM method assumes[19-21] the followings to validate the investigations: (i) horizontal contact geometry, (ii) linear resistance between the metal and semiconductor, (iii) equipotential and low resistivity contact metallization, (iv) identical sheet resistance underlying the contact to that outside contact (i.e., uniform channel resistivity), and (v) planar contact $L_{S/D} > \sim 2L_T$. The relationship between contact resistance, R_C and specific contact resistance, $\rho_{contact}$ is given by:

$$R_C = \frac{1}{W}\sqrt{R_S \cdot \rho_{contact}} \cdot coth\left(\sqrt{\frac{R_S}{\rho_{contact}}} L_{S/D}\right)$$

$$\approx \frac{1}{W}\sqrt{R_S \cdot \rho_{contact}} \qquad (2)$$

$$\approx \frac{\rho_{contact}}{W L_T}$$

where, $L_{S/D}$ is the source/drain contact length (fixed at 200 μm in this study) and L_T is the transfer length defined as $(\rho_{contact} / R_S)^{1/2}$, which is the effective length of the source/drain electrodes. The relation above describes that R_C is approximated to $\rho_{contact}/(WL_T)$ when $L_{S/D} > \sim 2L_T$ (i.e., assumption *(v)* for the TLM measurements) and this value is the minimum value for R_C since $coth(d_{S/D}/L_T)$ is saturated as one (unity) when $L_{S/D}/L_T > \sim 2$. The ratio of $L_{S/D}/L_T$ in this study is greater than 13 as L_T of each TFT is shown in Figure S3, which is valid for the TLM analysis. Rearrangement of (2) yields the specific contact resistance, $\rho_{contact}=(R_C \cdot W)^2/R_S$.

From a series resistance model, a total resistance measured from the linear regime (at V_D=0.2 V in this study) of output curves consists of the two contact resistances ($2R_C$; source and drain) and the channel resistance (R_{ch}) as $R_{Total}=2R_C+R_{ch}$, where the R_{ch} is expressed with channel sheet resistance (R_S) and channel width and length, $R_{ch}=(R_S \cdot L)/W$ [2, 22]. The R_{Total} measured from each TFT as a function of electrode spacing (L or the channel L of each TFT portion in the TLM structure) and V_G is shown in Figure S2(a-d) with detailed parameter (e.g., R_C, R_S) extraction procedures. From the approach, the channel resistivity ($\rho_{channel}$) of the IZO TFTs were determined by the relation of $\rho_{channel}=R_S \times t$ where t is the channel thickness. Figure 4a shows the channel resistivity of the IZO TFTs as a function of metallization buffer thickness as well as the gate bias applied. An inset shows a magnified view of the dashed box in the $\rho_{channel}$ plot. For all the IZO TFTs, the channel IZO is shown to be well modulated in response to the gate field applied, which agrees well with the output and transfer characteristics shown in Figure 2 and 3. It should be noted that the channel resistivity varies with contact buffer layer thickness although all the channel IZO was deposited in identical conditions. For the carrier density at V_G=0 V, we hypothesize that (i) the contact buffer layer facilitates the carrier supply from the source to the (effective) channel IZO of buffered IZO TFTs, compared to IZO TFTs without buffer layers and (ii) buffer layer thickness

is a dominating factor that determines the carrier supply capability. To understand the effect of the contact buffer layer and its thickness on the carrier injection capability of the TFTs, the channel carrier density (n) for each TFT was estimated using the determined channel resistivity in Figure 4a and the extracted saturation mobility (13.41 cm^2/Vs for 0 nm buffer; 41.74 cm^2/Vs for 10 nm buffer; 56.49 cm^2/Vs for 20 nm-buffer; and 21.15 cm^2/Vs for 40 nm buffer) by the equation $\sigma=1/\rho_{channel}=qn\mu_{FE}$. Previous studies on amorphous GaInZnO[23] and IZO[24] reported that the contact resistance at the channel/metallization may underestimate the field effect mobility of AOS TFTs with the channel length shorter than 50 μm while no considerable underestimation was observed in TFTs with channel length longer than 50 μm. In the present study, all the TFT/TLM investigations were performed on TFT devices with the channel length ranging 100-1000 μm and, therefore, the field effect mobility is reasonable to estimate the channel carrier density without significant influences by the contact resistance.

Figure 4b shows the estimated carrier density of the IZO TFTs as a function of buffer layer thickness and gate bias. The channel carrier density of the buffered TFTs is higher than that of un-buffered TFTs at all the gate biases including zero bias. This higher channel carrier density of the buffered TFTs at zero gate bias can be understood by the energetic bombardment of reflected ions from the oxygen deficient sputter plasma during buffer IZO depositions, which would increase the oxygen vacancy concentration and hence free carriers.[22] Additional oxygen vacancies (or free carriers) may be further injected from the conducting buffer IZO to the channel IZO to obtain the same electrochemical potential (i.e., Fermi energy) in the two layers. It should also be noted that at a zero gate bias, among the buffered TFTs the carrier density is nearly the same regardless of buffer layer thickness. Therefore, the channel resistivity variance at V_G=0 V is attributed to the different carrier mobility of the buffered TFTs. At higher gate biases,

the carrier density increases in all the TFTs due to the injection of carriers to the channel in response to the gate field applied. Among the buffered devices, TFTs with a 20 nm-thick buffer show the highest increase in carrier density, and TFTs with a 40 nm buffer are shown to have the least increase. The significance of the carrier density trend as a function of buffer thickness is three-fold. First, the trend of estimated carrier density is in good agreement with the output and transfer characteristics shown in Figure 2 and 3 – TFTs with higher channel carrier density leads to higher on and off drain currents, and lower threshold voltages (or shift to the negative direction).[2] Second, in the carrier density regime below 10^{20} /cm^3, it is known that higher carrier density leads to higher carrier mobility due to the charge screening effect,[18, 25] which agrees with the values of field effect mobility of the TFTs in this study: higher carrier mobilities were obtained from the TFTs with higher channel carrier density. Third, the overall carrier supply from the source to the channel is considerably enhanced by the addition of a contact buffer layer and depends on buffer layer thickness.

In order to evaluate the carrier supply performance of the contact of the IZO TFTs, the difference between carrier densities at V_G= 0 and 10 V ($\Delta n = n_{10V} - n_{0V}$) is determined and the results are shown in Figure 4c. The channel carrier difference, Δn, which indicates the injected carriers (per unit volume) into the channel by the gate bias application, is significantly higher in the buffered TFTs (4-10 × 10^{17} /cm^3, depending on buffer thickness and gate bias), compared to that (0.4 × 10^{17} /cm^3) of the TFTs without an interfacial buffer (i.e., up to ~25 times differences). Therefore, it is concluded that a conducting buffer layer leads to a significant enhancement in carrier supply ability for AOS TFTs. In TFTs with a 10 nm- and 20 nm-thick buffer, the contact enhancement effect is dominant on the carrier injection. However, a reduced carrier supply from the source was observed in TFTs with a 40 nm buffer, compared to those of TFTs with thinner

buffer layers. This is likely attributed to that the carrier transport becomes a limiting factor for thicker buffer layers. The mean free path (L_{mean}) of the carriers in conducting IZO buffer is found to be approximately 15.6 nm via the equation $L_{mean}\sim(h\mu/q)(3n/\pi)^{1/3}$, where h is the Planck constant, q is the unit charge of electron[26-27]. For the L_{mean} calculation of the conducting buffer layer, the carrier density, n and carrier mobility, μ values of 4.6×10^{20} /cm^3 and 49.6 cm^2/Vs, determined through Hall Effect measurements, were used. This estimated L_{mean} for conducting IZO means that the carrier transport is limited in a conducting IZO buffer thicker than 15.6 nm due to scattering effects, which supports the reduction in carrier supply observed in TFTs with a 40 nm-thick buffer.

The specific contact resistance, $\rho_{contact}$ of the IZO TFTs were determined from the measured contact resistance and the channel sheet resistance, by the relationship,[2, 22] $\rho_{contact}=(R_C\cdot W)^2/R_S$ and the results are shown in Figure 5. As previously demonstrated for the bottom-gated TFT structures where the gate metallization and gate oxide extend beneath the source/drain contact region, the specific contact resistance is modulated as channel conductance is modulated in response to the gate bias.[2, 22] An inset exhibits the $\rho_{contact}$ plot in log scale. Note that the specific contact resistance of the buffered IZO TFTs considerably decreased, compared to that without a buffer layer. Since all the other fabrication conditions and device components are the same except inserting a buffer between the channel and the metallization, the enhancement of the contact properties is attributed to the addition of the buffer layer. The effect of employing the conducting buffer on the specific contact resistance is two-fold. First, an increase in channel carrier density, evidenced in Figure 4b, leads to a decrease in specific contact resistance, as is clear by the fact that higher carrier density leads to higher current flows at the contact interface. This carrier density-dependent improvement in contact resistance is supported by previous

studies on amorphous IZO and InGaZnO for TFT channel application.[22, 28-29] Second, the inserted interfacial layer better aligns the work functions between the channel and the metallization. Since the work function is defined as the energy to take an electron from the Fermi energy level to the vacuum level, the work function of a material varies with carrier density.[30-31] In many electronic and optoelectronic applications, proper work function matching is critical to facilitate the carrier transport at the active layer/metallization contacts and hence achieve high device performance. Work function alignment toward enhanced contact properties is further detailed with photoelectron spectroscopic investigations in Figure 6. The ratio of contact resistance to total resistance ($2R_C/R_{Total}$) is shown in Figure S4, from which it is clearly observed that the $2R_C/R_{Total}$ ratio of buffered TFTs is much lower than that of un-buffered TFTs. The smaller ratio of buffered TFTs indicates that the loss of drain bias applied to the channel is smaller, which leads to the enhancement of TFT performance and limits power loss during device operations.

In order to analyze the effect of contact buffer layers on the work function alignment at the channel/metallization contact, photoelectron spectroscopic investigations were performed on channel IZO (semiconducting, n=~6.7×10^{16} /cm^3 estimated with TLM the results and μ_{FE}) and buffer IZO (conducting IZO, n=~4.6×10^{20} /cm^3 from Hall Effect measurements). The work function (Φ) is determined by the equation below with the photon energy ($h\nu$=1486.6 eV in this study), the Fermi edge kinetic energy ($E_{F,kin}$), and the onset cut-off kinetic energy (E_{onset}), which is the free electron energy due to the photoelectric effect:

$$\Phi = h\nu + E_{onset} - E_{F,kin} \quad (3)$$

Figure 6 shows onset kinetic energy measurements and Fermi energy level locations for the photo-excitations of channel IZO (Figure 6a and b) and conducting buffer IZO (Figure 6c and d).

The E_{onset} of channel IZO is determined to be 33.79 eV by linear extrapolation in Figure 6a. The position of $E_{F,kin}$ is found to be 1515.58 eV, which is determined by the kinetic energy of the mean of the two linear extrapolated energies in Figure 6b. According to the E_{onset} and $E_{F,kin}$ values, the work function of channel IZO ($\Phi_{channel}$) is then estimated to be 4.81 eV. Similarly, the work function of conducting buffer IZO (Φ_{buffer}), 4.37 eV is determined from Figure 6c and d, with E_{onset} of 33.46 eV and $E_{F,kin}$ of 1515.76 eV. The smaller work function of conducting buffer IZO indicates that the Fermi energy level of the conducting IZO buffer is located higher than that of channel IZO as much as 0.44 eV (i.e., 4.81 - 4.37 eV) since the fermi level of n-type semiconductors shifts toward higher energy with increasing carrier density.

According to the work function measurements in Figure 6a-d, schematics of band alignments were constructed under a positive V_G and V_D condition. For the E_C and E_V locations, it is reasonably assumed that the Fermi energy location of the conducting buffer IZO with the carrier density of 4.6×10^{20} /cm^3 is placed at the conduction band minimum (i.e., E_C). Therefore, the location of E_C for the conducting buffer IZO is the same as the Fermi energy level, identified from work function measurements for the conducting buffer. From the E_g values determined from UV-Vis, shown in Figure S5, the location of E_V of the conducting buffer IZO can also be determined (i.e., $E_V=E_C-E_g$). The E_C and E_V locations of channel IZO were assumed to be the same for this analysis since the only difference between these compositionally homogeneous buffer and channel layers is the carrier density. In the constructed band diagrams, the effect of the buffer layer on the carrier supply to the effective channel region at (or near) the channel/dielectric interface is visually described in Figure 6e and f. It should be noted that since bottom-gated TFTs behave as buried-channel field effect transistors, the effective channel forms near the dielectric layer, away from the source metallization. For the IZO TFTs without the buffer in Figure 6e, the larger work function

difference (>~0.5 eV) between the metallization (~4.2-4.3 eV)[32-33] and the channel IZO (4.81 eV) results in a large downward band-bending in the channel and an energy valley at the source (metal)/channel interface. Therefore, a high energy barrier (Ψ) is created, which is defined as the energy difference between the energy for charge carriers near the source/channel interface (blue dash; E_C in this case) and the peak energy (red dash) for charge carriers to overcome so that the carriers arrive at the effective channel region (near the dielectric). Due to the high energy barrier, Ψ shown in Figure 6e, the carrier supply from the metallization to the effective channel is limited. However, for the IZO TFTs with the buffer shown in Figure 6f, the Fermi level of the conducting buffer IZO is more closely aligned with the metallization (i.e., similar work functions of Φ_{buffer}= 4.31 eV and Φ_{Ti}=4.2-4.3 eV). This better energy alignment favors the carrier injection from the metallization to the buffer IZO and the lower barrier (Ψ_{buffer}) facilitates the further supply of the carriers from the source (metal) to the effective channel region near the dielectric.

4. Conclusion

The ability to tune the carrier density in IZO is emphasized to enhance the channel/metallization contact behaviors of amorphous IZO TFTs. The insertion of compositionally homogeneous and highly conducting IZO (n=~4.6 × 10^{20} /cm^3) as a buffer significantly lowers the specific contact resistance by better aligning work functions of the channel and metallization, and hence improving carrier supply performance from the source to the effective channel region. In addition, the enhanced carrier supply performance was shown to lead to higher carrier mobility since the charge carrier transport in indium oxide-based amorphous semiconductors is governed by the charge screening mechanism in the carrier density regime < ~10^{20} /cm^3. Much higher field effect mobility (up to ~56.5 cm^2/Vs) was obtained from buffered IZO TFTs, compared to 13.4 cm^2/Vs of un-buffered devices. The demonstrated buffer

approach with carrier density tunability is expected to improve TFT performance for next-generation fast switching display applications by reducing contact resistances, limiting the loss of voltages applied to the channel, and enhancing the carrier mobility.

ASSOCIATED CONTENT

Supporting Information. HR XPS spectra of major cation elements (In and Zn) obtained from conducting buffer IZO and channel IZO; R_{Total}-L plots for TLM analysis; Transfer length (L_T) as a function of buffer thickness; Contact resistance and contact resistance to total resistance ($2R_C/R_{Total}$) as a function of buffer thickness and gate bias; Optical bandgap of conducting buffer and channel IZO. "This material is available free of charge via the Internet at http://pubs.acs.org."

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Author Contributions

M. Liu and H. Kim contributed equally to this work. M. Liu, H. Kim, and S. Lee designed the experiments and wrote the manuscript; M. Liu and X. Wang fabricated devices and evaluated TFT performance; H. W. Song and K. No conducted contributed to data analyses and writing the manuscript.

Notes

The authors declare no competing financial interest.

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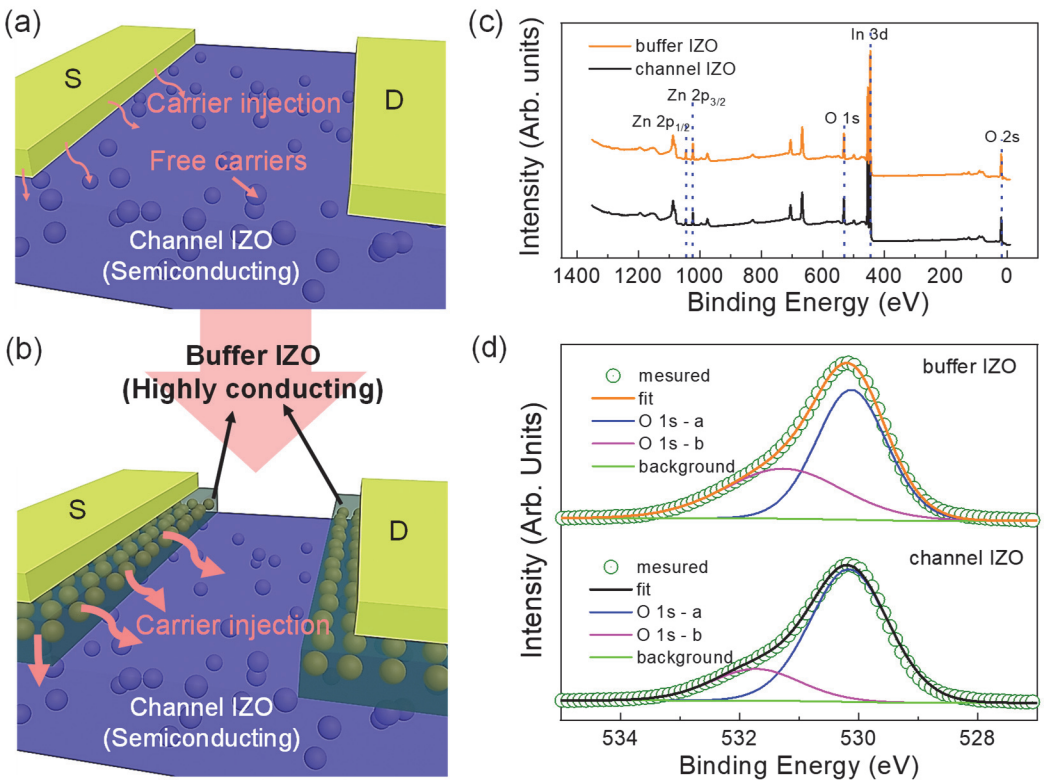

Figure 1. Schematics of the IZO-based TFTs in a typical bottom-gated configuration (a) without a buffer layer and (b) with highly conducting IZO buffer at the channel/metallization interface. The conducting buffer IZO and semiconducting channel IZO are processed from the same IZO target using identical sputtering conditions except oxygen potentials in the sputter gas, ensuring process simplicity and greater chemical compatibility than other buffers using dissimilar materials; XPS investigations of buffer and channel IZO films: (c) survey scans in the BE range of 0 to 1400 eV, showing similar spectra to each other for the peaks from major elements of O, In, and Zn and (d) core level HR XPS spectra of O 1s peak deconvoluted into O 1s-a and -b, which representing stoichiometric oxygen and oxygen deficient states, respectively, for the conducting buffer IZO (upper) and the semiconducting channel IZO (lower).

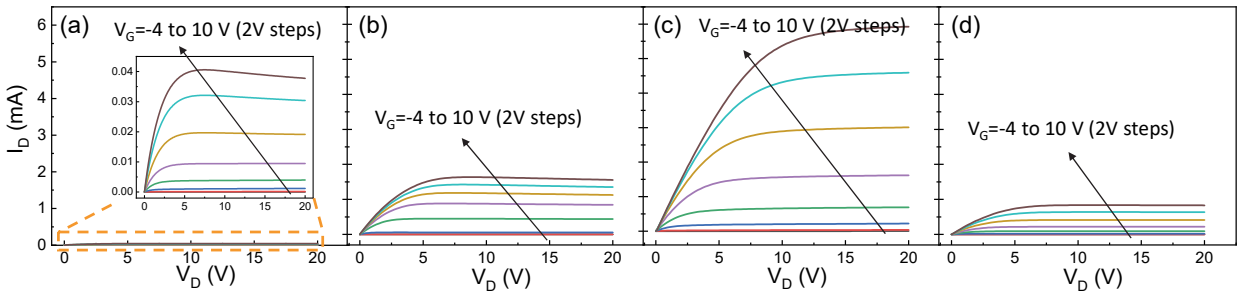

Figure 2. Output characteristics of IZO TFTs as a function of buffer layer thickness: (a) 0 nm buffered, (b) 10 nm-buffered, (c) 20 nm-buffered, and (d) 40 nm-buffered TFTs with the channel width and length ratio of W/L=2000 μm/100 μm.

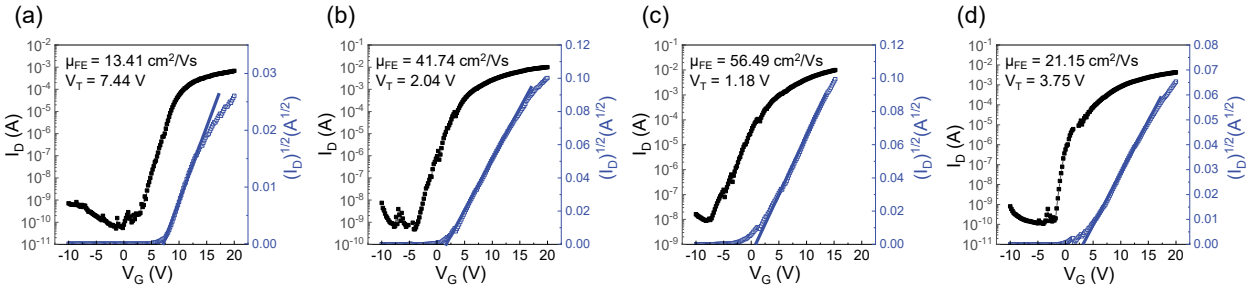

Figure 3. Transfer characteristics of IZO TFTs as a function of buffer layer thickness: (a) 0 nm buffered, (b) 10 nm-buffered, (c) 20 nm-buffered, and (d) 40 nm-buffered TFTs. The extracted field effect mobility and the threshold voltage of buffered TFTs are found to be significantly enhanced, compared to those of un-buffered IZO TFTs.

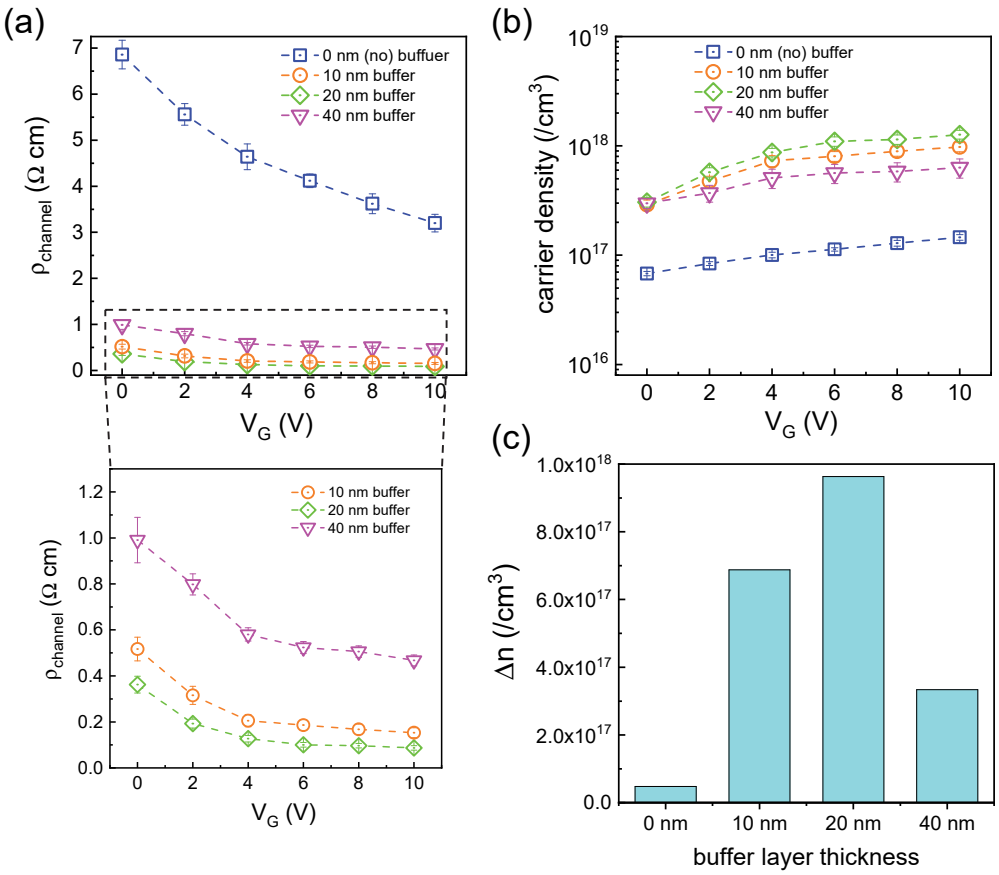

Figure 4. (a) Channel resistivity, $\rho_{channel}$ of the IZO TFTs as a function of buffer layer thickness and gate bias, determined from TLM measurements where the channel resistivity of buffered TFTs is much lower, compared to that of IZO TFTs without a buffer layer. An extended $\rho_{channel}$ regime for the buffered TFTs is shown as inset; (b) channel carrier density of the IZO TFTs extracted from TLM analyses; and (c) carrier density difference, Δn between carrier densities at V_G=10 and 0 V.

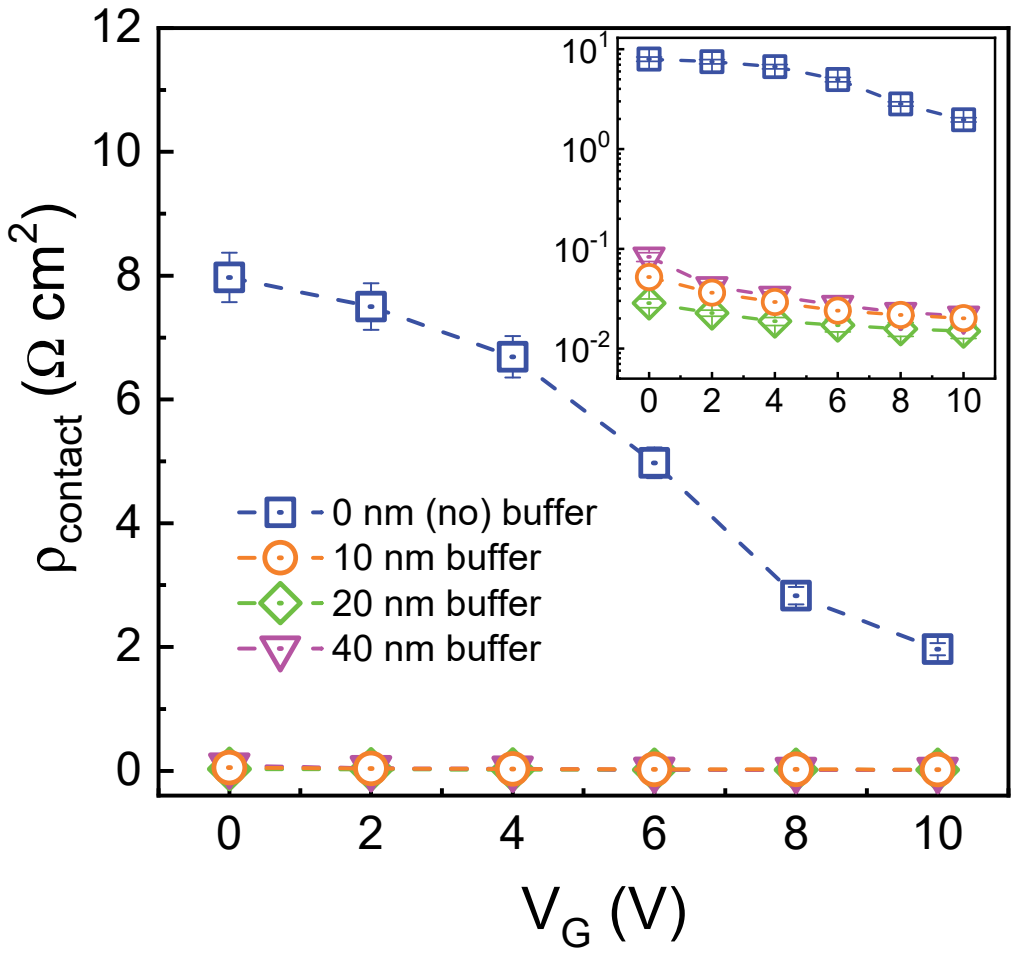

Figure 5. Specific contact resistance of IZO TFTs as a function of buffer layer thickness, determined from TLM measurements. The specific contact resistance of buffered TFTs decreases more than two orders of magnitude than that of IZO TFTs without a buffer layer.

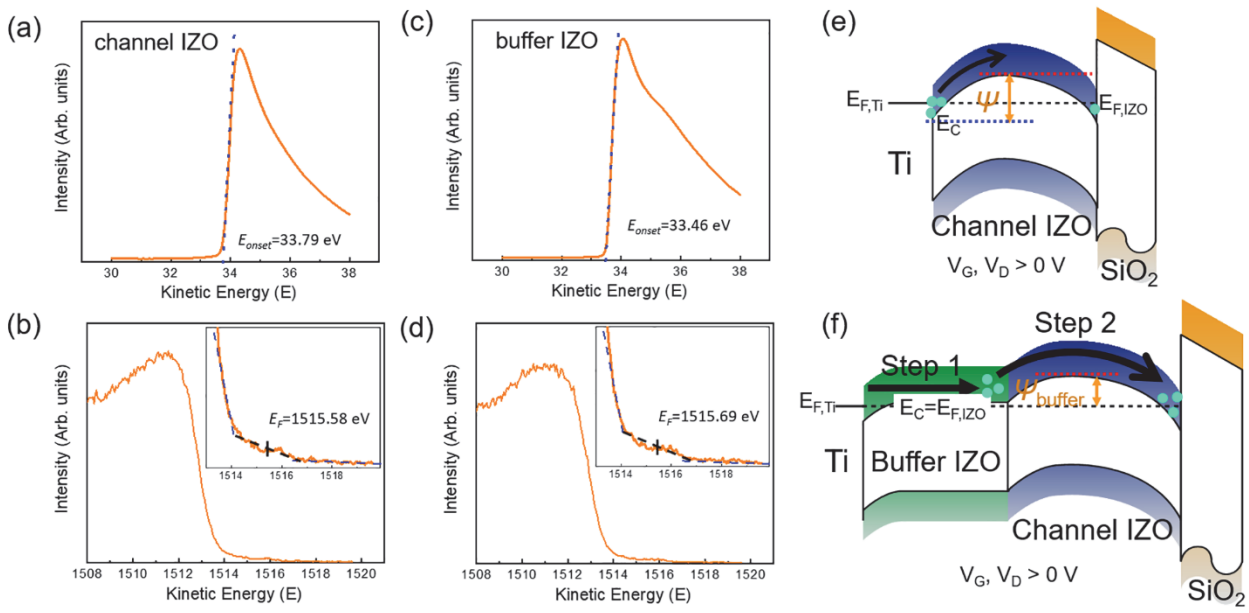

Figure 6. Work function measurements through photoelectron microscopy: the work function of the channel IZO (semiconducting) and the buffer IZO (conducting) was evaluated from onset cut-off energy and Fermi energy measurements on (a and b) channel IZO and (c and d) buffer IZO films, respectively where the work functions were determined to be 4.81 eV for channel IZO and 4.37 eV for buffer IZO, indicating the E_F position is located higher (close to that of metallization Ti, ~4.2-4.3 eV) than that of channel IZO; Schematics that compare the band alignment and carrier injection capability from the metallization to the effective channel near the dielectric: (e) IZO TFTs without the buffer and (f) with the buffer, where the lower barrier energy of the buffered TFTs due to the better Fermi energy alignment facilitates the carrier injection.

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