

Air-stable n-type transistors based on assembled aligned carbon nanotube arrays and their application in complementary metal-oxide-semiconductor electronics

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ABSTRACT

Carbon nanotubes (CNTs) are ideal candidates for beyond-silicon nano-electronics because of their high mobility and low-cost processing. Recently, assembled massively aligned CNTs have emerged as an important platform for semiconductor electronics. However, realizing sophisticated complementary nano-electronics has been challenging due to the p-type nature of carbon nanotubes in air. Fabrication of n-type behavior field effect transistors (FETs) based on assembled aligned CNT arrays is needed for advanced CNT electronics. Here in this paper, we report a scalable process to make n-type behavior FETs based on assembled aligned CNT arrays. Air-stable and high-performance n-type behavior CNT FETs are achieved with high yield by combining the atomic layer deposition dielectric and metal contact engineering. We also systematically studied the contribution of metal contacts and atomic layer deposition passivation in determining the transistor polarity. Based on these experimental results, we report the successful demonstration of complementary metal-oxide-semiconductor inverters with good performance, which paves the way for realizing the promising future of carbon nanotube nano-electronics.

KEYWORDS

carbon nanotube, field effect transistor, air-stable, complementary metal-oxide-semiconductor

1 Introduction

In recent years, intense research and studies have been conducted on the new generation of materials for energy-efficient and high-speed nano-electronics after silicon transistors approach their physical and theoretical limits [1–4]. Carbon nanotube (CNT), due to its one-dimensional nature and excellent electronic properties, is a promising channel material that can enable high-performance and multi-functional (such as flexible and wearable) electronics [5–17]. Significant accomplishments have been made on both performance and scaling for carbon nanotube field effect transistors (FETs) [9–11, 18–22]. However, most of the previous work studied either individual or carbon nanotube random networks. Recently, aligned nanotubes based on assembling pre-separated semiconducting carbon nanotubes have emerged and served as an important platform for advanced CNT electronics [23–25]. In 2016, Brady et al. reported the floating evaporative self-assembly (FESA) technique to assemble high-semiconducting-purity nanotubes into aligned high-density arrays on SiO₂ or quartz substrates [23]. Aligned nanotube arrays enjoy the benefits of not only the high aligned nanotube density, but also fewer defects in the transistor channel area. CNT array transistors can take advantage of simultaneous contributions of the carrying currents passed by multiple-nanotube channels to achieve high current densities [23, 24].

Quasi-ballistic p-type behavior FESA carbon nanotube array transistors with a saturated on-state current density exceeding silicon have been achieved when compared at the same gate oxide thickness and off-state current density [24]. Besides, p-type behavior carbon nanotube array transistors were investigated for radio frequency electronics and Rutherglen et al. observed excellent radio frequency performance, which operated at over 100 gigahertz frequencies and is close to that of GaAs technology [26–29]. Furthermore, Liu et al. demonstrated high-density nanotube arrays (> 100 CNTs per micrometer) for high-performance electronics [25].

As for now, the work on such high-density, aligned carbon nanotube arrays have barely reported n-type behavior transistors. However, obtaining both p-type and n-type transistors is of great importance in realizing the promising future of complementary nano-electronic circuits with low steady-state power dissipation and short stage delay [15, 22]. Even though significant research work was devoted to producing n-type behavior transistors based on individual nanotubes or nanotube networks, many scientific challenges still need to be solved for reliable industrial-scale applications of aligned nanotube arrays [23, 30–35]. Semiconducting CNTs are usually p-type materials in atmosphere due to the adsorption of oxygen [36]. Many groups including our own have researched techniques to convert CNT to n-type material, such as chemical doping [33, 37],

using metal contacts with small work functions (Gd, Sc, or Y) [23, 33–34], and passivating CNT with atomic layer deposition (ALD) [22, 30–32]. However, whether these techniques can be extended to assembled aligned CNT array devices is not clear so far. Importantly, the carrier transport mechanisms can be different between long-channel transistors (channel length $\gg$ nanotube length) and short-channel transistors (channel length $\ll$ nanotube length). The effects of metal contacts and ALD passivation on assembled aligned CNT arrays need to be systematically studied to provide a reliable and robust n-type conversion method. Long-term stability and standard fabrication compatibility are needed for future semiconductor electronics. It is thus necessary to investigate and develop an n-type conversion method for aligned CNT array FETs with short channel lengths, and to study ways to mitigate any adverse effects.

Here, by taking advantage of the FESA platform [24, 25], we have successfully achieved aligned, high-density, and high-semiconducting-ratio carbon nanotubes and fabricated FESA CNT FETs of various channel lengths from 100 nm to 10 μm . The mechanism of carrier type has been systematically studied to shed light on the importance of factors affecting the n-type conversion process. We have found that for FESA CNT FETs (with ALD passivation) with channel length $\sim$ 100 nm, the transistor polarity is dominated by the work function of source/drain metal contacts. We attribute this to the direct contact carrier transport in short-channel transistors. We have then combined the use of Ti contacts and ALD passivation to obtain air-stable n-type behavior CNT FETs with high on-state current density $\sim$ 130 $\mu\text{A}/\mu\text{m}$, while maintaining large on/off ratio of $> 10^6$. The use of Ti contacts is particularly interesting as Ti is a metal with moderate work function (as compared to low-work function metals such as Gd, Sc), and while Ti contacts are widely used for III-V semiconductors, it has not been thoroughly studied as nanotube contacts. A complementary metal-oxide-semiconductor (CMOS) inverter is also demonstrated using the as-made p-type and n-type behavior CNT FETs. Our experimental demonstration and understanding of the transport behavior in aligned CNT array transistors can help the development of future high-performance aligned CNT array transistor-based electronics.

2 Results and discussion

The high-density, well-aligned semiconducting nanotubes in this study were deposited using the FESA technique. Details of the aligned CNT arrays on the wafer are presented in the “Isolation and alignment of semiconducting carbon nanotubes” section in Methods. The scanning electron microscope (SEM) images show the uniform aligned nanotube arrays reside in stripes of width $\sim$ 30 μm (Fig. 1(a)). Figure 1(b) shows a zoomed-in image of the aligned region. The tubes are well-aligned with high densities. Inset is the Raman spectra of FESA CNT. The Raman spectrum shows a G-band/D-band peak ratio as high as 17, which verifies that our carbon nanotube arrays are of high quality and with low defects. Figure 1(c) shows the SEM image of the channel area of FESA CNT FET with channel length = 100 nm, where individual carbon nanotubes can be clearly identified inside the channel area. The nanotube packing density of the FESA CNT film in channel area is determined as $\sim$ 50 tubes/ μm from SEM measurements. Figures 1(d) and 1(e) depict the atomic force microscopy (AFM) image and height profile of the FESA CNT array. Figure 1(f) is the optical image of the as-made CMOS inverter, which is constructed of p-type and n-type FETs based on the aligned CNT array. With the highly aligned and dense nanotube array, excellent transconductance and on-state current can be expected, which would advance the electronic performance of CNT transistors and provide an excellent platform for CNT electronics.

The schematic diagram of the back-gated device structure based on the FESA CNTs is depicted in Fig. 2(a). The active channel areas were selectively chosen to land in the aligned regions. Heavily p-type doped Si was used as the common back gate. The gate dielectric is a thermally grown 15 nm thick SiO_2 layer. High-semiconducting-ratio, densely aligned carbon nanotubes were deposited onto the SiO_2 surface via the FESA technique. Pure 30 nm palladium (Pd) formed the source and drain metal contacts of the transistors (See “Fabrication and measurement of CNT devices” section in Methods). Channel lengths were patterned with 100 nm, 200 nm, 500 nm, 1 μm , 2 μm , 5 μm , and 10 μm with the same channel width ($W = 2 \mu\text{m}$) to study the length scaling behavior. The fabricated aligned CNT

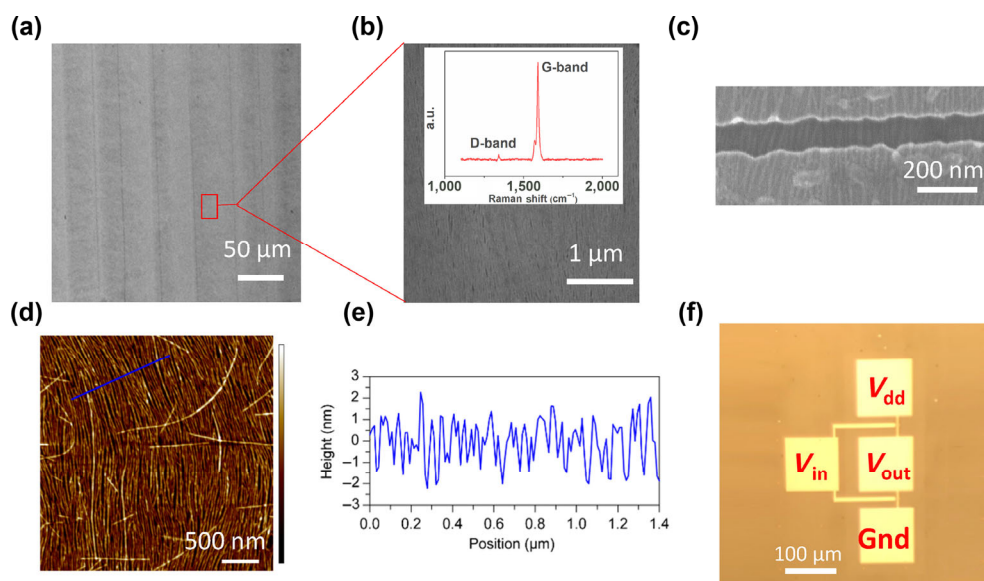


Figure 1 Characteristics of aligned carbon nanotube arrays. (a) and (b) SEM images of the aligned tubes of a larger area (a) and aligned region (b). Inset is the Raman spectra of aligned carbon nanotube arrays. (c) SEM image of the channel area of a CNT FET ($L_{\text{ch}} = 100 \text{ nm}$). (d) and (e) AFM image and height profile of aligned nanotube array. The range of the color scalebar to the right of the AFM image in (d) is 7 nm. (f) Optical image of the as-made CMOS inverter based on aligned carbon nanotube arrays.

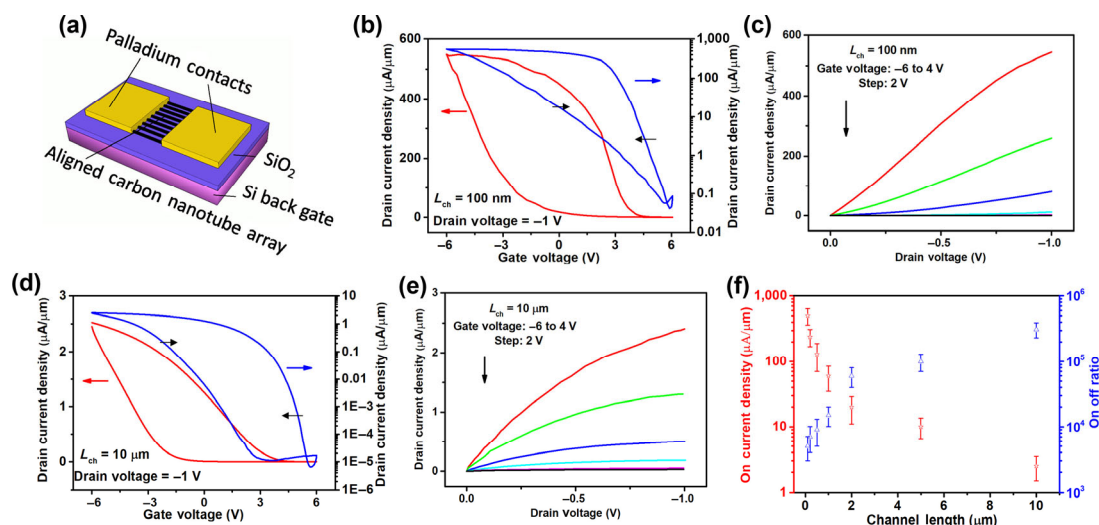


Figure 2 Electronic properties of CNT FETs based on aligned nanotube arrays. (a) Schematic diagram of a back-gated carbon nanotube transistor. (b) I_{ds} – V_{gs} curves of a typical short channel nanotube transistor ($L_{ch} = 100$ nm) in both linear (red) and log (blue) scales. (c) I_{ds} – V_{ds} curves of the same transistor in (b). (d) and (e) I_{ds} – V_{gs} curves and I_{ds} – V_{ds} curves of a typical long channel nanotube transistor ($L_{ch} = 10$ μ m). (f) The averaged on-state current density and on/off ratio for carbon nanotube transistors with different channel lengths. Error bars represent standard deviations from 10 FETs for each channel length.

array FETs were measured with a probe station and semiconductor parameter analyzer to characterize the electrical performance. Holes are the majority carriers injecting into CNTs from Pd electrodes either via tunneling or thermal emission, which leads to typical p-type behavior transistors. The black arrows in the following transfer curves show the forward and backward curves. The electrical performance of CNT FET with channel length = 100 nm is depicted in Figs. 2(b) and 2(c). In Fig. 2(b), the red curve is in the linear scale while the blue curve is in the logarithm scale. We achieved high on-state current density of ~ 520 μ A/ μ m, peak transconductance normalized by width g_m of ~ 163.2 μ S/ μ m, and on/off ratio of $\sim 5,000$ for the back-gated CNT transistor. We studied further on FESA CNT FETs with longer channel lengths. Figure 2(d) presents the I_{ds} – V_{gs} transfer curves of a representative CNT FET with channel length = 10 μ m. We can observe that the transistor shows high on/off ratio of $\sim 2 \times 10^5$, peak transconductance normalized by width $g_m \sim 1.2$ μ S/ μ m, and high current density of ~ 2.5 μ A/ μ m even under relatively small drain bias. The I_{ds} – V_{ds} output curves of the same CNT FET were plotted in Fig. 2(e), which shows output current saturation behavior. A negatively biased drain voltage of 1 V is applied here to measure p-type CNT FETs. In the subsequent measurements, V_{ds} would be positively biased to measure the n-type performance of FETs. We also quantified hysteresis by characterizing the voltage difference (δV) when the drain current equaled half of the maximum value in the measurement. Notably, all of the CNT FETs show large hysteresis ($\delta V = 5.9$ V for channel length = 100 nm, $\delta V = 4.3$ V for channel length = 10 μ m) under double sweep DC measurement. The origin of the prominent hysteresis is believed to be the adsorption of moisture and oxygen at the CNT/SiO₂ interface [38, 39]. Hydroxyl/water groups at the CNT/SiO₂ surface form the electron traps, which are the important factors of large hysteresis in FETs. The electrons in the traps in the vicinity of the CNTs would provide negative gating towards the on-state and lead to large hysteresis. Therefore, ALD passivation is believed to be one route to minimize the effects of oxygen and moisture and drastically reduce the hysteresis [30]. Channel length scaling behaviors of FESA CNT FETs are plotted in Fig. 2(f) to further investigate and understand the carrier transport mechanism and its dependence on the channel lengths. It is found that the on/off ratio decreases with decreasing channel length. There can be a combination of various factors

behind the decreasing on/off ratio phenomenon. One possible factor can be the short channel effects, which include possible tunneling and barrier lowering effects [40]. Another possible factor is the existence of metallic tubes directly bridging the source and drain. Other possibilities include the reduced gate control over the channel with short-channel length as well as the tube-tube interaction due to the densely aligned nature (cross tube junctions are not frequent but can sometimes happen in the active short channel area) [41]. Improving the nanotube pitch uniformity and alignment with minimal inter tube interaction would be necessary in order for CNT arrays to be the candidate for beyond-silicon nano-electronics. As for the on-state current density, it decreases with the increasing channel length, but the extracted field effect mobility (estimated using the standard FET model, see Fig. S1 in the Electronic Supplementary Material (ESM) for more details) shows a relatively weak dependence on channel length (Fig. S1(a) in the ESM) at long channel lengths, which is in agreement with the percolation transport mechanism in carbon nanotube devices [42]. On the contrary, the on-state current and the field effect mobility increase dramatically with the decreasing channel length in the short-channel regime where the channel length is scaled down to nanotube length of ~ 500 nm (Fig. S1(b) in the ESM). This phenomenon can be attributed to the domination of direct contact transport in short channel regime [25]. These experimental results demonstrate the exceptional electrical properties of FESA CNT and can shed light on the importance of charge transport in CNT electronics.

Complementary electronics offer low static power consumption as significant power is only drawn when the CMOS circuits are switching between on and off states. However, CNT FETs often show p-type behavior in the air. An effective n-type conversion method is needed for CNT CMOS integrated circuit applications. We performed a systematic study of ALD passivation on FESA CNT FETs with the different channel lengths, and the experimental results are summarized in Fig. 3. The schematic process diagrams are illustrated in Fig. 3(a). For the ALD approach, a 40 nm Al₂O₃ layer was deposited via ALD to form the gate oxide and 1 nm/50 nm Ti/Au stack was utilized as the top gate electrode. Besides atomic layer deposition, liquid metal reaction media such as Gallium-based liquid alloys can also serve as a solvent for synthesizing Al₂O₃ on the

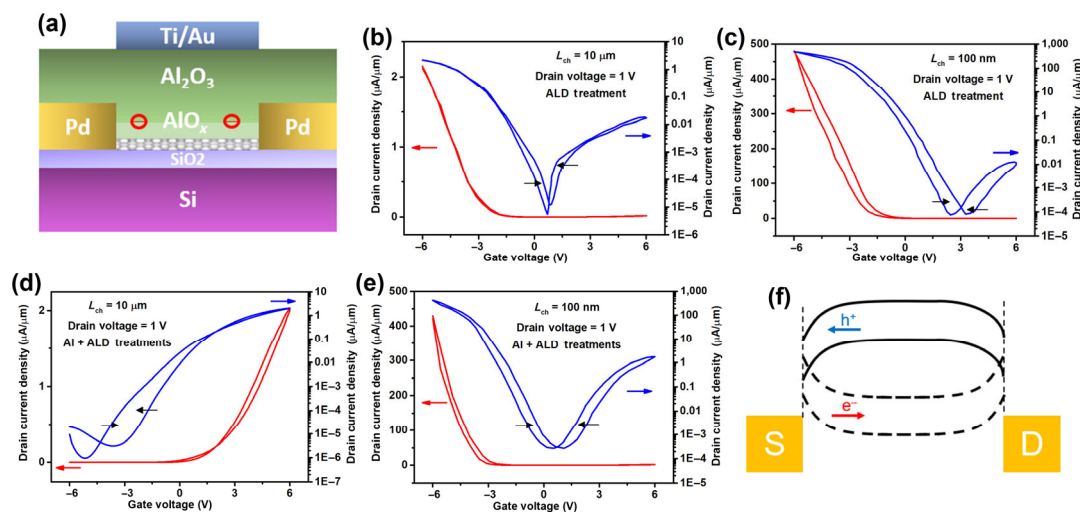


Figure 3 Electronic properties of CNT FETs under ALD passivation. (a) Schematic diagram of a top-gated CNT transistor. (b) and (c) I_{ds} - V_{gs} curves of typical long channel ($L_{ch} = 10 \mu\text{m}$, (b)) and short channel ($L_{ch} = 100 \text{ nm}$, (c)) CNT transistors in both linear (red curve) and log (blue curve) scales after 40 nm Al_2O_3 ALD passivation. (d) and (e) I_{ds} - V_{gs} curves of typical long channel ($L_{ch} = 10 \mu\text{m}$, (d)) and short channel ($L_{ch} = 100 \text{ nm}$, (e)) CNT transistors in both linear (red curve) and log (blue curve) scales after 1 nm Al layer evaporation/oxidation and 40 nm Al_2O_3 ALD passivation. (f) Schematic illustration of n-type conversion process.

aligned CNT array [43]. In addition, we tried an aluminum (Al) assisted ALD passivation approach following the work pioneered by Tang et al. and Wei et al. [22, 31], in which a 1 nm thick Al layer was first evaporated on the channel area. Devices were then heated on the hot plate (120 °C for 1 h) to let the Al layer oxidize in air. We found that the formed AlO_x layer would aid the subsequent ALD process to ensure a harmless and high-yield approach. I_{ds} - V_{gs} transfer curves (both linear and logarithm scale) of typical long channel device (channel length = 10 μm) and short channel device (channel length = 100 nm) with only ALD treatment are shown in Figs. 3(b) and 3(c) respectively. These devices both show a high on/off ratio above 10^6 and nearly hysteresis-free behavior ($\delta V < 0.5 \text{ V}$) as the ALD layers can keep nanotubes passivated from oxygen molecules and moisture in the air. The long channel device shows on-state current density $\sim 2.2 \mu\text{A}/\mu\text{m}$, which is slightly lower than the current before the ALD process. And the long channel devices were turned into ambipolar behavior with n-branch current instead of predominant p-type behavior. The low temperature (80 °C) ALD process baked devices and drove away the oxygen molecules adsorbed in the vicinity of nanotubes. Meanwhile, the deposited Al_2O_3 layer covered nanotubes and prevented the oxygen molecules from being absorbed again. Besides, it is reported that the ALD Al_2O_3 layer can be rich in positive charges because of the deficiency of oxygen atoms, which gives rise to electron conduction and leads to ambipolar behavior [30, 44–46]. The short channel device shows on-state current density $\sim 460 \mu\text{A}/\mu\text{m}$, peak transconductance normalized by width $g_m \sim 210 \mu\text{S}/\mu\text{m}$, subthreshold swing $\sim 300 \text{ mV}/\text{dec}$, and on/off ratio $> 4 \times 10^6$. The on/off ratio increased from $\sim 5,000$ for devices without ALD to $\sim 10^6$ for devices with ALD. We attribute this increase in on/off ratio to the ALD passivation. It is known that the adsorbed oxygen molecules and hydroxyl/water groups on the surface can form electron traps. The electrons in the traps in the vicinity of the CNTs can provide negative gating effect biasing the CNTs toward the on state, thus leading to higher off-state current in the I_{ds} - V_{gs} measurements [38, 39, 47]. Regarding the devices with ALD coating, the deposited ALD layer can keep nanotubes passivated from oxygen molecules and moisture in the air, thus leading to low off-state current and high on/off ratio.

However, CMOS electronics prefer separate p-type and n-type

behavior transistors instead of ambipolar behavior transistors. The simple ALD Al_2O_3 passivation approach presented above is not sufficient and further developments are needed to convert the FESA CNT devices into n-type behavior. Channel doping techniques have been investigated a lot as an n-type conversion approach for CNT FETs. But the traditional organic dopants often bring poor stability and fabrication compatibility issues, which limit the application range of doping techniques [33, 37]. Here we utilize a 1 nm Al layer to assist the Al_2O_3 ALD passivation layer and get the n-type behavior CNT transistors. The electrical performance of the long channel device (channel length = 10 μm) after Al doping and ALD is shown in Fig. 3(d). Unipolar n-type FESA CNT FET was successfully achieved with hysteresis-free behavior ($\delta V < 0.5 \text{ V}$). The device showed an n-branch on-current density $\sim 2 \mu\text{A}/\mu\text{m}$ and on/off ratio $> 2 \times 10^6$. This method also offers the benefit of long-term stability in air. The electrical performance of the same device almost kept the same even after being exposed in ambient condition for 3 months (Fig. S2 in the ESM). The evaporated thin Al layer oxidized in air and served as a seeding layer between FESA CNT surface and ALD Al_2O_3 layer. The formed native AlO_x can introduce more positive fixed charges at the nanotube/ALD interface [30, 45, 46]. These positive charges would generate electrical fields and bend the nanotube energy band downward. In long channel devices (channel length $\gg$ nanotube length), tube-tube junctions affect charge transport mostly and conduction is in fact a percolation process. Charge transport would be determined by the conduction that can surpass the average tube-tube junction barrier height to provide a connected path. Under the Al layer and ALD Al_2O_3 treatment, the bulk of the nanotubes in the long-channel FETs were converted to n-type, enabling the FETs to show n-type transistor behavior. But the situation becomes different when it comes to short channel devices (channel length $<$ nanotube length). Figure 3(e) shows the I_{ds} - V_{gs} curves in linear scale and logarithm scale for FESA CNT FET with channel length equals 100 nm. It has a p-branch on-state current density $\sim 420 \mu\text{A}/\mu\text{m}$. The device shows ambipolar behavior with a stronger n-branch on-state current density $\sim 2 \mu\text{A}/\mu\text{m}$. In the short channel regime, tube-tube junctions hardly exist in the channel area and the metal/nanotube junctions dominate the charge transport. Carriers overcome the metal/nanotube

contacts and transport in the nanotube directly. Palladium (Pd) has a large work function, and usually the Fermi level aligns with the valence band of nanotubes, which results in larger Schottky barriers for electrons even when nanotubes are passivated. Therefore, hole conduction is still much stronger than electron conduction, which lets the devices exhibit larger p-type current than n-type current. I_{ds} - V_{gs} curves of typical FESA CNT FETs with various channel lengths (from 100 nm to 10 μm) after Al layer evaporation and Al_2O_3 passivation at the same V_{ds} are presented Fig. S3 in the ESM, which show the device changed from almost ambipolar to predominant n-type behavior. The increased surface scattering in longer channel devices lead to less steep subthreshold transition than shorter-channel devices [48, 49].

As channel length scaled down to less than nanotube length, the devices approach contact-dominated transport regime and Al layer + ALD Al_2O_3 method is not sufficient to convert short channel FESA CNT FETs to n-type transistors. Alternatively, metal contact engineering has the possibility to obtain n-type conduction from the nanotubes [23, 33]. Low-work-function metals would allow the Fermi level of the metal contacts to align with the conduction band of carbon nanotubes and lead to large Schottky barriers for holes but ohmic contacts for electrons. However, this technique nevertheless has some drawbacks. For example, low-work-function metals such as Gd or Sc are very susceptible to air and moisture and can be easily oxidized, which gives rise to high resistance and leads to the degraded output current. Therefore, it is of great importance to develop a durable metal contact engineering technique to convert FESA CNT FETs to n-type behavior. Figure 4(a) depicts the schematic diagram of n-type conversion techniques of FESA CNT short channel FETs. Back-gated FESA CNT FETs with 30 nm Titanium (Ti, with a work function of 4.3 eV) as source/drain metal contacts were fabricated firstly. Figure 4(b) presents the transfer characteristics for a typical back-gated FET (channel length = 100 nm) measured at $V_{ds} = 1$ V. The device still shows p-type behavior with a relatively small on-state current density $\sim 1 \mu\text{A}/\mu\text{m}$ and on/off ratio $\sim 10,000$. The transistor polarity of CNT FETs with short channel devices

(channel length < nanotube length), is dominated by the work function of source/drain metal contacts. Palladium has a large work function (5.3 eV), and usually the Fermi level aligns with the valence band of nanotubes, which results in strong hole conduction and leads to large p-type current. On the contrary, titanium forms low work function metal contacts (4.3 eV), and the Fermi level is far away from the nanotube valence band, which results in a large barrier for holes conduction and leads to smaller p-branch current. Nanotubes are heavily p-type due to the adsorption of oxygen molecules, so even the devices with Ti contacts exhibit p-type behavior in air rather than n-type behavior. To suppress the p-type conduction in devices, ALD Al_2O_3 passivation layer was deposited on top of the device as gate dielectric. Low temperature is a crucial factor because Ti is likely to get oxidized under elevated temperatures during the ALD process. A 1 nm/50 nm Ti/Au stack was then deposited by e-beam evaporation as the gate electrodes. The I_{ds} - V_{gs} transfer curves of the device after passivation are shown in Fig. 4(c). Interestingly, the figure indicates that the n-type conduction becomes predominant and the p-type conduction is suppressed. The device shows n-type on-state current density $\sim 50 \mu\text{A}/\mu\text{m}$, peak transconductance normalized by width $g_m \sim 20.1 \mu\text{S}/\mu\text{m}$, and on/off ratio $> 10^5$. After passivation, the Fermi level of FESA CNTs shifts towards conduction band because of desorption of oxygen, resulting in n-type behavior. We then further tried a 1 nm Al layer + ALD Al_2O_3 technique to improve the n-type performance. The I_{ds} - V_{gs} transfer curves are shown in Fig. 4(d) and the device shows an n-type on-state current $\sim 130 \mu\text{A}/\mu\text{m}$, peak transconductance normalized by width $g_m \sim 54.7 \mu\text{S}/\mu\text{m}$, with on/off ratio $> 2 \times 10^6$. The formed AlO_x at nanotube/ Al_2O_3 interface would bend the energy band downward, and together with the Ti contacts make the barrier for electrons much smaller than before, resulting in n-type behavior with decent performance. Figure S4 in the ESM shows I_{ds} - V_{gs} transfer curves for 10 n-type CNT FETs (channel length = 100 nm) without 1 nm Al layer (a) and with 1 nm Al layer (b). Using thinner dielectric layer with higher dielectric constant will improve the gate control and lead to higher subthreshold swing. We note that the p-type transistors showed

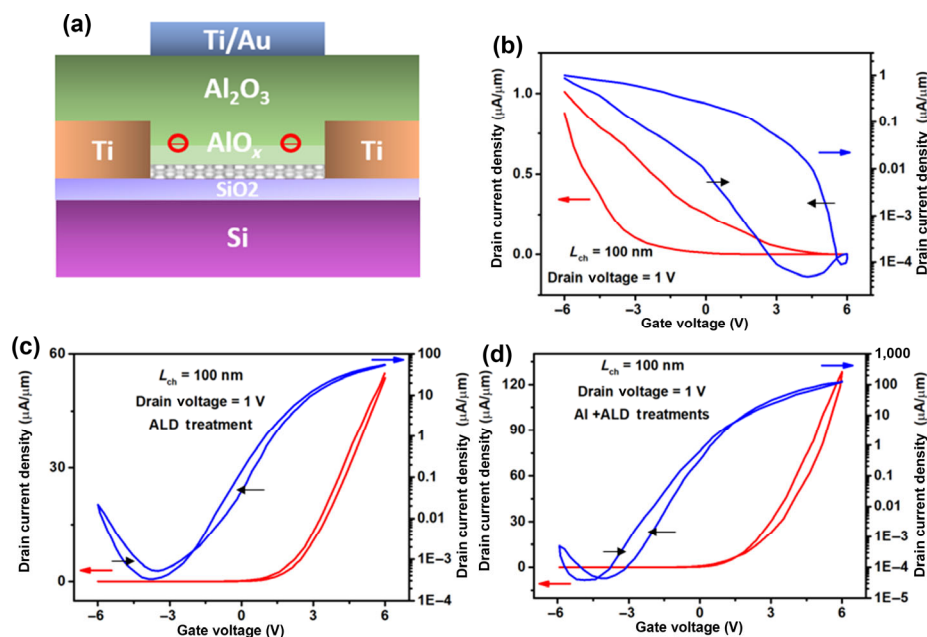


Figure 4 Electronic properties of CNT FETs with Ti source/drain contacts. (a) Schematic diagram of a top-gated CNT transistors with Ti source/drain contacts. (b) I_{ds} - V_{gs} curves of a typical short channel back-gated CNT transistors ($L_{ch} = 100$ nm) in both linear (red) and log (blue) scales. (c) I_{ds} - V_{gs} curves of the transistor in (b) after 40 nm Al_2O_3 ALD passivation. (d) I_{ds} - V_{gs} curves of a typical short channel CNT FET ($L_{ch} = 100$ nm) after 1 nm Al layer evaporation/oxidation and 40 nm Al_2O_3 ALD passivation.

more Schottky behavior than the n-type transistors, while n-type transistors showed smaller current density than the p-type devices. For nanotubes with diameters < 2 nm, it was observed that Schottky barriers at the Pd contacts are small but cannot be completely eliminated as the bandgap of single-wall nanotubes is inversely proportional to the diameter [6]. The diameter of our carbon nanotube arrays is ~ 1.5 nm, and hence a small Schottky barrier is expected. Further engineering of the metal contacts by using different metals or by annealing may lead to elimination of Schottky barriers for p-type transistors. On the other hand, electron transport in our n-type devices may be affected by scattering due to the fixed oxide charges, resulting in lower current density. We also note that our long-channel devices show Ohmic behavior while the short-channel transistors show slight Schottky behavior. The reason is that for long-channel devices, the transport is dominated by scattering/hopping of carriers in the channel instead of contacts, and thus the slight Schottky behavior of contacts has become unnoticeable in the I_{ds} - V_{ds} curves.

Furthermore, an integrated CMOS inverter was demonstrated with the as-made p-type and n-type FESA CNT FETs (channel length = 100 nm). FETs with Ti source/drain contacts are selected and followed by 1 nm Al layer evaporation and 80 °C Al_2O_3 ALD to achieve the n-type behavior transistors. The p-type transistors are the CNT FETs with Pd source/drain contacts after ALD passivation treatment. The channel widths of the p-type behavior FET and n-type behavior FET are designed to obtain similar drain current ($W_p = 2$ μm , $W_n = 7$ μm). The output characteristics of CNT-based CMOS inverter are shown in Fig. 5(b). The inverter works with $V_{ds} = 1$ V, and the input voltage is swept from -2 to 2 V. The output voltage switched from 1 to 0 V and results in a maximum gain of 5, suggesting the successful operation of FESA CNT inverter. We note that the input voltage of the inverter had wider range than the output voltage because the 40 nm ALD dielectric we used required higher voltage to turn and turn off the transistors. In the future, we can use thinner dielectric layer to improve the gate control and get the inverter with symmetric input and output and rail-to-rail operation.

3 Conclusions

Our work presents the significant advance in the fabrication of n-type densely aligned FESA CNT FETs and the application of FESA CNTs in CMOS logic circuits. We systematically studied the effects of ALD passivation and metal contact engineering on devices with various channel lengths. For long channel (channel length $\gg$ nanotube length) devices, a thin Al layer followed by oxidation and subsequent ALD passivation are sufficient for the carrier type conversion and resulted in n-type behavior. We then revealed further that for FESA CNT FETs (with ALD passivation) with short channel devices (channel length $<$ nanotube length), the transistor polarity is dominated

by the work function of source/drain metal contacts. Air-stable n-type behavior CNT FETs can be achieved using the Ti contacts and ALD passivation method and showed high on-state current density ~ 130 $\mu A/\mu m$ with on/off ratio of $> 10^6$. Moreover, a CMOS inverter has been demonstrated using as-obtained p-type and n-type FESA CNT FETs. These findings help the understanding of the device physics and would benefit future high-performance air-stable CNT FETs. Our achievements may open a door to future large-scale and energy-efficient CNT based CMOS computing units.

4 Methods

4.1 Isolation and alignment of semiconducting carbon nanotubes

Semiconducting carbon nanotube inks isolated using polyfluorene derivative polymer wrapper poly[(9,9-dioctylfluorenyl-2,7-diyl)-alt-co-(6,6'-[2,2'-bipyridine])] (PFO-BPy) are prepared according to published procedures [44]. Briefly, a 1:1 mass ratio of arc-discharge carbon nanotube soot (Sigma-Aldrich, #698695) and PFO-BPy (American Dye Source, Inc., Quebec, Canada; #ADS153-UV) are combined at a concentration of 2 mg/mL in toluene. The polymer and nanotube solution are sonicated using a horn-tip ultrasonicator (Fisher Scientific, Waltham, MA; Sonic Dismembrator 500) at 40% amplitude for 10 min. After sonication, the dispersion is centrifuged, and the supernatant is retained. The supernatants are concentrated and filtered through a 5 μm filter. The filtered solution is then centrifuged for 18–24 h. After centrifugation, the pellets are retained and dispersed using horn-tip ultrasonication in fresh toluene. These centrifugation and sonication steps are repeated to remove excess PFO-BPy in solution until the nanotube: PFO-BPy ratio is approximately 1:1. The resulting high semiconducting purity ($> 99.98\%$) carbon nanotube (typical diameter ~ 1.5 nm, typical length ~ 500 nm) pellets are dispersed at a concentration of 30 $\mu g/mL$ in ethanol stabilized chloroform (Fisher Scientific, #C606SK-1) and the nanotube inks are aligned using the previously developed FESA process [24, 25].

4.2 Postdeposition treatment of the CNT arrays

The CNT arrays were boiled in toluene at 120 °C for 1 h to remove excess PFO-BPy. Upon completion, CNT arrays were annealed in vacuum at a base pressure of 10^{-5} Torr and temperature of 400 °C for 1 h.

4.3 Fabrication and measurement of CNT devices

Aligned carbon nanotube arrays were used as the channel material. Alignment markers were patterned followed by identifying the aligned CNT regions with SEM. The CNTs outside the device channel regions were etched away by oxygen plasma. Source and drain metal contacts (30 nm thickness of palladium for p-type

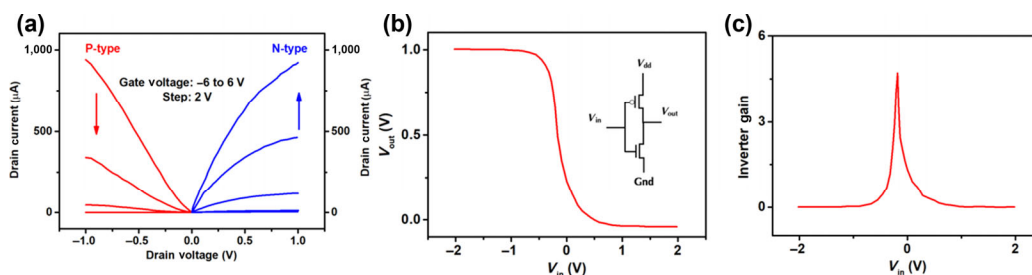


Figure 5 CMOS inverter circuit using the as-made p-type and n-type CNT FETs. (a) I_{ds} - V_{ds} curves of a p-type behavior CNT FET (Al_2O_3 treatments, Pd source/drain metal contacts, $L_{ch} = 100$ nm) and an n-type behavior CNT FET (Al + Al_2O_3 treatments, Ti source/drain metal contacts, $L_{ch} = 100$ nm). (b) Voltage transfer characteristics of the CMOS inverter based on aligned CNT array. (c) Plot of inverter gain versus input voltage.

transistor/30 nm thickness of titanium for n-type transistors) were then patterned. Sequentially, a 1 nm aluminum layer was evaporated onto the channel region and oxidized in air at 120 °C. Next, 40 nm thickness of Al₂O₃ was deposited as gate dielectric via ALD. Finally, a 1 nm/50 nm Ti/Au stack was utilized as the top gate electrode. During the fabrication process, poly(methyl methacrylate) (PMMA) layers were spin-coated onto the Si/SiO₂ surface, and then electron beam lithography was used to define the interested region on the wafer. All metal stacks were deposited at 10⁻⁷ Torr using an e-beam evaporator. The electronic properties were measured using a Keithley 4200-SCS semiconductor characterization system.

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Electronic Supplementary Material: Supplementary material (extracted carrier mobility for CNT FET (S1); air-stable performance of CNT FET (S2); length scaling behavior of CNT FETs after Al evaporation and Al₂O₃ passivation (S3); I_{ds} - V_{gs} transfer curves at V_{ds} = 1V for 10 CNT FETs without 1 nm Al layer and with 1 nm Al layer (S4); I_{ds} - V_{gs} transfer curves of CNT FETs with 1 nm Al evaporation (S5)) is available in the online version of this article at <https://doi.org/10.1007/s12274-021-3567-9>.

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