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Deep-subthreshold Schottky barrier IGZO TFT for ultra low-power applications

Abhijeet Barua[a,*], Kevin D. Leedy[b], Rashmi Jha[a]

[a] Department of Electrical Engineering and Computer Science, University of Cincinnati, Cincinnati 45221, OH, USA
[b] Air Force Research Laboratory, Sensors Directorate, Wright-Patterson AFB, Dayton 45433, OH, USA

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ABSTRACT

This study reports the deep subthreshold characteristics (≤1 V) of low thermal budget Indium Gallium Zinc Oxide (IGZO) thin film transistors (TFTs) with Schottky barrier source/drain contacts. The Schottky barrier was analyzed and a consistent ideality factor was observed across the devices. A deep subthreshold region was extracted from the nominal characteristics and barrier influence was observed in the low voltage region. This operation led to high output impedance (~$10^{12}\Omega$) and excellent trans-conductance leading to a high voltage gain (>100) due to hard saturation of the output characteristics. Positive bias stress and stability tests were conducted within this region that showed minimal drift in the transfer characteristics. Such characteristics make these devices an excellent choice for low-power deep subthreshold and weak signal applications.

1. Introduction

Amorphous oxide semiconductor (AOS) materials such as Indium Gallium Zinc Oxide (IGZO) have been reported to demonstrate increased mobility, low process complexity, improved uniformity and stability in threshold voltage, and reduced leakage due to the wide bandgap [1–5]. Due to these characteristics, IGZO thin film transistor (TFT) devices can provide high drive currents that make them a lucrative choice for driver circuities in displays applications. Recently, these devices have also caught significant attention for various types of sensor circuities. For sensor circuitries, low-power operation, noise immunity, device stability, and high sensitivity become important criteria [6–11]. In fact, it has been reported that the IGZO TFT can provide maximum sensitivity in biomolecule detection when used as sensors operating in the subthreshold regime [12].

These requirements have recently instigated significant interests in understanding the deep subthreshold operation of IGZO TFT with Schottky source/drain (S/D) contacts. The use of Schottky S/D regions facilitate deep subthreshold operation due to the two reverse-biased Schottky diodes that modulate the current injection or extraction and shield the channel from deleterious contact effects. Additionally, this regime enables operation at ultra-low power levels with below unity switching voltages and almost infinite output resistance such that the intrinsic gain is high [13–15]. The low-voltage operation is important for various applications. For example, in biosensors, this would allow devices to remain within the electrochemical window (<1–2 V) of the analyte solution, prevent the local work function change of the electrodes, and enable stable bias stress operation to sample the analyte at regular intervals [16]. In spite of such promising potential, there is limited work on designing IGZO TFT for low-power deep subthreshold operation and understanding their characteristics. This study reports the deep subthreshold behavior of IGZO TFT with Schottky S/D contacts via metal/semiconductor contact engineering and sheds some light on the device physics.

* Corresponding author.
E-mail address: baruaat@mail.uc.edu (A. Barua).

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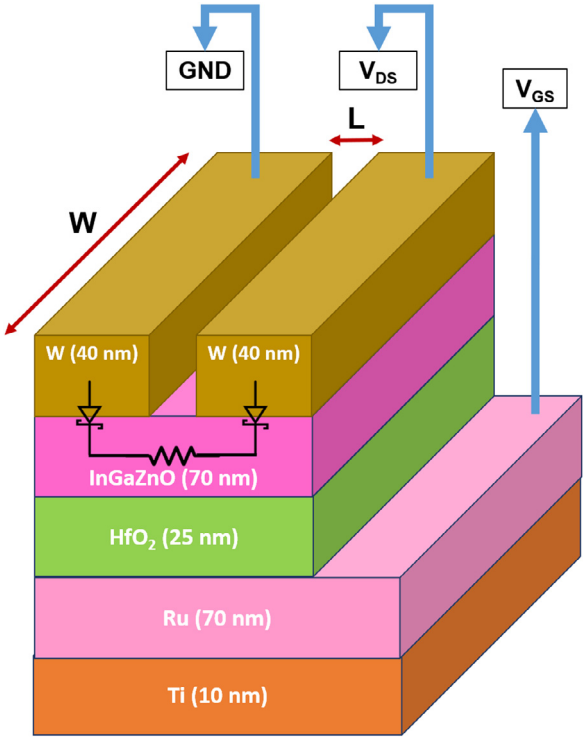

Fig. 1. Thin film transistor schematic with bias setup and Schottky configuration.

2. Experiment

Fig. 1 shows the bottom gate, inverted staggered architecture that was used for fabrication of IGZO TFTs on a 4-inch *p*-Si/SiO_2 wafer substrate. 10 nm Ti adhesion promoter and 70 nm Ru were deposited in situ without any vacuum break at room temperature (RT) through radio frequency (RF) magnetron sputter deposition in an Ar environment at a flow rate of 12 sccm, a process pressure of 5.44 to 5.47 mTorr, and RF power of 100 W to form the bottom gate. For achieving a high gate capacitance to enable the accumulation of a higher charge density in the channel at lower voltages while suppressing gate leakage current, HfO_2 high-k gate dielectric was chosen [17]. High-*k* amorphous HfO_2 film with short-range order was deposited in a Cambridge Nanotech Fiji F200 atomic layer deposition (ALD) system at 250 °C. Tetrakis(dimethylamido)hafnium (IV) was used as the hafnium source and a remote radio frequency O_2 plasma at 300 W was used as the oxygen source yielding a growth rate of 1 Å/cycle. Ar was used as a precursor carrier gas and plasma purge gas. Amorphous IGZO films were deposited in a Neocera Pioneer 180 pulsed laser deposition (PLD) system with a KrF excimer laser (Lambda Physik COMPex Pro 110, $\lambda = 248$ nm, 10 ns pulse duration), laser energy density of 2.6 J/cm^2, laser repetition rate of 30 Hz, deposition temperature of 25 °C, oxygen partial pressure of 25 mTorr, and substrate-to-target distance of 9.5 cm. The target was a 50 mm diameter by 6 mm thick sintered ceramic disk of In_2O_3:Ga_2O_3:ZnO with a 1:1:5 molar ratio.

To achieve Schottky S/D contacts on IGZO channel, we determined from ideal band offsets that among various metals, W on IGZO provides a theoretical barrier height of 0.34 eV which is above the Ohmic contact ceiling. Therefore, W can serve as a good candidate for this application without the need to alter and adjust channel deposition conditions. Additionally, W is easy to etch on IGZO with high etch-selectivity using commercially available TFW etchant from Transene company. Therefore, 40 nm W was deposited through RF magnetron sputter deposition at RT under a process pressure of 3.01 mTorr and RF power of 50 W to form Schottky metal contacts. Active regions with channel lengths of 10/20/50/100 µm and two common channel widths of 100/150 µm were patterned with a positive etch mask in an EVG 620 Mask Aligner. No post fabrication anneal was performed on the wafer such that virgin characteristics were preserved and the maximum process temperature used was only in ALD. The device regions were cleaved for further electrical characterization through a Keithley 4200A Semiconductor Characterization System (SCS) with a Cascade Microtech MPS150 Probe Station at room temperature (RT) of 298.15 K under ambient environment, and a Lakeshore Cryotronics PS-100 Cryogenic Probe Station with TTPX Model 336 Controller, under vacuum environment.

3. Results and discussion

3.1. Schottky behavior

Fig. 2(a) shows the drain source current (I_{DS}) under air ambient conditions for W/*L* = 150 µm/10 µm devices, when a drain source voltage (V_{DS}) was swept across the source/drain/channel without any gate bias (V_{GS} = 0 V). The zero-bias barrier height at the metal-semiconductor junction was extracted through a general reverse bias method from the diode equation below:

$$I_{DS} = \left(SA^{*}T^{2}e^{\left(-q\phi_{Bn}/kT\right)} \right) e^{V_{DS}/nkT} \quad (1)$$

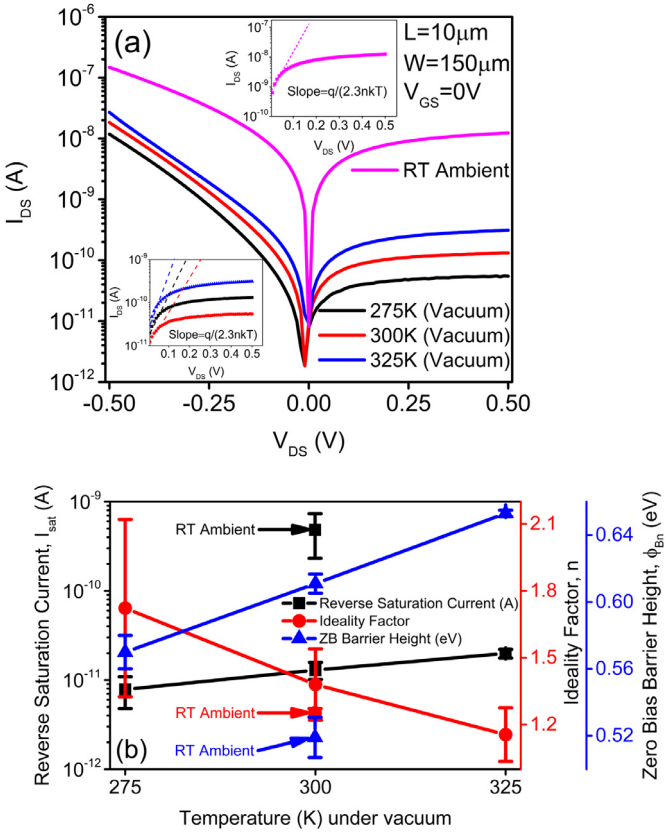

Fig. 2. (a) Average initial Schottky IV characteristic of 4 identical devices sized 10 × 150 μm^2 across fabricated wafer under room temperature ambient and under vacuum with temperature dependency at 3 different temperatures. (Insets) Forward sweeps for extraction of Schottky contact parameters under air ambient and under vacuum at different temperatures. (b) Average temperature dependent trends of reverse saturation current (I_{sat}), zero bias barrier height (Φ_{Bn}), and ideality factor (n) in vacuum.

Where the extrapolated reverse bias source drain current at zero source drain bias (V_{DS} = 0 V) was 4.826 × 10^{-10} A, S is the effective area of the diode, A^* ~ 41 Acm^{-2} K^{-2} is the Richardson's constant for an effective mass of IGZO determined from m_e^*/m_e ~ 0.34, T is the room temperature in K, q is electronic charge in C, ϕ_{Bn} is the zero-bias barrier height in eV, and k is Boltzmann's constant. Under air ambient conditions, the devices uniformly demonstrated an average ideality factor between 1.22 and 1.28 which indicated a non-ideal diode, and the barrier height extracted from the measurements were between 0.5 and 0.533 eV. This implied that the measured barrier heights were comparatively higher than the theoretical calculated value of 0.34 eV possibly due to a chemical reaction at the W/IGZO interface leading to the formation of an interfacial layer (IL). This IL seems to work in favor of providing a higher barrier height, leading to a better Schottky S/D contact.

Next, to observe the stability of this barrier, measurements were carried out at different temperatures under vacuum conditions. Interestingly, the same devices consistently exhibited a lower conductance compared to air ambient behavior at RT (Fig. 2(a)). This is possibly because under air ambient conditions, the presence of moisture in the environment can lead to the surface adsorption of H_2O molecules on the IGZO channel, which may act like a donor-like surface state, and lead to the formation of a surface accumulation region with increased conductivity. A slight asymmetry between positive and negative sweeps was observed which was not expected. This could possibly be due to slight differences in barrier height in the two back-to-back Schottky diodes under bias. At any instant, one Schottky diode is forward biased whereas the other one is reverse biased. At the biased terminal, the image charge barrier lowering due to carriers that approach the metal-semiconductor interface cause an effective barrier height reduction and higher conduction than the grounded terminal where the conduction may be limited by Schottky barrier injection. A well-behaved S/D diode performance was observed under various temperatures without any significant dispersion in reverse saturation current which attests to the excellent W/IGZO interface. From Fig. 2(b), one can observe that the measured barrier height increased with temperature from 0.57 eV at 275 K to 0.653 eV at 325 K though reverse saturation current increased. The increase of reverse saturation current with temperature was due to higher thermal generation of carriers. The diodes approach ideality with temperature with an average of 1.16 at 325 K.

Another requirement for Schottky barrier formation is a higher lattice compensation of the inherent oxygen vacancies (V_0^{2+}) in the IGZO channel such that the effective carrier density predominantly formed by such V_0^{2+} is reduced. High quality PLD deposition of IGZO and ALD HfO_2 deposition with reduced interface state density takes care of this criteria in our work. The oxygen partial pressure ($P_O/(P_O+P_{Ar})$) relative to Ar was fixed around 25mTorr for IGZO deposition and there was no adjustment of this parameter to change the intrinsic carrier density in the channel. IGZO channel had clear accumulation and depletion regions in capacitance-voltage (CV) characteristics with extremely low hysteresis that indicated low density of border traps (Fig. 3). A channel carrier density of 8.63 × 10^{17}cm^{-3} was extracted from $1/C^2$ data compared to the average density of 3.82 × 10^{17}cm^{-3} determined from turn-on voltages of the TFTs. The dielectric constant of HfO_2 was extracted to be 23.06 from the accumulation region of CV measurements using a physical thickness of dielectric to be 25 nm. The interface state density (D_{it}) between HfO_2 and IGZO interface was extracted to be 3.72 × 10^{12}cm^{-2}eV^{-1} using subthreshold

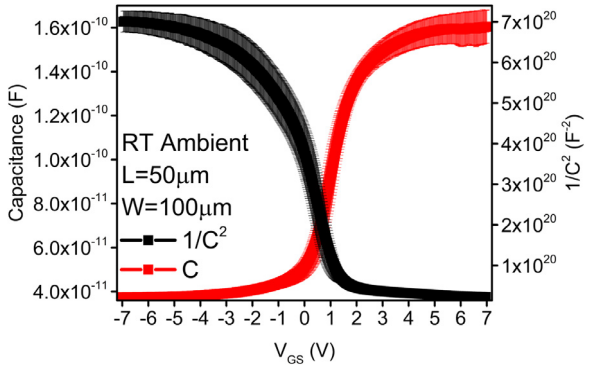

Fig. 3. 2 terminal MOS Capacitance and $1/C^2$ versus gate voltage (V_{GS}) at 3 MHz across 5 identical TFTs sized 50 × 100 µm^2 with clear accumulation and depletion regions.

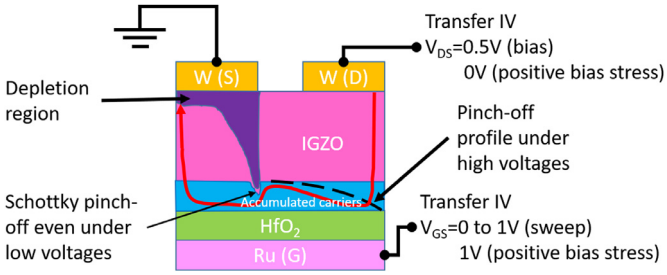

Fig. 4. Schematic to show the difference between conventional TFT pinch-off regime and Schottky depletion transport.

slope (SS) measurement technique as shown in Eq. (2).

$$D_{it} = \frac{C_{ox}}{q}\left[\frac{SSlog(e)}{kT/q} - 1\right] \tag{2}$$

HfO_2 has also been recorded to have a low standard enthalpy of formation and its thermodynamic stability is improved further by the amorphous layer of IGZO that imparted a smoother IGZO/HfO_2 interface [18]. We believe that low deposition temperature of HfO_2 and amorphous nature of IGZO led to a well-behaved interface as evident from the low interfacial state density and preservation of the dielectric constant. The above further implies that the lattice mismatch between HfO_2 and IGZO is limited to a minimal in our devices.

3.2. Deep subthreshold switching

Next, we studied deep-subthreshold switching characteristics. One should note that unlike conventional IGZO TFTs, Schottky S/D IGZO devices have significantly different and complex depletion-width and carrier profile, as shown in Fig. 4. Lee et al. defined a current range of 10^{-12} to 10^{-9}A as the ultralow power deep subthreshold regime bordering the device off state ($\leq 10^{-12}$A) [13]. This region was determined for 5 devices with W/L = 100 µm/50 µm dimensions (Fig. 5(a)). The devices exhibited consistent transfer characteristics across the wafer with an average subthreshold slope (SS) of 0.295 V/dec and the lowest SS of 0.227 V/dec with low threshold voltages (V_{TH}) between 2.12 and 2.86 V extracted in the linear region at low V_{DS} as shown in Fig. 5(b). In this study, the deep subthreshold regime limits were defined in the drain current region between 10^{-11} and 10^{-9}A which determined the gate voltage ranges required to restrain device operation within this region (V_{ref} and V_{high}). The average output characteristics of the 5 devices are presented in Fig. 5(c) where the gate voltage is incremented between V_{ref} and V_{high} and demonstrates that in W/IGZO Schottky contact TFTs, the saturation region is almost singular and independent of the drain bias, and the transition boundary is defined around V_{DS} = 0.5 V before which the transport gradually dominates from a drain side Schottky limited conduction to a source side limited one. The conductance within the V_{ref} to V_{high} zone is increasingly limited by the reverse saturation current of the source Schottky diode whose space charge region width is modulated by the gate bias and dictates the thermionic field emission transport, due to which at low V_{GS} (=V_{ref}~0.43 V as extracted in Fig. 5(a)), the I_{DS} encounters a hard saturation and is virtually flat with no curvature that allows a high output resistance (r_0) with no dependence on the drain voltage beyond V_{tran} (Fig. 5(d)). The hard saturation is further proved by the transfer curves at two different V_{DS} of 0.5 V and 1 V (Fig. 5(d) inset) chosen beyond V_{tran} that show convergence around the same V_{GS}~0.43 V and follow identical trends afterward within the unity gate voltage region. In MOSFETs, this saturation occurs due to channel pinch-off via high drain bias, however, in Schottky TFTs, the hard saturation occurs earlier and even at very low drain bias due to the depletion region formed by the reverse biased source region that almost impinges upon the gate dielectric (Fig. 4). Average transconductance across the devices shows a linear trend within the deep subthreshold zone with the lowest value (g_m~3.775 × 10^{-11}S) at V_{GS}=V_{ref} used to calculate the intrinsic signal gain of the TFT at the start of the deep subthreshold region (Fig. 6). At V_{GS}=V_{ref}, the highest output resistance observed across the different deep subthreshold states of the devices was 5.67 × 10^{12} Ω with an average of 1.83 × 10^{12} Ω, and the highest intrinsic gain factor calculated from the product (A_i=g_m/g_{ds} where g_{ds}=1/r_0 is the output conductance given by g_{ds}=$\delta I_{DS}/\delta V_{DS}$) was 124.5 and an average gain of 69 [19]. At the least, this is a magnitude higher than Ohmic contact TFTs which consistently exhibit gain factors much below 100 at such low voltage operation [13–15].

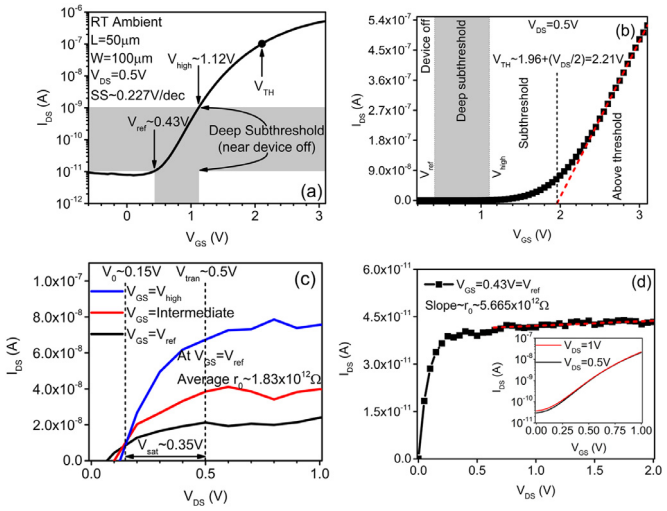

Fig. 5. (a) Representative transfer IV characteristic in air ambient for extraction of the deep subthreshold region below nA current range. (b) Depiction of the deep subthreshold region just before device off region and far below the extracted threshold voltage (extrapolation in the linear region). (c) Average output characteristics at low V_{DS} and three different gate voltages: $V_{GS}=V_{ref}$, intermediate V_{GS}, and $V_{GS}=V_{high}$, extracted from (a), where V_{sat}, V_{tran}, and V_0 are defined as shown. (d) Extraction of the output resistance from the representative output IV characteristic when $V_{GS}=V_{ref}$. (Inset) Transfer characteristic at $V_{DS}=0.5$ V and $V_{DS}=1$ V.

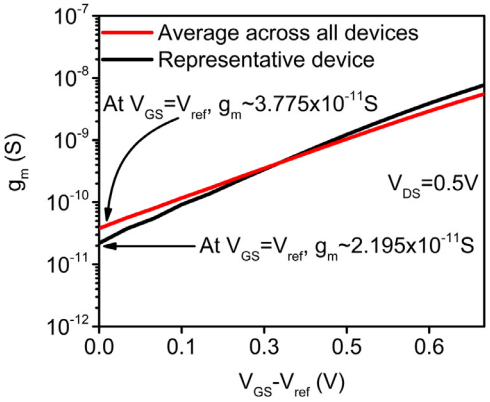

Fig. 6. Variation of the transconductance as a function of the gate voltage across the voltage range defined by V_{ref} and V_{high} extracted from Fig. 5(a).

3.3. Positive bias stress and stability

To operate this device in deep subthreshold region, let us define a gate voltage V_{ST} such that when $V_{GS}=V_{ST}$, the device operates in the deep subthreshold regime with a deep subthreshold slope (DSS) associated with it. This voltage on the gate clearly distinguishes the off-state of the device from the deep subthreshold region on-state. In this work, V_{ST} is determined through linear extrapolation of the transfer IV in the deep subthreshold region when the I_{DS} changes by one order of magnitude. A critical question lies in understanding how stable V_{ST} is under bias stress conditions over time in this region. To study this, positive bias stress (PBS) measurements were performed as the gate voltage (V_{GS}) was swept from 0 to 1 V at low drain voltage ($V_{DS}=0.5$ V) from 0 to 1000 s in intervals of 200 s. A bias stress of $V_{GS}=1$ V was sustained on gate with no bias on the drain while source was grounded during these measurements. We anticipate $V_{GS}=1$ V to be the highest stress voltage in the proposed deep subthreshold regime of the device operation. Fig. 7(a) shows I_{DS} vs. V_{GS} after every 200 s stress and Fig. 7(b) shows the extraction of V_{ST} using linear extrapolation technique in deep subthreshold region. Shift in V_{ST} towards right can be observed in these plots though negligible change in DSS was evident. To quantify this shift, drift in V_{ST} (ΔV_{ST}) with respect to V_{ST} under no stress is plotted over time in Fig. 7(c) where the trend saturates over time. The difference in V_{ST} between two consecutive transfer IV sweeps after intervals of 200 s is shown in Fig. 7(d) where initially a relative larger drift of 0.0192 V can be observed between two subsequent stress periods which saturated over time approaching negligible drift between subsequent stresses towards 1000 s.

To understand the impact of V_{ST} drift on I_{DS}, Fig. 8(a) shows the evolution of I_{DS} under bias stress over time. A total normalized change of 0.25% in I_{DS} was observed after 1000 s. To understand if this change still provides a good on:off margin, off-state and on-state I_{DS} with stress was measured over 1000 s and plotted in Fig. 8(b). Clearly, a 53.72% change in on:off ratio is evident in the first 30 s, mostly due to drift in the on-state I_{DS} due to V_{ST} drift with PBS. However after the initial 200 s, a stable change of 41.9% is maintained between on:off state which establishes the merit in using these devices for subthreshold operations. The drift in V_{ST} can possibly occur due to the presence of donor type interface traps at IGZO/HfO_2 interface as shown in Fig. 8(c). Initially, traps are empty in off-state of device due to depletion of electrons in the channel. However, on application of V_{GS}, the device turns-on and channel becomes rich in electrons leading to the trapping of some electrons in the interface states at IGZO/HfO_2. This leads to the gradual positive shift in the transfer curves with stress times. Due to small V_{GS} only border traps are filled over stress time leading to the saturation of ΔV_{ST} shown in Fig. 7(c) and 7(d). The negligible change in DSS and saturation of ΔV_{ST} over time indicates that no additional traps are created over time which is an

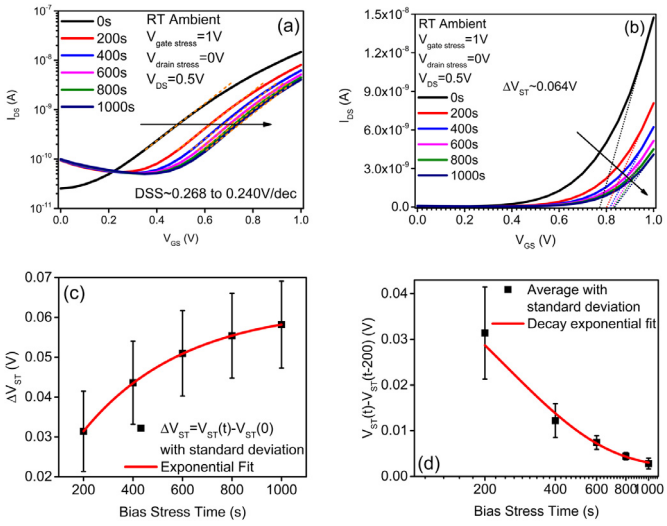

Fig. 7. (a) Semilog representation of deep subthreshold transfer IV in air ambient to show current limited within the nA range and similar slope profile (DSS) with negligible variation across 5 identical TFTs sized 50 × 100 μm^2. (b) Representative transfer IV characteristic for extraction of proposed V_{ST} in the nA current range. (c) Exponential variation of $\Delta V_{ST}(t)$ with bias stress time derived from (b) with similar upper and lower bounds. (d) Negative exponential dependency of $V_{ST}(t)$-$V_{ST}(t\text{-}200\ s)$ with time to show convergence to an offset value with an increase in stress time.

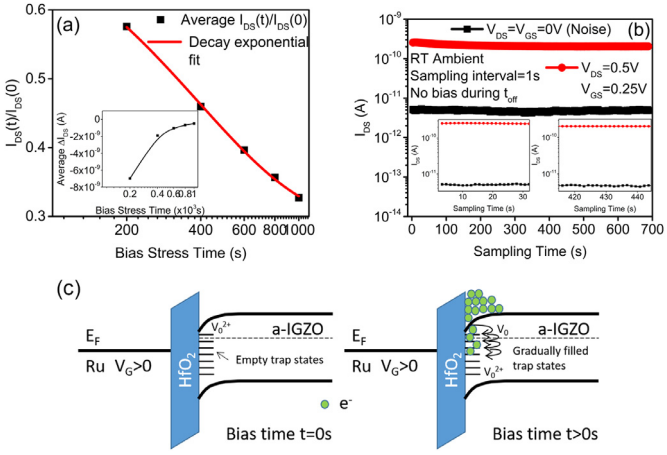

Fig. 8. (a) Normalized drain current as a purely decay exponential function of stress time. (Inset) Inherent drift current that approaches negligible drift after ~ 800 s. (b) Average short-term stability with a flat profile and saturation of the current in the below nA range after initial convergence within the first few seconds of sampling time, as well as uniform noise floor profile, when sampled with DC biases on both gate and drain. (Insets) Zoomed in profile in the initial seconds where the highly stable channel current ~ 259pA settles to ~ 205pA afterwards. (c) Band representation of PBS in the low-voltage regime.

encouraging result in this operational regime of devices. This drift is much smaller because of deep subthreshold operation compared to reported above-threshold IGZO devices which have non-saturating ΔV_T [20]. The drift in ΔV_{ST} was modeled by fitting into the Eq. (3) as:

$$\Delta V_{ST} = \Delta V_{ST\infty}\left(1 - e^{-t/\tau}\right) \tag{3}$$

Where $\Delta V_{ST\infty}$ is the ΔV_{ST} at infinite time and $\tau=\tau_0 e^{(Eb/kT)}$ is the thermally activated characteristic trapping time of the carriers and can be obtained from the fit. τ_0 is the thermal prefactor for thermionic emission over the barrier, and the thermal activation energy is $E_a=E_b\beta$ where E_b is the effective energy barrier. At values beyond 1000 s, the infinite time drift $\Delta V_{ST\infty}$ increases to a maximum of 0.0582 V and τ is approximately 0.408 ms. With this low trapping time, the traps fill up quickly and allow the rest of the carriers to freely take part in channel transport. The normalized drop in $I_{DS}(t)$ also follows a decay exponential trend given by Eq. (4):

$$\frac{I_{DS}(t)}{I_{DS}(0)} = e^{-t/\tau} \tag{4}$$

The equation was fitted as shown in Fig. 8(a) with the parameters extracted from (3) above and it can be seen from the inset of Fig. 8(a) where $\Delta I_{DS}=\Delta I_{DS}(t+200)$-$\Delta I_{DS}(t)$ that the drift current does approach zero with time and after certain time t_C (~800 s) is small enough to be neglected. Indeed, it can be seen that at no voltage ($V_{DS}=V_{GS}=0$ V) and very low voltage (V_{DS}=0.5 V, V_{GS}=0.25 V), the stability behavior of drain current against time, sampled at certain intervals, initially decays and then settles to a certain flat profile afterwards (Fig. 8(b)). For the first few seconds, the drift behavior of the devices is manifest in a higher ~259 pA current that reaches an inflection point and then settles to ~205 pA after certain time when the voltage drift has also settled, thus stable for the rest of the measurement window. This corroborates the hypothesis that there were limited number of interface traps that were quickly filled to saturation with

Table 1
Comparison of fabrication conditions and characteristics of Schottky barrier IGZO TFTs.

Parameters	[13]	[15]	This work
Gate dielectric	350 nm SiO_x/SiN_x, PECVD	100 nm, SiO_2, RF Sputter	25 nm HfO_2, ALD at 250 °C
Channel deposition	50 nm, RF Sputter, annealed at 250 °C/450 °C	20 nm, RF sputter, annealed at 300 °C	70 nm, PLD at 25 °C
Adjustment of deposition conditions	Yes, P_{Ox} varied in IGZO	Yes, P_{Ox} varied in Pt	No
S/D metal contacts	Mo, Ohmic	Pt, Ohmic	W, Schottky
Fabrication flow	Complex, etch stop layer and passivation layer, wet etch /RIE/dry etch process	Shadow mask, wet etch process	Simple, facile, wet etch process
Post fabrication anneal	Yes, 450 °C	No	No
Zero bias barrier height (eV)	0.165	0.74	0.5 to 0.533
W/L (μm/μm)	50/20	2000/60	100/50
n	1.7	~1.6	1.28
V_T (V)	~1.6	11.7	2.12
SS (V/dec)	0.28	–	0.227
g_m (S)	9×10^{-12}	–	3.775×10^{-11}
r_0 (Ω)	5×10^{13}	–	5.67×10^{12}
Intrinsic gain	450 at V_{GS}=0 V	29,000 at V_{GS}=20 V	124.5 at V_{GS}=0.43 V
PBS study	No	No	Yes
Stable I_{DS}	~100pA	–	205pA
Interface state density ($cm^{-2}eV^{-1}$)	4.7×10^{12}	–	3.72×10^{12}
Deep subthreshold regime (V)	0.5 to 2	~0 to 4V	0.43 to 1.12

time and nil or negligible traps were created with stress bias of the devices. The noise floor of the device is limited to the pA region and the voltages for the stability characteristics were chosen such that the electric fields between gate/source and drain/gate were equal and opposite to nullify each other (E_{GS}=E_{DG}=26.32 MV/cm). The characteristics of devices reported in this work are compared with other published data in this area in Table 1. Clearly, the devices reported in this work offer very promising characteristics in several categories for low-voltage operation with opportunity for further improvement in gain.

4. Conclusion

In summary, the TFTs in this study were realized through a simple and facile Schottky metal/channel combination of W and PLD IGZO using a low-thermal budget process. These devices demonstrated excellent deep subthreshold characteristics with a high input impedance and high gain of above 100 when operated in the deep subthreshold regime with operating voltages below 1 V. It was observed that this regime can form the basis of another novel low voltage measurement region for sensor applications due to its robustness, limited voltage drift and high stability especially with respect to measurement times. The novel deep subthreshold voltage drift shown in this region along with extremely small drift currents will allow highly sensitive measurements. Such observations establish these TFTs as promising candidates for operation in the below subthreshold regime and can be another design paradigm for heavily power constrained applications.

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Declaration of Competing Interest

The authors declare no conflict of interest.

CRediT authorship contribution statement

Abhijeet Barua: Conceptualization, Methodology, Validation, Formal analysis, Investigation, Data curation, Writing - original draft, Writing - review & editing, Visualization. **Kevin D. Leedy:** Resources, Writing - original draft, Writing - review & editing, Supervision. **Rashmi Jha:** Conceptualization, Methodology, Validation, Resources, Data curation, Writing - original draft, Writing - review & editing, Visualization, Supervision, Project administration, Funding acquisition.

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