Applied Physics Letters ARTICLE scitation.org/journal/apl

# On the characteristics of N-polar GaN Schottky barrier contacts with LPCVD SiN interlayers

Cite as: Appl. Phys. Lett. **118**, 122103 (2021); doi: 10.1063/5.0039888
Submitted: 7 December 2020 · Accepted: 11 March 2021 ·
Published Online: 23 March 2021

View Online Export Citation CrossMark

Dolar Khachariya,[1] Dennis Szymanski,[2] M. Hayden Breckenridge,[2] Pramod Reddy,[3] Erhard Kohn,[2] Zlatko Sitar,[2,3] Ramón Collazo,[2] and Spyridon Pavlidis[1,a)]

## AFFILIATIONS

[1]Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, North Carolina 27695-7911, USA
[2]Department of Materials Science and Engineering, North Carolina State University, Raleigh, North Carolina 27695-7919, USA
[3]Adroit Materials, Inc., 2054 Kildaire Farm Rd., Cary, North Carolina 27518, USA

[a)]**Author to whom correspondence should be addressed:** spavlidis@ncsu.edu

## ABSTRACT

We study the behavior of N-polar GaN Schottky diodes with low-pressure chemical vapor deposited (LPCVD) SiN interlayers and unveil the important role of an amphoteric miniband formed in this interlayer due to a previously identified and dominating Si dangling bond defect. Through analysis of temperature-dependent current–voltage ($I$–$V$–$T$), capacitance–voltage ($C$–$V$), and x-ray photoelectron spectroscopy measurements, we observe that when nickel is deposited on LPCVD SiN pretreated with hydrofluoric acid, the SiN/GaN interface is responsible for determining the overall system's barrier height. By contrast, contact formation on oxidized LPCVD SiN leads to a metal/SiN-dominant barrier. We, consequently, propose band diagrams that account for an amphoteric miniband in LPCVD SiN, leading to a new understanding of LPCVD SiN as a lossy dielectric with surface barrier-dependent behavior.

*Published under license by AIP Publishing.* https://doi.org/10.1063/5.0039888

Schottky contacts to N-polar GaN have been widely considered a challenging technical building block due to the material's polar orientation and a rather reactive surface. On N-polar GaN, the inverse (positive) polarization surface charge ($\sigma_p$) with respect to the Ga-polar surface yields a lower Schottky barrier height, leading to higher leakage currents and lower breakdown strength.[1–7] In addition, the N-polar GaN surface reacts readily with many chemicals used in standard fabrication processes.[6,8–11] It is thus difficult to form reliable Schottky barrier contacts for diodes and field-effect transistor (FET) gates.

A possible solution to overcome these challenges is to insert a thin dielectric interlayer between the metal contact and N-polar GaN, making it a dielectric-assisted Schottky barrier system.[12] The most commonly used passivation dielectric in GaN technology is silicon nitride (SiN).[13–22] SiN interlayers have also been implemented in gate contacts of N-polar GaN FETs.[23–26] Recent studies have examined the SiN/N-polar GaN interface and proposed associated energy band diagrams.[27–29] In these studies, SiN films ranging in thickness from 5 to 30 nm have been deposited on N-polar GaN via *in situ* metalorganic chemical vapor deposition (MOCVD), and the resulting structure has been analyzed as a metal–insulator–semiconductor capacitor (MIS-CAP). The SiN is often assumed to behave as a charge-containing insulator, with few details provided regarding the DC conductance of SiN, especially when very thin films have been used, or the barrier height at the metal/SiN interface.

SiN employed in this study has been deposited via low-pressure chemical vapor deposition (LPCVD) at 725 °C, which is within the temperature range to obtain a near stoichiometric or slightly Si-rich SiN amorphous layer.[30–32] Slightly Si-rich LPCVD contains a Si dangling bond-related defect center (≡Si) within the upper half of the bandgap, which is amphoteric in nature and may become the dominating defect.[12,33] This characteristic is often exploited as a charge storage layer in Si memory device technologies.[34–37] When deposited on N-polar GaN, the negative counter charge can be placed within the SiN interlayer; a band diagram including bulk charge states for this system has been previously drawn.[12,38] This leads to the formation of a defect miniband within the SiN, grossly aligned with the conduction band edge of GaN.[12] Thus, the system represents a tri-layer one, containing barriers between the metal/SiN and SiN/N-polar GaN as well as a trap-determined dielectric in between. A first-order model was proposed in our recent work, primarily focusing on the Ga-polar case and only briefly on the N-polar case.[12] It is worth noting that miniband conduction has also been reported in a tri-layer GaAs metal–insulator–semiconductor (MIS) diode system consisting of Al metal and an insulating layer of low temperature (LT) GaAs on $n^+$ GaAs.[39]


Published under license by AIP Publishing

Here, we provide a detailed analysis of the interlayer-modified Schottky system consisting of metal/SiN/N-polar GaN and focus on the electrical behavior of LPCVD SiN in this system. To identify the interlayer behavior clearly, a thickness of 7 nm of LPCVD SiN was chosen, which is beyond that of a pure tunneling barrier, making it akin to an MIS system. In addition, we have accounted for the chemical termination of the SiN surface, which may result in a highly oxidized state.[40,41] Our measurements show that the LPCVD SiN film does not behave as a charge-containing insulator and that the previously identified amphoteric miniband must be included. We thus propose a modified band structure compared to previous studies that captures the properties of the specific LPCVD constellation employed.

N-polar GaN layers were grown on a c-plane sapphire substrate with a 4° offcut toward the m-plane using a vertical, cold-wall, radio frequency (RF) heated, low-pressure MOCVD system. A 0.6-$\mu$m-thick $n^+$-doped layer followed by a 2.6-$\mu$m-thick n-type layer were grown with carrier concentrations of $5.0 \times 10^{19}\,cm^{-3}$ and $3.5 \times 10^{17}\,cm^{-3}$, respectively. Both layers were unintentionally doped with oxygen.[42,43] Then, a 7-nm-thick SiN film was deposited using LPCVD at 725 °C and 320 mTorr with dichlorosilane and ammonia precursors. Before depositing SiN, an *in situ* cleaning step with ammonia was performed to remove native oxides.[12,38] The deposited SiN layer thickness was confirmed using reflectometry.

Device fabrication started with deposition of a large area Ohmic contact (V/Al/Ni/Au–30/100/70/70 nm) on top of the SiN surface using e-beam evaporation. The Ohmic contacts were annealed at 850 °C for 30 s in $N_2$ ambient.[12] It should be noted that the SiN is present during this short annealing step. However, the quality of the SiN is not affected as it was already deposited at high temperature. Measurements of the current between two Ohmic contacts in forward and reverse bias confirmed a linear relationship in both directions. This is in agreement with our previous results when forming large area Ohmic contacts on LPCVD SiN/Ga-polar GaN heterostructures.[12] Prior to the Schottky metal deposition (Ni, 250 nm) on the SiN surface, Sample A was cleaned with 10% hydrofluoric (HF) acid for 1 min, followed by a de-ionized (DI) water rinse, while Sample B was kept in an ambient environment. It is expected that HF cleaning removes several angstroms of oxidized SiN.[18,40] The experiment was designed to determine the influence of the surface termination on the electrical characteristics of the three-layer structure. Schottky diodes without SiN (Sample C) were also fabricated as control samples. The Schottky metal pattern was deposited using a metal shadow mask to avoid exposure of the N-polar GaN and SiN-coated diodes to photolithography developer.[6] Cross-sectional diagrams of the fabricated devices are shown in Fig. 1.

X-ray photoelectron spectroscopy (XPS) was used to determine the band offsets, Fermi level ($E_F$), and barrier height at the interface between the SiN and N-polar GaN. Both thick (150 nm) and thin (~3–4 nm) SiN films were deposited on two separate N-polar GaN samples (without subsequent metal deposition) to determine the parameters mentioned above. The procedure, experimental setup, and Au- and C-based charging correction during XPS data analysis are described elsewhere.[21,38]

The core level binding energies of Si 2p and Ga 3d at the interface were determined with respect to the interface Fermi level, as shown in Figs. 2(a) and 2(b), respectively. Employing the valence band and core level characterization in thick SiN films,[38] thick N-polar GaN films,[5]

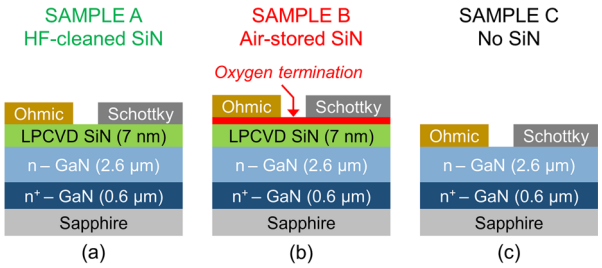


**FIG. 1.** Schematic cross sections of Schottky diodes on (a) HF-cleaned and (b) air-stored SiN interlayers as well as on (c) bare N-polar GaN. Not drawn to scale.

and the core level binding energies at the interface, we can determine the SiN/N-polar GaN valence band offset to be ~0 eV. Interestingly, the interface Fermi level is at 3 eV from the valence bands of GaN and SiN. Based on the doping in N-polar GaN, $n = 3.5 \times 10^{17}\,cm^{-3}$, the difference between the conduction band and Fermi level ($E_C - E_F^{bulk}$) in the bulk region would be less than 0.05 eV. Hence, the barrier height at the charge neutrality level, i.e., the energy difference between the interface Fermi level and conduction band of GaN, is 0.4 eV. Furthermore, since this energy level lineup coincides with the ≡Si defect level in slightly Si-rich SiN, it may be reasonable to assume that a defect miniband is formed in this case, determining the Fermi level throughout the SiN interlayer. A tentative energy band diagram at the SiN/N-polar GaN interface is created using these findings, as shown in Fig. 2(c). It shows a very low barrier system when SiN is deposited on N-polar GaN.

The N-polar GaN diodes were then electrically characterized to study the barrier at the metal/SiN interface and confirm whether the Fermi level in SiN is pinned due to the miniband. Temperature-dependent current–voltage (*I*–*V*–*T*) measurements were performed in

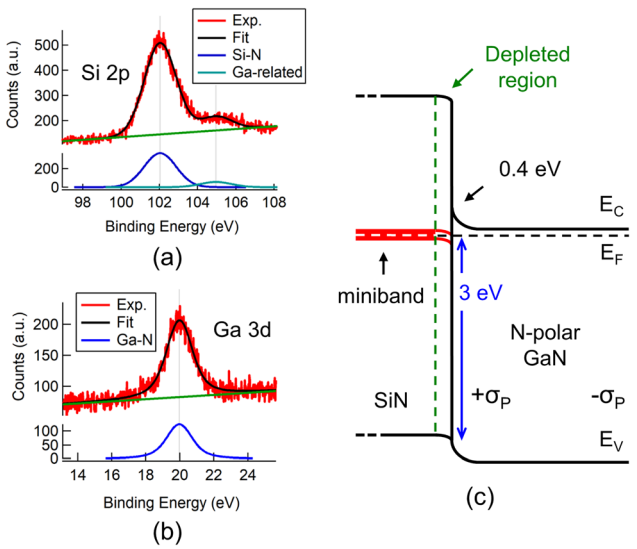


**FIG. 2.** XPS spectra of (a) Si core level (Si 2p) and (b) GaN core level (Ga 3d) peaks measured on SiN/N-polar GaN. (c) A tentative energy band diagram of SiN deposited on N-polar GaN without the metal/SiN interface. $\sigma_P$ denotes the polarization charge in N-polar GaN.


Published under license by AIP Publishing

a vacuum probe station (base pressure $\sim 1 \times 10^{-7}$ Torr) using a Keithley 4200 semiconductor parameter analyzer. Capacitance–voltage ($C$–$V$) measurements were conducted at 1 MHz using the parallel $R$–$C$ circuit mode.

The room temperature $I$–$V$ characteristics of all three diodes are shown in Figs. 3(a) and 3(b). The ideality factors ($n$) of Samples A and B are >1.6 and exhibit a slight voltage dependence. Their threshold voltages are $V_{th,A} \sim 0.6$ V and $V_{th,B} \sim 5.0$ V, respectively, as extracted from the linear representation. Sample C showed an $n_A \sim 1.07$, which represents near-ideal Schottky diode behavior, and $V_{th,C} \sim 0.4$ V. The $I$–$V$ barrier heights ($\phi_{B,IV}$) for all three samples are calculated by extracting the saturation current density ($J_0$) that is extrapolated from the exponential region of the forward bias $I$–$V$ measurements as a function of temperature up to 200 °C (not shown). The procedure is described elsewhere.[6,44] As shown in Fig. 3(c), $\phi_{B,IV}$ values in Samples A, B, and C are 0.4 eV, 1.1 eV, and 0.4 eV, respectively. It should be noted that $\phi_{B,IV}$ values for Samples A and B are apparent barrier heights due to the higher ideality factors (>1.6) of these diodes.

The $\phi_{B,IV}$ in Sample A is consistent with the XPS results, indicating that the barrier is determined by the SiN/N-polar GaN interface, with no or negligible barrier at the metal/SiN interface. Thus, the reason that $V_{th,A} \sim 0.6$ V is that the lossy SiN interlayer drops an additional 0.2 V across it with respect to Sample C. Under forward bias, charge is injected from GaN into the lossy SiN, which conducts through the defect miniband. I–V measurements show an observable temperature dependence (not shown) that confirms that defect-assisted tunneling is not the dominant conduction mode when 7-nm-thick LPCVD SiN is used. This is in contrast with our previous experiments[38] where 2–4 nm of LPCVD SiN were deposited on Ga-polar GaN. There, a weak temperature dependence was observed in forward bias, which is indicative of tunneling. Here, we note that more than one conduction mechanism may be involved. Due to the overall low barrier, the current through the diode reaches the metal series resistance level at very low voltages, so identifying the exact current mechanism through the SiN interlayer is complex and not attempted in this work.

The semilog $I$–$V$ of Sample B shows two distinct current regimes: one at lower voltages (<2 V) and another above it, before reaching the metal series resistance limit at around 8 V. The first regime is exponential, while the second regime is a current limiter; the linear $I$–$V$ reveals that this is a superlinear transition region at medium voltages. That $V_{th,B} \sim 5.0$ V is well above GaN's bandgap indicates a strong influence of the oxygen termination on the SiN surface. $I$–$V$–$T$ reveals a very high barrier height of ~1.1 eV for this case, which is extracted from the first exponential at lower voltages. From XPS, the barrier at SiN/N-polar GaN is 0.4 eV, so the measured $I$–$V$ barrier height in Sample B must be at the metal/SiN interface. Consequently, the current limiter could be related to the SiN interlayer, the barrier at the metal/SiN interface, or both, and the current transport mechanism could be one or many of the different mechanisms mentioned earlier. To summarize, $I$–$V$ measurements reveal a low barrier system in the HF-cleaned SiN MIS diodes, with a dominating barrier at the SiN/GaN interface, no barrier at metal/SiN interface, and neutral defect miniband in-between. In comparison, the air-stored SiN MIS diodes are characterized by a high barrier at the metal/SiN interface and high overall resistance, indicating that much of the SiN is depleted.

$C$–$V$ measurements were performed to support the $I$–$V$ findings and estimate the upper limit of the defect concentration, which forms the defect miniband in SiN. Figure 4 shows the $C$–$V$ barrier height ($\phi_{B,CV}$) extracted from $1/C^2 - V$ for all three cases, and the top-right corner of the graph shows the modified equivalent circuit of the $C$–$V$ measurements. Although the C–V barrier height equation consists of the intercept voltage, (kT/q), and the energy difference between the conduction band and Fermi level, the sum of the total energy for those additional two terms is within 0.05 eV for the doping level of our N-polar GaN diodes. Thus, these additional terms do not significantly impact our estimate of the C–V barrier height.[6] It should be noted that the circuit shown here is not developed using impedance spectroscopy; it is a representation of the extended $R$–$C$ circuit by considering the two series components of $R$–$C$ from the SiN interlayer and GaN space charge layer. The reason for this additional SiN $R$–$C$ parallel element is that in reverse-bias, SiN becomes capacitive, while in forward-bias, it becomes conductive due to the conduction through the miniband. This is evidenced by the sudden drop in capacitance at distinct forward bias voltages corresponding to the onset of charge injection.[45]

All three diodes appear linear in the $1/C^2$–$V$ plots measured at 1 MHz, as shown in Fig. 4. The $\phi_{B,CV}$ values for Samples A, B, and C

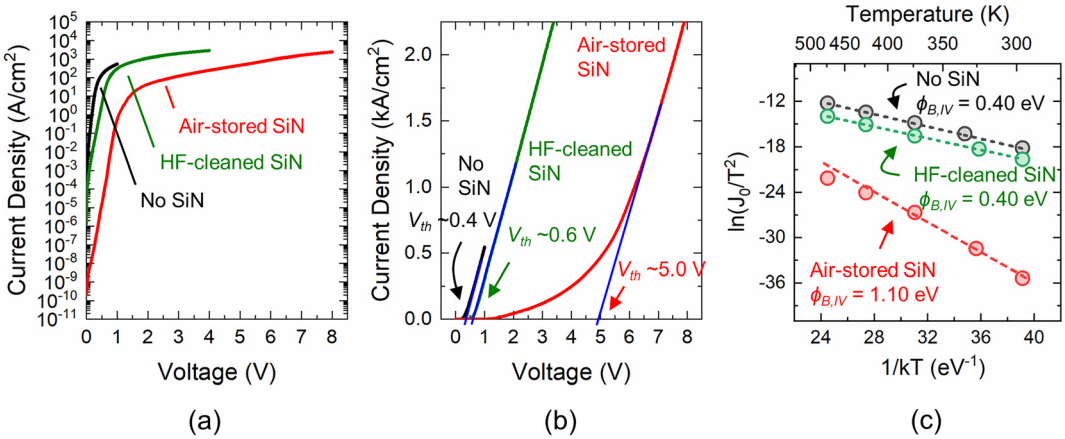


**FIG. 3.** Room temperature forward bias $I$–$V$ characteristics in the (a) semilog-scale and (b) linear-scale for the fabricated Schottky diodes with different surfaces. (c) $I$–$V$ barrier height extraction using [ln($J_0$/$T2$) vs 1/$kT$] generated from temperature-dependent $I$–$V$ characteristics.


Published under license by AIP Publishing

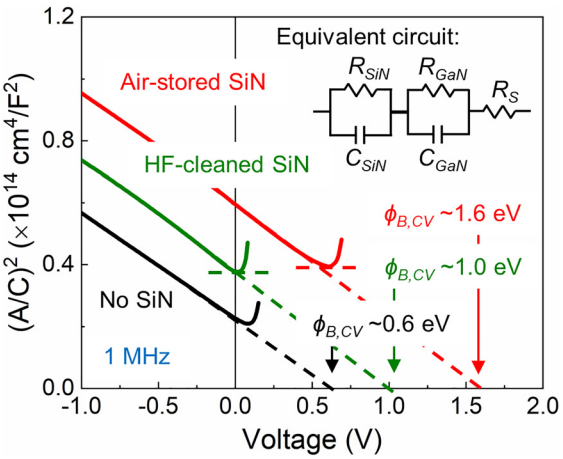


**FIG. 4.** *C–V* barrier height extraction for without SiN, HF-cleaned, and air-stored SiN surface Schottky diodes. The top-right corner of the graph shows the equivalent circuit of the diode for the *C–V* measurements.

are ~1.0 eV, ~1.6 eV, and ~0.6 eV, respectively. The net doping concentration is extracted for all three cases using the slope of the $1/C^2$–$V$ curve and is found to be around $3.5 \times 10^{17}$ cm$^{-3}$, as expected. Thus, the modulated capacitance in all three diodes is of the SiN/N-polar GaN junction, and no additional modulation of a metal/SiN junction capacitance is observed. Whereas $\phi_{B,IV}$ values of Samples A and C were found to be equivalent, the $\phi_{B,CV}$ value of Sample A is now larger due to the additional capacitance presented by SiN in series with the GaN space charge layer capacitance in reverse bias. By calculating the difference in the $1/C$ values in Samples A and C, it is estimated that SiN has a thickness of 6.5 nm, which agrees with the reflectometry measurements.

The *C–V* behavior of Sample A suggests that the SiN acts as a capacitor in reverse bias up to zero bias. The *I–V* behavior of the same sample suggests that the SiN is neutral and acts as a resistor since there is no barrier at the metal/SiN interface. This is characteristic of a lossy dielectric that experiences dielectric relaxation (below 1 MHz) and it confirms that, in the case where an HF-cleaned SiN interlayer is used, there is no noticeable barrier between the top metal and SiN.

The $1/C^2$–$V$ characteristic of Sample B is shifted upwards as compared to Sample A, which results from a higher barrier at the metal/SiN surface and is consistent with the same sample's *I–V* behavior. It should be noted that the impedance bridge cannot balance anymore at approximately 0.6 V, which is the beginning of the transition region where the resistive behavior takes over. The large transition region in *I–V* [see Fig. 3(b)] shows that transport increases gradually, and there may be a mixture of the transport mechanisms mentioned earlier. This transition region appears exponentially increasing with a shallow slope in semilog *I–V*, whereas in linear *I–V*, it appears as a superlinear rise. Thus, the metal/SiN barrier dominates the overall barrier behavior, and this higher barrier is caused by the oxygen termination of the SiN interlayer in Sample B. Since capacitance modulation is not observed in SiN, it is concluded that the metal/SiN barrier results in complete depletion of the SiN interlayer. Using the *I–V*-extracted barrier of 1.1 eV, the upper limit in defect density within the miniband can be estimated. Considering that 2 to 2.5 nm SiN is already depleted at the SiN/GaN interface due to the countercharge of ~$10^{13}$ cm$^{-2}$ polarization charge of N-polar GaN, 1.1 eV needs to deplete the remaining 4.5 to 5 nm SiN. Therefore, the upper limit of the defect density is found to be around 2 to $5 \times 10^{19}$ cm$^{-3}$ in this LPCVD SiN.

Based on the above analysis, energy band diagrams for Samples A and B are proposed and schematically depicted in Figs. 5(a) and 5(b), respectively. HF treatment of the LPCVD SiN prior to metal deposition results in a system dominated by the SiN/GaN interface, whereas oxide formation on the SiN surface leads to a dominating barrier at the metal/SiN interface. Whereas previous depictions of SiN on GaN have assumed that SiN acts as a charge-containing insulator,[29] our results reveal that the picture may be more complex. Si dangling bonds in LPCVD SiN can lead to the formation of a defect miniband.[33] It was predicted that a trapped electron level (≡Si$^-$) and trapped hole level (≡Si$^0$) are separated by 0.4 eV.[33] Our analysis also

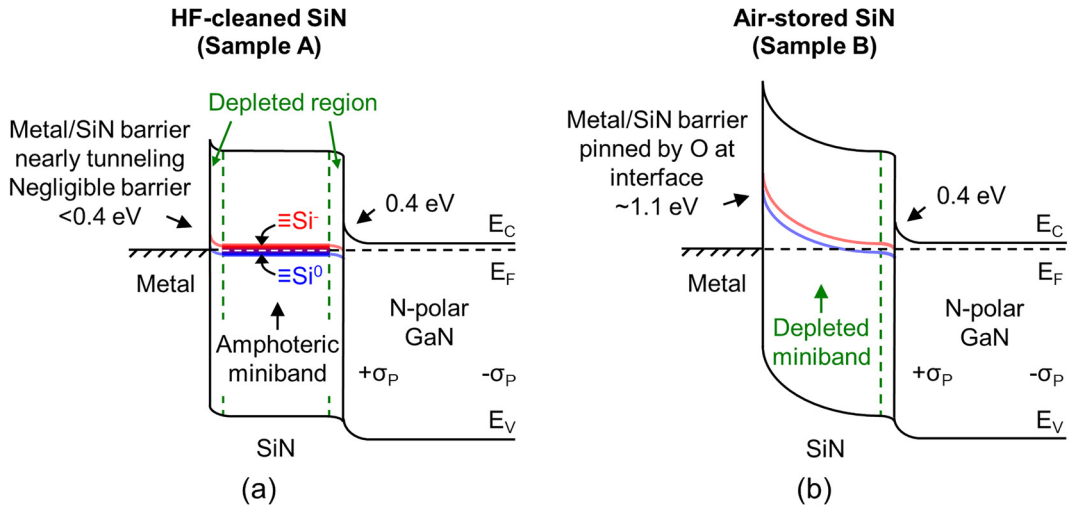


**FIG. 5.** Band structure alignment at equilibrium between metal, SiN, and N-polar GaN for (a) HF-cleaned and (b) air-stored SiN surface Schottky diodes. Not drawn to scale.


Published under license by AIP Publishing

shows evidence that the formed miniband is amphoteric, pointing to an overlap of the distribution of trapped charge states [depicted by the shaded regions in Fig. 5(a)]. Due to its shallow energy level, conduction can occur through the interlayer. Consequently, the amphoteric nature of the miniband is also responsible for the depletion of donors and acceptors at the metal/SiN and SiN/GaN junctions, respectively. This is key, since the presence of a unipolar miniband would lead to the formation of two back-to-back diodes. This would limit current flow until one of the two diodes would break down. Instead, we observe a behavior that is consistent with two series-connected diodes, where the potential across them adds up.

In summary, this work considers the defect- and surface-dependent properties of LPCVD SiN in determining the electrical behavior of Metal/SiN/N-polar GaN diodes. Based on XPS, *I–V–T*, and *C–V* measurements, band diagrams are proposed, which account for an amphoteric miniband formed in the LPCVD SiN, where both the donor and acceptor state distributions overlap. When metal is deposited on HF-treated SiN, the SiN/GaN interface is responsible for determining the system's barrier height, whereas the use of oxidized SiN leads to a metal/SiN-dominant barrier. Due to the amphoteric nature of the miniband configuration, the top and bottom barriers in this tri-layer system are not back-to-back biased but in series, which is a highly unusual configuration. SiN deposited on GaN has long been considered a charge-containing insulator in dielectric-assisted Schottky barrier systems, MIS-gate structures, and as a passivation layer. However, this picture may be oversimplified. The tri-layer system analyzed here contains a barrier-controlled lossy dielectric. Thus, rigorous analysis of SiN properties is important in determining its behavior on GaN and further quantitative studies are needed to optimize such structures in devices.

The authors gratefully acknowledge funding in part from NSF (Nos. ECCS-1610992, ECCS-1916800, and ECCS-1653383), AFOSR (Nos. FA-95501710225 and FA9550-1910114), DOE (No. DE-AR0000873), and the PowerAmerica Institute at North Carolina State University. This work was performed in part at the NCSU Nanofabrication Facility (NNF) and Analytical Instrumentation Facility (AIF), which are supported by the State of North Carolina and the National Science Foundation (Award No. ECCS-1542015). The NNF and AIF are members of the North Carolina Research Triangle Nanotechnology Network (RTNN), a site in the National Nanotechnology Coordinated Infrastructure (NNCI).

## DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

## REFERENCES

[1]U. Karrer, O. Ambacher, and M. Stutzmann, Appl. Phys. Lett. **77**, 2012 (2000).
[2]A. Rizzi and H. Lüth, Appl. Phys. Lett. **80**, 530 (2002).
[3]J. Osvald, J. Kuzmik, G. Konstantinidis, P. Lobotka, and A. Georgakilas, Microelectron. Eng. **81**, 181 (2005).
[4]B. P. Downey, D. J. Meyer, D. S. Katzer, D. F. Storm, and S. C. Binari, Solid-State Electron. **86**, 17 (2013).
[5]P. Reddy, I. Bryan, Z. Bryan, W. Guo, L. Hussey, R. Collazo, and Z. Sitar, J. Appl. Phys. **116**, 123701 (2014).
[6]D. Khachariya, D. Szymanski, R. Sengupta, P. Reddy, E. Kohn, Z. Sitar, R. Collazo, and S. Pavlidis, J. Appl. Phys. **128**, 064501 (2020).
[7]T. Suemitsu and I. Makabe, Phys. Status Solidi B **257**, 1900528 (2020).
[8]S. Rajan, A. Chini, M. H. Wong, J. S. Speck, and U. K. Mishra, J. Appl. Phys. **102**, 044501 (2007).
[9]M. H. Wong, Y. Pei, T. Palacios, L. Shen, A. Chakraborty, L. S. McCarthy, S. Keller, S. P. DenBaars, J. S. Speck, and U. K. Mishra, Appl. Phys. Lett. **91**, 232103 (2007).
[10]C. R. English, V. D. Wheeler, N. Y. Garces, N. Nepal, A. Nath, J. K. Hite, M. A. Mastro, and C. R. Eddy, J. Vac. Sci. Technol. B **32**, 03D106 (2014).
[11]D. Wei, T. Hossain, D. P. Briggs, and J. H. Edgar, ECS J. Solid State Sci. Technol. **3**, N127 (2014).
[12]P. Reddy, D. Khachariya, D. Szymanski, M. H. Breckenridge, B. Sarkar, S. Pavlidis, R. Collazo, Z. Sitar, and E. Kohn, Semicond. Sci. Technol. **35**, 055007 (2020).
[13]B. Luo, J. W. Johnson, J. Kim, R. M. Mehandru, F. Ren, B. P. Gila, A. H. Onstine, C. R. Abernathy, S. J. Pearton, A. G. Baca, R. D. Briggs, R. J. Shul, C. Monier, and J. Han, Appl. Phys. Lett. **80**, 1661 (2002).
[14]T. Hashizume, S. Ootomo, T. Inagaki, and H. Hasegawa, J. Vac. Sci. Technol. B **21**, 1828 (2003).
[15]D. Gregušová, R. Stoklas, K. Čičo, T. Lalinský, and P. Kordoš, Semicond. Sci. Technol. **22**, 947 (2007).
[16]N. Ramanan, B. Lee, C. Kirkpatrick, R. Suri, and V. Misra, Semicond. Sci. Technol. **28**, 074004 (2013).
[17]B. M. Green, K. K. Chu, E. M. Chumbes, J. A. Smart, J. R. Shealy, and L. F. Eastman, IEEE Electron Device Lett. **21**, 268 (2000).
[18]J. R. Shealy, T. R. Prunty, E. M. Chumbes, and B. K. Ridley, J. Cryst. Growth **250**, 7 (2003).
[19]A. Alexewicz, M. Alomari, D. Maier, H. Behmenburg, C. Giesen, M. Heuken, D. Pogany, E. Kohn, and G. Strasser, Solid-State Electron. **89**, 207 (2013).
[20]M. Hua, C. Liu, S. Yang, S. Liu, K. Fu, Z. Dong, Y. Cai, B. Zhang, and K. J. Chen, IEEE Trans. Electron Devices **62**, 3215 (2015).
[21]P. Reddy, S. Washiyama, W. Mecouch, L. H. Hernandez-Balderrama, F. Kaess, M. Hayden Breckenridge, B. Sarkar, B. B. Haidet, A. Franke, E. Kohn, R. Collazo, and Z. Sitar, J. Vac. Sci. Technol. A **36**, 061101 (2018).
[22]V. K. Surana, N. Bhardwaj, A. Rawat, Y. Yadav, S. Ganguly, and D. Saha, J. Appl. Phys. **126**, 115302 (2019).
[23]B. Romanczyk, S. Wienecke, M. Guidry, H. Li, E. Ahmadi, X. Zheng, S. Keller, and U. K. Mishra, IEEE Trans. Electron Devices **65**, 45 (2018).
[24]O. S. Koksaldi, J. Haller, H. Li, B. Romanczyk, M. Guidry, S. Wienecke, S. Keller, and U. K. Mishra, IEEE Electron Device Lett. **39**, 1014 (2018).
[25]S. Rajabi, S. Mandal, B. Ercan, H. Li, M. A. Laurent, S. Keller, and S. Chowdhury, IEEE Electron Device Lett. **40**, 885 (2019).
[26]X. Zheng, H. Li, M. Guidry, B. Romanczyk, E. Ahmadi, K. Hestroffer, S. Wienecke, S. Keller, and U. K. Mishra, IEEE Electron Device Lett. **39**, 409 (2018).
[27]I. Sayed, W. Liu, S. Chan, C. Gupta, M. Guidry, H. Li, S. Keller, and U. Mishra, Appl. Phys. Lett. **115**, 032103 (2019).
[28]I. Sayed, W. Liu, S. Chan, C. Gupta, H. Li, S. Keller, and U. K. Mishra, Appl. Phys. Express **12**, 121001 (2019).
[29]W. Liu, I. Sayed, C. Gupta, H. Li, S. Keller, and U. Mishra, Appl. Phys. Lett. **116**, 022104 (2020).
[30]K. E. Bean, P. S. Gleim, R. L. Yeakley, and W. R. Runyan, J. Electrochem. Soc. **114**, 733 (1967).
[31]R. S. Rosler, Solid-State Technol. **20**, 63 (1977).
[32]H. J. Stein, J. Appl. Phys. **57**, 2040 (1985).
[33]J. Robertson and M. J. Powell, Appl. Phys. Lett. **44**, 415 (1984).
[34]H. Wong, M. C. Poon, Y. Gao, and T. C. W. Kok, J. Electrochem. Soc. **148**, G275 (2001).
[35]S. Choi, H. Yang, M. Chang, S. Baek, H. Hwang, S. Jeon, J. Kim, and C. Kim, Appl. Phys. Lett. **86**, 251901 (2005).
[36]E. Vianello, L. Perniola, P. Blaise, G. Molas, J. P. Colonna, F. Driussi, P. Palestri, D. Esseni, L. Selmi, N. Rochat, C. Licitra, D. Lafond, R. Kies, G. Reimbold, B. De Salvo, and F. Boulanger, in 2009 IEEE International Electron Devices Meeting (IEDM) (2009), pp. 1–4.
[37]Y. Sun, H. Y. Yu, N. Singh, K. C. Leong, E. Gnani, G. Baccarani, G. Q. Lo, and D. L. Kwong, IEEE Trans. Electron Devices **58**, 1329 (2011).
[38]P. Reddy, S. Washiyama, F. Kaess, M. Hayden Breckenridge, L. H. Hernandez-Balderrama, B. B. Haidet, D. Alden, A. Franke, B. Sarkar, E. Kohn, R. Collazo, and Z. Sitar, J. Appl. Phys. **119**, 145702 (2016).


Published under license by AIP Publishing

[39]P. Arifin, T. L. Tansley, and E. M. Goldys, Solid-State Electron. **41**, 1075 (1997).
[40]S. I. Raider, R. Flitsch, J. A. Aboaf, and W. A. Pliskin, J. Electrochem. Soc. **123**, 560 (1976).
[41]H. Du, R. E. Tressler, and K. E. Spear, J. Electrochem. Soc. **136**, 3210 (1989).
[42]R. Collazo, S. Mita, A. Rice, R. F. Dalmau, and Z. Sitar, Appl. Phys. Lett. **91**, 212103 (2007).
[43]R. Kirste, R. Collazo, G. Callsen, M. R. Wagner, T. Kure, J. Sebastian Reparaz, S. Mita, J. Xie, A. Rice, J. Tweedie, Z. Sitar, and A. Hoffmann, J. Appl. Phys. **110**, 093503 (2011).
[44]P. Reddy, B. Sarkar, F. Kaess, M. Gerhold, E. Kohn, R. Collazo, and Z. Sitar, Appl. Phys. Lett. **110**, 011603 (2017).
[45]L. Stauffer, *Fundamentals of Semiconductor C-V Measurements* (Keithley Instruments, Inc., 2009), Vol. 4.


Published under license by AIP Publishing