A 200-GHz Power Amplifier With a Wideband Balanced Slot Power Combiner and 9.4-dBm P_{sat} in 65-nm CMOS: Embedded Power Amplification

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***Abstract*— The effect of gain and embedding of amplifying cells (amp-cell) on the output power of power amplifiers (PAs) at high mm-wave frequencies is studied. This is the frequency range where matching loss becomes comparable with the gain of the amp-cell in most silicon technologies. By deriving power equations of embedded amp-cell, power contours are plotted in the gain plane and an optimum embedding is designed to maximize the output power for a desired gain. To showcase the theory, a high-frequency, high-power amp-cell, called matched cascode, is introduced and subsequently embedded to boost both power gain and output power. To increase the output power even further, a differential slot power combiner (SPC) is introduced and its equivalent circuit is analyzed. Finally, using the embedded matched cascode cell, and the SPC, a 2 × 8 PA is implemented in 65-nm bulk CMOS. It consumes 732 mW from 2.4-V supply voltage, with a maximum power-added efficiency (PAE) of 1.03%. The PA features a P_{sat} and OP1dB of 9.4 and 6.3 dBm, respectively, at 200 GHz, and a maximum power gain of 19.5 dB.**

***Index Terms*— CMOS, embedded, high mm-wave, power combiner, P_{sat}.**

I. Introduction

ONE of the key factors in improving the range of a transceiver is increasing the power it radiates, which is directly impacted by the output power of its power amplifier (PA) [1]–[6]. Recently, achieving high maximum oscillation frequencies (f_{max}) in silicon processes has made them low-cost candidates for the implementation of transceivers at the high end of mm-waveband [7]–[12]. The trade-off between the output power and operation frequency, however, stays a major challenge to overcome in PAs operating at this frequency band [13]–[17].

As the operation frequency gets closer to $f_{max}/2$, the available gain from transistors starts to diminish to values comparable with the loss of the matching networks [18]–[27]. This, as elaborated in Section II, not only lessens the overall gain of the PA but also adversely affects the maximum output power of the PA with a practical gain. Low power gain, also, adds to the number of cascaded amplifying cells (amp-cells) needed to reach a desired gain, increasing dc power consumption. High-voltage topologies such as cascode and stacked amp-cells are traditionally used to increase the supply voltage by which the maximum output swing and hence the output power can be elevated. Nevertheless, conventional cascode amp-cells commonly suffer from large intra-cell parasitic capacitance and hence small gain at higher mm-wave frequencies [28]. Stacked amp-cells have even lower gain compared with cascode as the gate capacitors function as a negative voltage feedback and reduce the gain [29], [30].

Power combining techniques, which mostly fall into series and parallel categories, can be used to raise the output power. Nonetheless, the former suffers from imbalanced input impedances due to parasitic capacitors between the primary and secondary of the transformer and therefore the output power and gain drop [31]. The latter increases the impedance transformation ratio and the loss of the output matching network, and thus decreases the output power and gain [32].

In this article, the authors aim to maximize the output power of the PA while operating at high mm-wave frequencies. To this end, a strategy that combines system- and circuit-level optimization and design with passive power combining technique is proposed, to implement a 200-GHz PA in the 65-nm CMOS process. This strategy can be implemented in any other technology as well. In the system-level analysis, the effect of power gain on the output power of a PA at frequencies where the gain of amp-cells becomes comparable with the loss of matching networks is explained. It is illustrated that embedding boosts both gain and output power of a PA for minimum amplification. In the circuit-level design, the stable region of the gain plane in [33] is analyzed and power contours are demonstrated to find the optimum embedding that maximizes the output power for a given power gain. Then, a high-power, high-frequency amp-cell called matched cascode with an optimized embedding is introduced to maximize the output power for an acceptable power gain. Finally, a balanced and wideband slot power combiner (SPC) is introduced to boost the output power even further. Using the embedded matched cascode amp-cell and the SPC, a 2 × 8 embedded PA with an output saturated power, P_{sat}, of 9.4 dBm and gain of 19.5 dB is implemented at 200 GHz in a 65-nm CMOS technology.

The rest of this article is organized as follows. Section II explains the main challenges in achieving high P_{sat} at high frequencies, as well as the impact of gain on the output power

Manuscript received November 11, 2020; revised February 8, 2021, April 22, 2021, and June 10, 2021; accepted June 10, 2021. This article was approved by Associate Editor Kenichi Okada. This work was supported by the National Science Foundation (NSF). *(Corresponding author: Hadi Bameri.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/JSSC.2021.3091546.

Digital Object Identifier 10.1109/JSSC.2021.3091546

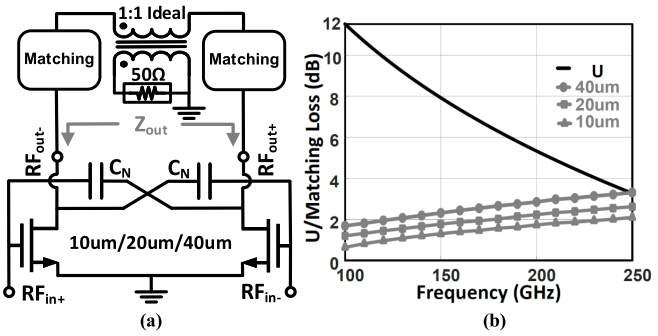


Fig. 1. Transistor/passive devices gain/loss versus frequency. (a) Circuit schematic of a neutralized differential CS amp-cell with three different transistor sizes. (b) Simulated unilateral power gain (U) of a 10-/20-/40-μm NMOS CS transistor and the losses of output matching network of the amp-cell shown in (a) to 50 Ω.

in a cascaded PA. The output power in embedded amplifiers is studied in Section III. A high-power, high-frequency, matched cascode amp-cell is introduced in Section IV. In Section V, the wideband, balanced SPC is discussed, and the simulation results are presented. Section VI explains the implementation of the PA and demonstrates the measurement results and comparison with state-of-the-art. Finally, Section VII concludes this article.

II. Impact of Limited Gain on the PA's Output Power at Near-$f_{\max}$ Frequencies

As frequency increases, the loss mechanisms in both active and passive devices start to dominate the performance of amplifiers. On one hand, in passives, the loss of metallic conductors increases proportional to the square root of frequency, due to the skin effect. Moreover, dielectric substrates become more lossy, as dielectric loss tangent increases proportional to frequency. These effects result in low-quality factor passives that adversely affect the matching networks' loss and hence the amplifier gain. On the other hand, internal losses of transistors diminish the maximum available power gain with frequency and cause the transistor to become a passive element beyond $f_{\max}$. These factors make the design of amplifiers challenging and in some cases impossible at near-$f_{\max}$ frequencies. In addition to the high-loss and low-gain challenges of small-signal amplifier design at these frequencies, PAs suffer from limited output power and low input–output impedances which increase the matching loss even further.

Fig. 1(a) shows an NMOS common-source (CS) differential amplifier neutralized by C_N capacitors. The output of the amplifier is matched to 50 Ω using an L-matching network for three different transistor sizes: 10, 20, and 40 μm in a 65-nm CMOS process. The quality factors of the inductor and capacitor of the L-matching network are selected to be 20 and 8, respectively, at all frequencies. Fig. 1(b) shows the matching loss versus frequency for the three transistor sizes, as well as unilateral power gain (U) of a 10-μm NMOS transistor. U of 20- and 40-μm NMOS transistors is assumed to be the same as 10-μm NMOS transistor, since the metal connections that are used to make 10-μm transistors in parallel to make

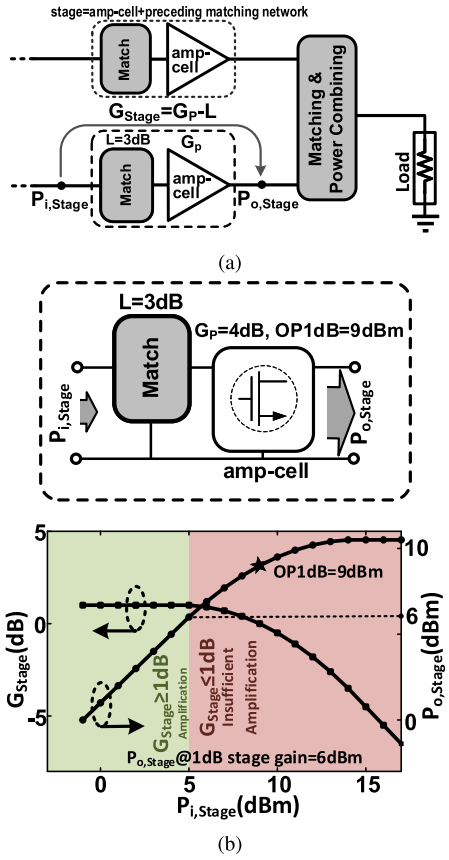


Fig. 2. Maximum output power of a cascaded PA with a minimum stage gain of 1 dB. (a) Block diagram of the last stage in a cascaded PA. (b) Simulated power performance of a high-power, low-gain amp-cell.

20- and 40-μm transistors are very short and low loss. As it can be seen, U falls below the matching loss at frequencies higher than 250 GHz for 40-μm transistor size, forcing the designer to reduce the transistor size or operation frequency. In reality, the quality factors of the matching network elements are not constant and drop with frequency, making it harder to design high-gain amplifiers with larger transistors at high frequencies. The rise in loss at high frequencies not only reduces the overall small-signal gain but also adversely affects output power of a PA. Since the available gain from amp-cells at high mm-wave frequency band is small, multiple amp-cells must be cascaded to achieve a reasonable gain. In cascaded PAs, the amp-cells close to the input, called the driver amp-cells, are meant to increase the small-signal gain. Every amp-cell added after the drivers has to deliver higher power to its load compared with its preceding amp-cell, while increasing the overall power gain of the PA. As shown in Fig. 2(a), each amp-cell needs its preceding matching network, and together they are called a stage (amp-cell + preceding matching network). Having the practical aspect of the PA in mind, we evaluate the highest output power of this stage at the point that the gain of the stage is compressed to the minimum gain of 1 dB. This ensures that the PA stage has an acceptable power gain when it is delivering its highest power. In other words, a PA stage with less than 1-dB gain is not useful even if it can deliver high output power. As shown in Fig. 2(b), since the small-signal power gain of the stage is

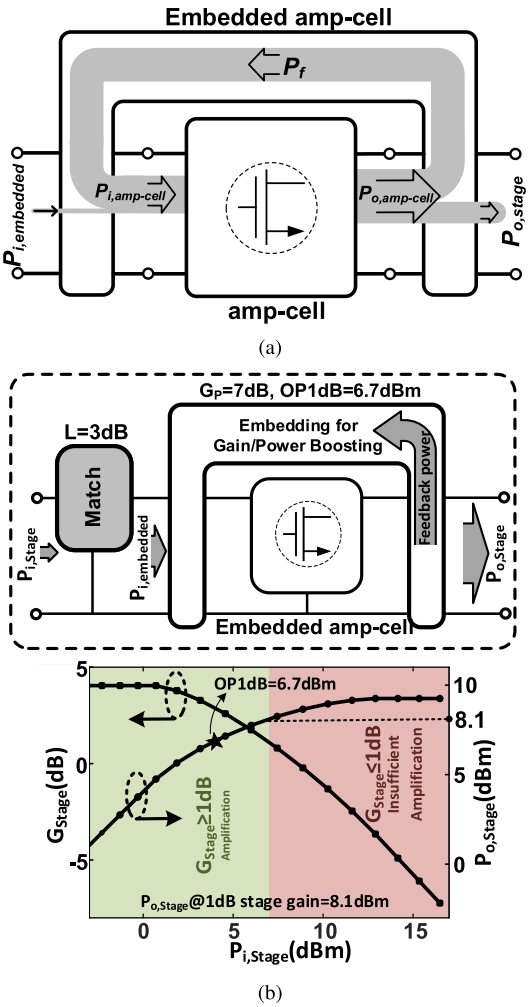


Fig. 3. Effect of gain boosting using embedding on the output power of a PA. (a) Power flow that results in boosting the power gain. (b) Performance of the cascaded PA after embedding the amp-cell of the last stage.

already 1 dB, no compression is acceptable, and therefore, the maximum output power of the stage is 6 dBm at the input power of $P_{i,\text{Stage}} = 5$ dBm, right before the compression in gain starts. Even though the amp-cell has 1-dB output compression point (OP1dB) of 9 dBm, and P_{sat} of 11 dBm, it only delivers 6 dBm at the 1-dB stage gain. This shows that low small-signal stage gain limits the maximum power that the amp-cell can deliver with an acceptable gain. The high power capability of the amp-cell, however, can be traded off to boost the small-signal power gain and extend the Amplification region (stage gain > 1 dB) to higher input powers. This results in higher output power at the 1-dB stage gain.

As shown in Fig. 3(a), a small fraction of the output power can be fed back to the input port of the amp-cell using an embedding network to boost the power gain. Using a numerical simulator (e.g., MATLAB), a constant fraction of the output power of the amp-cell is extracted and fed back to its input to emulate the operation of a lossless embedding. The feedback power is constructively added to the input power of the amp-cell to boost its power gain. This numerical simulation shows that although the embedding reduces OP1dB and P_{sat} of the embedded amp-cell to 6.7 and 9.05 dBm, respectively, it increases the small-signal power gain of the stage to 4 dB as shown in Fig. 3(b). The boost in the stage small-signal gain translates to 3-dB gain compression at 1-dB stage-gain. This extends the Amplification region to 7.1 dBm compared with 5 dBm of the non-embedded case and increases the output power of the stage from 6 to 8.1 dBm at the same 1-dB stage gain. Fig. 3(b) also shows that although OP1dB has dropped, the output power at the 1-dB stage gain is well above it. This analysis shows that embedding not only boosts the small-signal power gain of a PA but also improves the output power of the PA at a specific power gain.

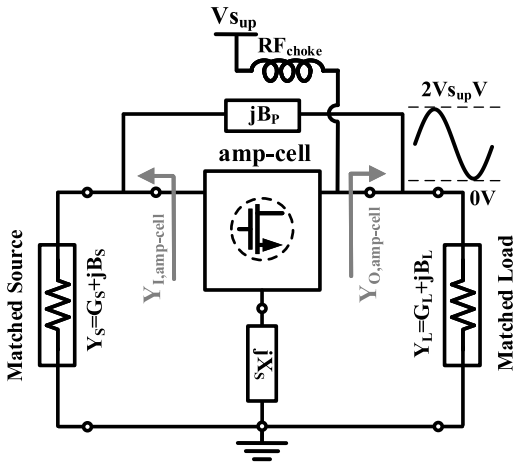


Fig. 4. Amp-cell embedded by T-embedding and supplied through an RF_{choke}.

III. Output Power in Embedded Amplifiers

Section II illustrated the effect of power gain on the output power of a PA by ideally subtracting some signal power from the output and adding it to the input port. In an actual circuit implementation, however, a passive network performs this feedback operation. As a result, not only the gain is boosted but also the power delivery capability of the stage is affected. This is because the feedback network directly influences the impedances that are seen by the amp-cell.

Since gain boosting is always performed using small-signal analysis, to find the relationship between the gain and output power of an embedded amp-cell and optimize them simultaneously, we must use its small-signal parameters to estimate the maximum linear output power. To this end, the setup shown in Fig. 4 is used where an amp-cell is embedded by T-embedding [33]. To conserve the hard-earned power gain, the embedded amp-cell is assumed to be conjugate matched to the source and load impedances. To simplify the power analysis, we assume that the output voltage of the amp-cell experiences clipping before its input voltage, and this clipping is the only nonlinear effect that causes gain compression. Hence, the maximum linear output power of the amp-cell shown in Fig. 4 can be estimated as

$$P_{o,\max} = 0.5V_{\text{Sup}}^2 \cdot G_{\text{L}} \tag{1}$$

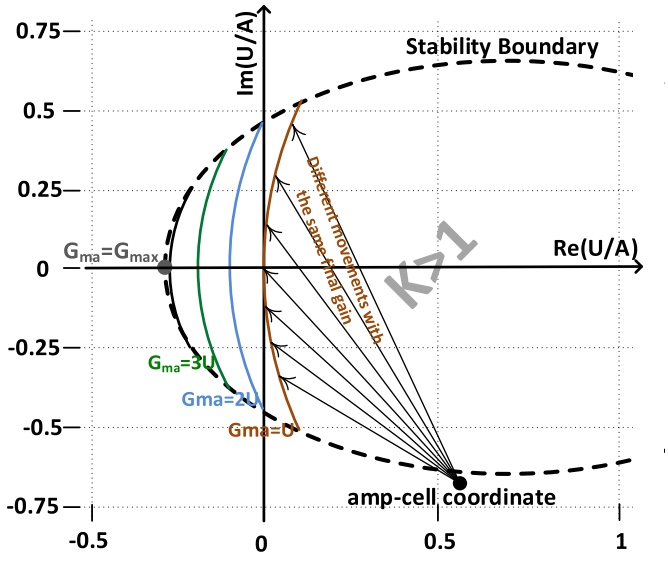


Fig. 5. Different movements (embeddings) can result in the same boosted power gain in a gain plane.

where V_{Sup} is the supply voltage of the amp-cell and G_{L} is the conductance of the simultaneously matched load admittance. Embedding in general functions as a feedback network, and as such it alters the admittances seen from the input and output ports of the embedded amp-cell (G_{S} and G_{L} in Fig. 4, respectively). Because V_{Sup} does not change with embedding, and knowing that load pull would decrease the power gain of the embedded amp-cell compromising its output power with a minimum acceptable gain, the maximum output power of the amp-cell can be estimated from G_{L}. Assuming the harmonic distortion is low at maximum output power, the maximum linear output power would be an acceptable estimation and starting point. After finding the optimum embedding based on linear output power estimation, one can improve the output power by simulating the large-signal performance of the embedded amp-cell and tuning the embedding even further. By changing the impedances seen by the amp-cell, embedding can increase or decrease the output power of the amp-cell itself. In case it increases the output power of the amp-cell at higher rate than the increase in the feedback power [see Fig. 3(a)], embedding can boost both the power gain and the output power of the embedded amp-cell simultaneously.

There are several T-embedding networks that can boost power gain of an amp-cell to a certain value, each of which results in a different G_{L}, and thus different output power. For example, using the gain-plane approach in Fig. 5, it is shown that the power gain of an arbitrary amp-cell can be boosted to U by different movements to different coordinates on the U curve (the gray curve in Fig. 5) [33]–[38]. All these movements result in the same power gain of U; however, they each need a different set of passive elements (jX_S and jB_P) to perform gain boosting [33]. This naturally results in different G_{L}, and hence, the maximum output power of the amp-cell would not be the same for different movements. In [33], the equations of series and parallel embeddings (jX_S and jB_P), are derived to move only to the horizontal axis, Re(U/A), for a desired gain mainly to maximize the stability margins and simplify the derivation. However, moving to a coordinate on Re(U/A) axis for a desired gain does not necessarily result in the maximum output power. To find the optimum embedding for the maximum output power of an embedded amplifier, the equations for jX_S and jB_P are generalized to cover the whole stable region of K >1. The equations and the descriptions are given in Appendix A. In other words, given the desired gain and the location on the equi-G_{ma} curve, the exact passive components can be calculated using these equations. Moreover, they help us quickly and efficiently optimize the embedding network for a desired gain value.

Having this theoretical foundation, and given a specific amp-cell, G_{L} can be calculated for each movement in the gain plane. As shown in Fig. 6, the contours of equi-G_{ma} and equi-G_{L} of a 40-μm CS NMOS in the 65-nm technology embedded by T-embedding at 200 GHz are plotted using the equations in Appendix A. To plot Fig. 6, first, we select a rectangle that is large enough to cover the entire stable region in the gain plane (boundaries of this rectangle can always be changed if later in the next simulation steps it turns out it does cover the entire stable region). Second, this rectangular region is divided into small pixels. Using the equations in Appendix A, the embedding networks are calculated and are used to move the amp-cell to all these pixels. Knowing the embedding networks, K, G_{ma}, and G_{L} were calculated for all the pixels. The region that corresponds to K $\geq$ 1 is found using numerical methods. Finally, the equi-G_{ma} and Equi-G_{L} contours within the stable region were plotted numerically.

It is evident from the figure that different coordinates on an equi-G_{ma} contour are associated with different G_{L} values, resulting in different output power. For example, if one selects to boost the power gain to U, a movement to E_1 would result in $G_{\text{L}} = 4.64$ m$\mho$. For $V_{\text{Sup}} = 1$ V, this translates to a maximum output power of $P_{O,\text{max}} = 3.65$ dBm. However, for the same power gain of U, the transistor can be embedded to move to E_2 or E_3, where G_{L} is equal to 15.2 and 18.4 m$\mho$ resulting in 8.8- and 9.6-dBm output power, respectively. These power levels are significantly higher than the one in E_1. Moreover, E_2 and E_3 are much further from the stability boundary compared with E_1 and therefore are much more reliable operating points. Interestingly, as shown in Fig. 6, the embedding that moves the transistor to E_4 not only results in higher gain of 7.3 dB but also a higher output power of 9.6 dBm, compared with the one for E_1. Intuitively speaking, to boost the power gain to higher values, embedding has to send a larger fraction of the output power to the input of the amp-cell. At the same time, the embedding is also changing the conductance seen by the amp-cell, real($Y_{O,\text{amp-cell}}$). In other words, in the case of E_4, the embedding is boosting the gain by feeding back more power, but at the same time and with a higher rate is increasing the output power of the amp-cell by increasing real($Y_{O,\text{amp-cell}}$). The analysis done in Fig. 6 is for a simple amp-cell of a 40-μm CS CMOS transistor embedded by T-embedding and can be performed for any general amp-cell to understand the PA's trade-offs and behavior and to be able

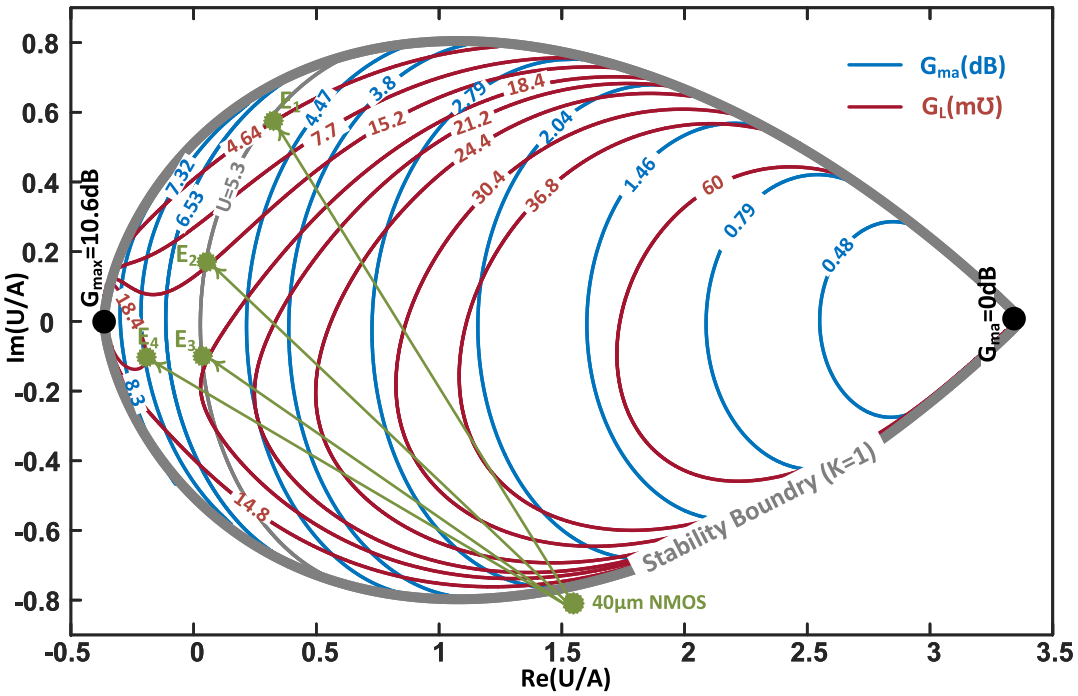


Fig. 6. Contours of equi-G_{ma} and equi-G_L, the conductance of simultaneously matched load admittance, in the gain plane for a 40-μm CS NMOS transistor in the 65-nm bulk CMOS process embedded by T-embedding [33] at 200 Hz.

to optimize for the best possible outcome. It must be noted that if other types of embeddings rather than T-embedding are used to move to the same coordinates in Fig. 6, the same U/As can correspond to different G_Ls from what is shown in the figure.

IV. High-Power/Gain Matched Cascode Amp-Cell at 200 GHz

As Fig. 3(a) suggests, the output power of an embedded PA is directly a function of its amp-cell's power capability. To enhance the output power of a single-transistor amp-cell (e.g., CS amp-cell), one can increase the size of the transistor. Nonetheless, a large transistor typically has low input–output impedances, and consequently high matching loss and low stage gain. This limits the maximum transistor size for an acceptable gain and output power at high mm-wave frequencies. The output power of the amp-cell can be boosted further using stacked transistors to increase the output voltage swing without exceeding the allowable voltage stresses of the transistors. However, stacking reduces the power gain since the gate capacitors function as negative feedback [29], [30]. This reduces the gain of the amp-cell and limits the operation frequency of this topology to low mm-wave frequencies. In this section we introduce a matched cascode amp-cell that delivers higher P_{out} at a higher power gain compared with a traditional cascode amp-cell at high mm-wave frequencies.

Gain compression is the result of transistors leaving their linear region, or clipping in the output voltage due to exceeding the rail voltages (e.g., 0 V and $2V_{Sup}$). The change in the operation region or clipping in the output voltage changes the transfer function of the amp-cell for a fraction of input cycle and leads to harmonic generation and gain compression. To avoid gain compression at low output powers, the amp-cell must be designed such that the output voltage reaches its rail-to-rail swing before the amp-cell transistor(s) exit their linear region. This guarantees that gain compression starts at maximum linear output power.

A CMOS transistor exits its linear region, if V_{GS} falls below the threshold voltage (V_{th}) corresponding to the Off region, or if V_{GD} exceeds V_{th}, corresponding to the Triode region. A traditional cascode amp-cell is shown in Fig. 7(a), on the left. Starting with the size of the transistors, it is assumed that the maximum transistor size that results in an acceptable input matching loss is selected for the CS transistor (M_1). The common-gate (CG) transistor (M_2) is selected to have the same size as the CS to ensure equal drain–source voltages without altering the optimum gate biasing voltages for maximum gate–source/gate–drain swing. On the right side of the figure, the small-signal equivalent of the amp-cell is shown. C_{GD} of the transistors is split into two miller capacitors at the gate and drain terminals, C_{Min1} and C_{Mout1}, respectively. To reach a high output power, I_{D2} must be maximized without pushing V_{GS} and V_{DS} into nonlinear regions. However, since M_1 and M_2 are large and the operation frequency is high, the total parallel parasitic capacitor ($C_{DB1} + C_{Mout1} + C_{GS2}$) has a very small impedance at high mm-wave frequencies, leading to a small V_{GS2} and hence a small I_{D2} and output power. In this scenario, to achieve a high I_{D2}, a large V_{GS1} is needed to generate a large I_{D1} and V_{GS2}. Therefore, before delivering high I_{D2} to the load, M_1 enters the Off region compressing the power gain of the amp-cell and limiting OP1dB. As a result, the large parasitic capacitor at the drain of M_1 results in a low power gain, as well as the amp-cell would have a small output power for large input power. Accordingly, a traditional cascode

amp-cell neither has high power gain nor high OP1dB at high mm-wave frequencies. The cascode amp-cell shown in Fig. 7(a) has a gain of 2.9 dB, and 3-dB matching loss at the input results in a total stage gain of −0.1 dB at 200 GHz. The amp-cell also has a OP1dB of 4.7 dBm, when matched to its conjugate load impedance and supplied from 2.4 V. The output power at the 1-dB stage gain is not defined as the small-signal stage gain is already lower than 1 dB (−0.1 dB).

To improve the low impedance at D_1, an inductor can be added between the node and the ground to resonate out the parasitic capacitances, as in Fig. 7(b). In this figure, Ind_1 that is composed of the transmission line $\text{TL}_{\text{M},1}$ and the dc block capacitor C_{blk} increases the total impedance seen by I_{D1}. This increases V_{D1} swing and accordingly V_{GS2} swing, and boosts the power gain and output power at the same time. However, this resonance also degenerates the source of M_2 with an impedance, Z_{DG}, that results in a smaller conductance at the output port of the amp-cell. Thus, the conductance of the conjugate matched load drops and $P_{o,\max}$ declines. With a small-signal stage gain of 3.2 dB, this amp-cell has an OP1dB of 3.1 dBm and delivers 4.1 dBm to the load at the 1-dB stage gain at 200 GHz.

To optimize the impedance seen by the source terminal of M_2, TL_{M2} is added between the drain of M_1 and the source of M_2 as depicted in Fig. 7(c). This transmission line increases the resistance of Z_{DG} from 3.9 to 6.4 Ω and decreases its reactance's absolute value from 5.3 to 1.5 Ω. This increase in the resistance-to-reactance ratio of the degeneration impedance increases this ratio at the output of the amp-cell as well. Therefore, the conductance of Y_{out} increases to 21.3 m℧, and this increases the output power. This amp-cell called matched cascode as Ind_1 and $T_{\text{L,M2}}$ increase the power flow from M_1 to M_2, and eventually to the load. This amp-cell has an OP1dB of 9.8 dBm and its stage gain is 1.2 dB at 200 GHz.

The minimum gain of the amp-cell after embedding is selected to be 6 dB at 210 GHz to make 2-dB compression possible before the stage gain falls below 1 dB. To find the coordinate of the $G_{\text{ma}} = 6$ dB arc in the gain plane that results in the maximum output power, first we used two pre-embeddings, $\text{TL}_{E,1}$ and $\text{TL}_{E,2}$, to adjust the direction of the movements in the gain plane toward the desired coordinates on the $G_{\text{ma}} = 6$ dB arc [33]. Then, a parallel embedding, $\text{TL}_{E,3}$ and $\text{TL}_{E,4}$ along with C_f for dc decoupling, was used to move to the desired coordinates on the arc. Since all the embedding elements are lossy, U changes after embedding. To compensate for the change in U, different pre-embeddings were used to move in slightly different directions and to be able to sweep the area around the coordinates that correspond to the maximum P_{out}. Finally, large-signal simulations were done to fine-tune the embedding for maximum output power. The matched cascode cell is embedded as shown in Fig. 8. All the embedding components are implemented as microstrip transmission lines in m9 metal layer of the process with m2 as the ground plane. The pre-embeddings help avoid high loss of series embedding and have an electrical lengths of 0.1λ and 0.3λ, respectively, [33]. $\text{TL}_{E,3}$ and $\text{TL}_{E,4}$ have lengths of 0.25λ and 0.1λ, respectively. The decoupling capacitor C_{blk} is a multi-layer capacitor composed of m2–m4 metal layers of the process. This decoupling capacitor in conjunction with $\text{TL}_{\text{M},1}$ forms a 26-pH inductor with a quality factor of 11 at 210 GHz. Fig. 9 shows the simulation results of the last-stage amp-cell

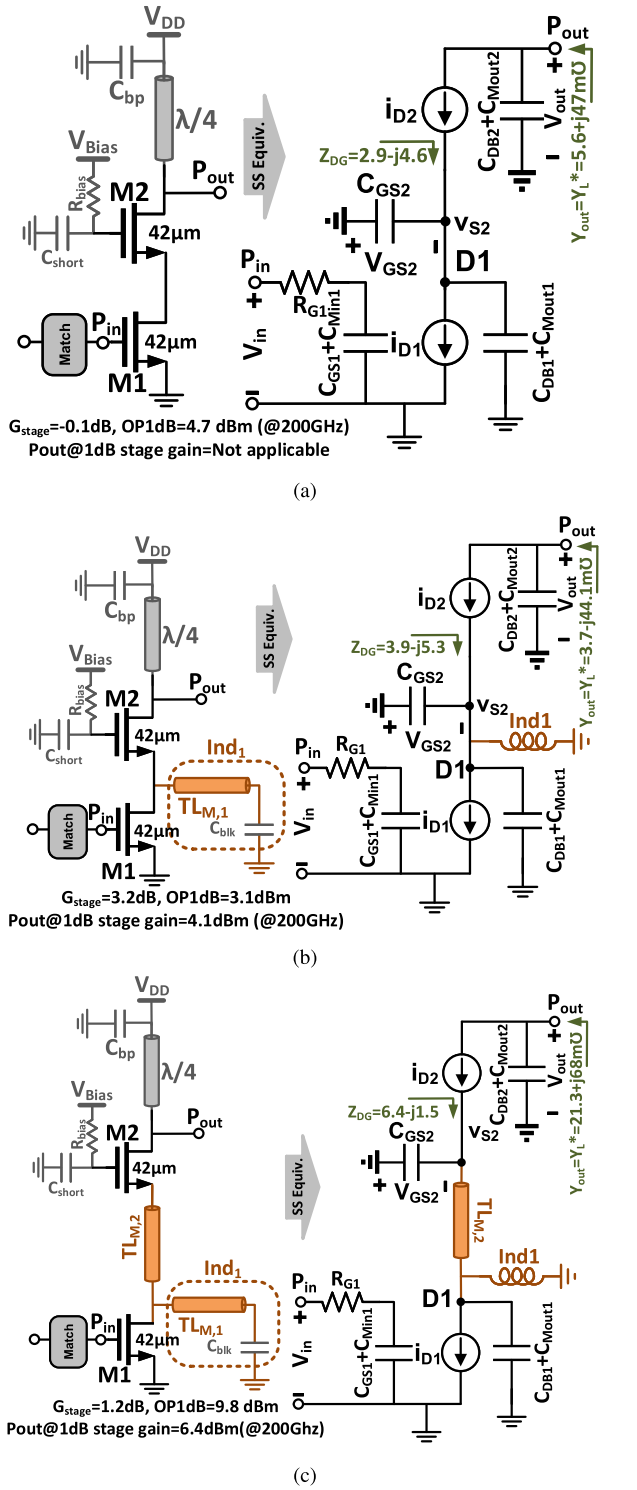


Fig. 7. (a) Traditional cascode has no gain and low OP1dB. (b) Cascode with the tuning inductor Ind_1 has higher power gain, still degeneration seen by M_2's source terminal reduces OP1dB. (c) Matched cascode has a modified degeneration impedance while benefiting from the tuning inductor Ind_1 too. It delivers both high OP1dB and high power gain. In all the three cases, the loss of preceding matching network is 3 dB, the supply voltage is 2.4 V, and the reported numbers are at 200 GHz.

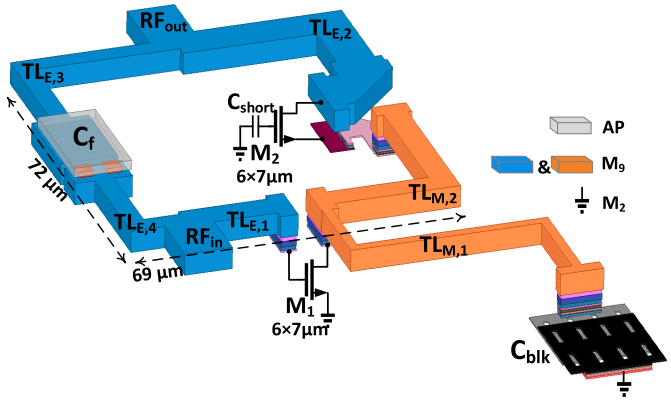


Fig. 8. Embedding used to boost power gain of the matched cascode amp-cell and maximize its output power.

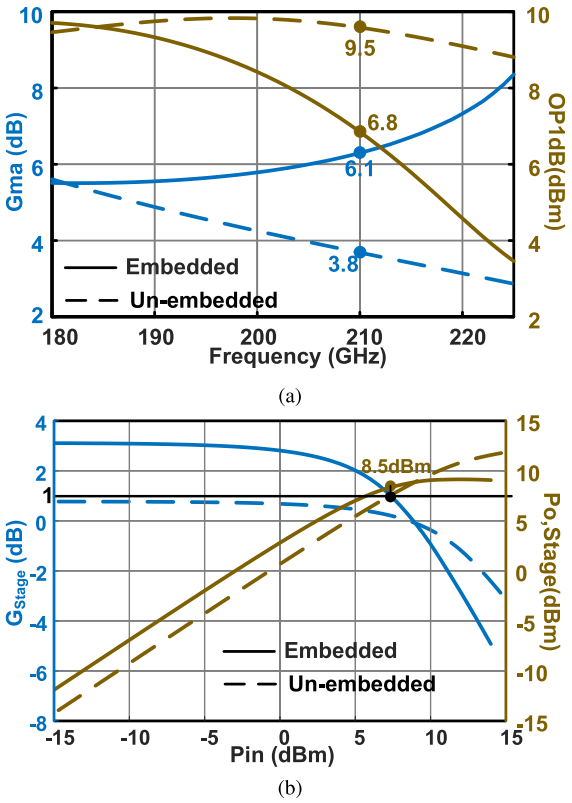


Fig. 9. (a) Maximum available gains (G_{ma})s and output 1-dB compression points of matched cascode (un-embedded) and embedded matched cascode (embedded) versus frequency. (b) Stage gain and stage output power at 1-dB stage gain before and after embedding at 210 GHz.

before and after embedding. As it can be seen, the power gain is boosted by 2.3 dB. This results in 8.5-dBm output power at the 1-dB stage gain at 210 GHz after embedding.

V. Wideband, Balanced SPC

Using large transistors and increasing the output swing using the proposed matched cascode amp-cell along with gain boosting could be exploited to increase the output power of a PA. To boost the output power further, traditionally power combiners are used at the end of PA chains. Nevertheless,

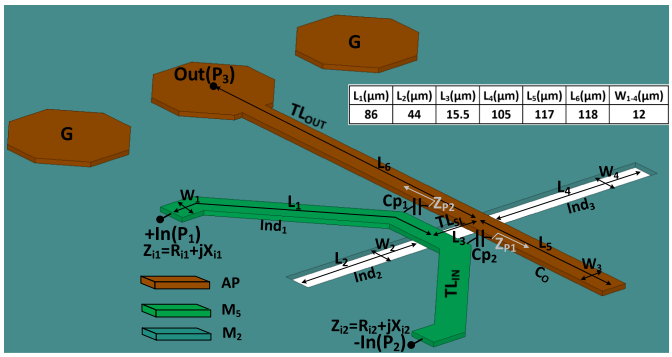


Fig. 10. 2-to-1 differential SPC.

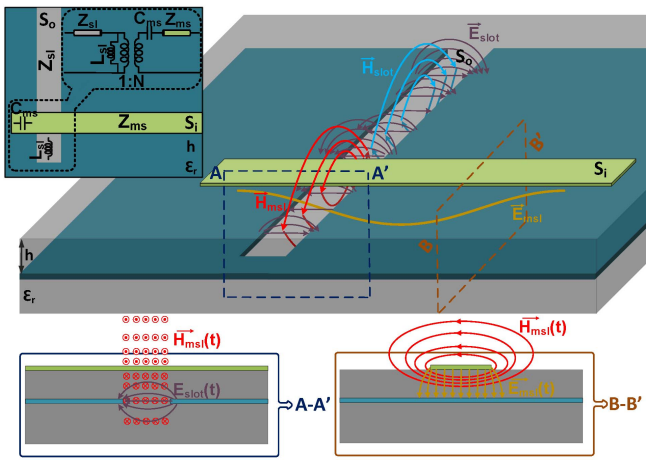


Fig. 11. Microstrip-slotline transition and its equivalent circuit.

power combiners suffer from known deficiencies, namely, high loss, and large/imbalanced impedances at the input ports. Large input impedances increase the impedance transformation ratio of the matching network between the last PA cell and the power combiner and therefore the loss [33]. Whereas imbalanced input impedances result in non-optimum loading of the last PA cells and phase mismatch of their output signals, both adversely affecting the total output power. This section introduces a two-to-one low-loss, wideband, balanced SPC with low input impedance.

The proposed SPC is shown in Fig. 10. Two out-of-phase signals from the last PA cells are applied to the input ports of the power combiner (P_1 and P_2). This differential signal creates a current in TL_{in}, which passes over the slotline in the ground plane perpendicularly. This current induces an electromagnetic (EM) wave in the slotline. The reciprocal of this transition takes place between the slotline and TL_{out}, which is in parallel with TL_{in}, and the combined signal would be delivered to the load. Fig. 11 shows a microstrip-slotline intersection and signal transition from its input port to the output port. A microstrip on a substrate with a height of h and permittivity of ε_r passes perpendicularly over a slotline etched in the ground plane. It is assumed that the input signal, S_i, is fed to the microstrip from the right side. A time-varying electric field $[E_{msl}(t)]$ and magnetic field $[H_{msl}(t)]$ start traveling

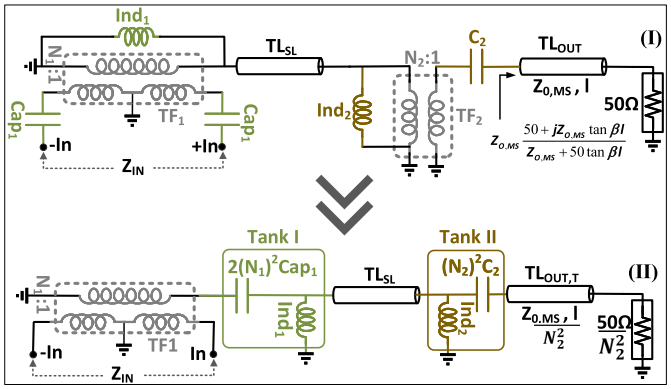


Fig. 12. Equivalent circuit of the SPC shown in Fig. 10.

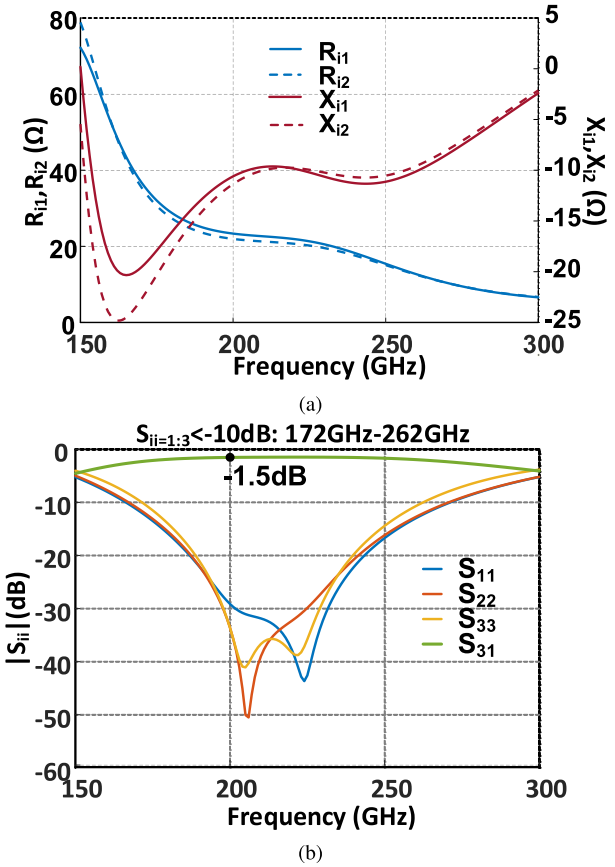


Fig. 13. (a) Simulated input impedances of the SPC shown in Fig. 10. (b) Simulated S-parameters of the SPC.

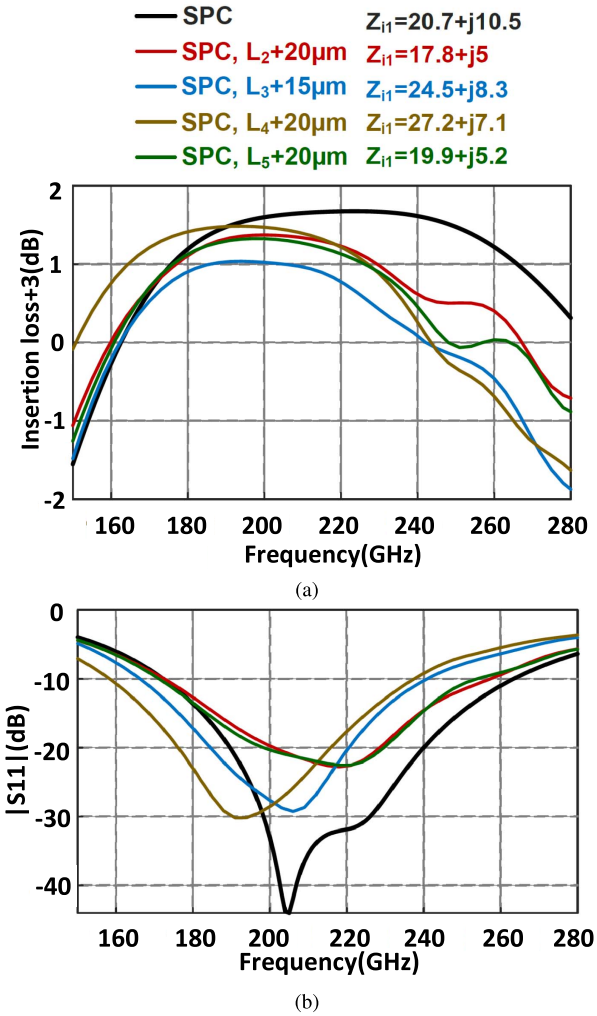


Fig. 14. (a) Changes in the insertion loss and input impedance of the SPC by geometry. SPC is the response of the SPC shown in Fig. 10. (b) Changes in the return loss.

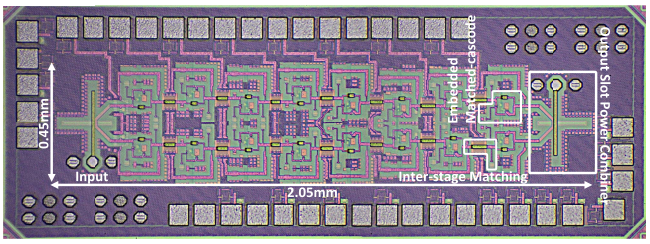
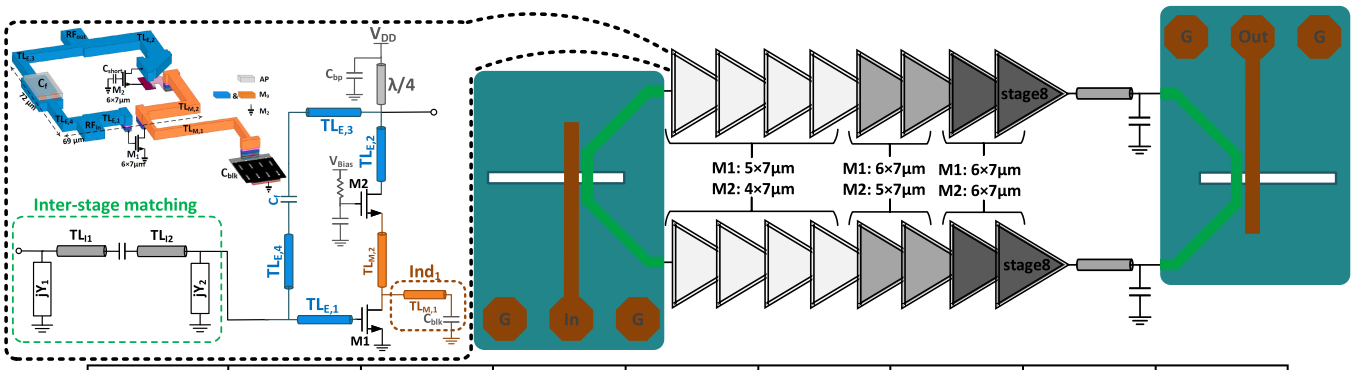


Fig. 15. Die micro-photograph of the PA.

toward the open end of the microstrip. At the intersection with the slotline, the time-varying $H_{msl}(t)$ induces a time-varying electric field $[E_{slot}(t)]$ perpendicular to the slotline edges, as shown in Fig. 11. This electric field generates a voltage across the edges of the slotline that changes with time and results in a time-varying current in the slotline. This current generates the slotline time-varying magnetic field $H_{slot}(t)$ and together with $E_{slot}(t)$ propagate to the output port of the slotline. This transition can naturally happen in an opposite fashion from the slotline to the microstrip.

The microstrip-to-slotline transition can be modeled by an equivalent resonant circuit shown on the left side of Fig. 11. The circuit consists of a transformer with a transformation ratio of N, where N is a function of the transmission lines characteristic impedances Z_{ms} and Z_{sl} [39]. L_{sl} is the inductance of the shorted slotline and C_{ms} is the capacitance of the open microstrip.

The equivalent circuit of the SPC is shown in Fig. 12. Since the signal experiences two transitions between the slotline and the microstrip, two transformers with inductors and capacitors



Stage #	1		2		3		4		5		6		7		8	
	M1	M2	M1	M2	M1	M2	M1	M2	M1	M2	M1	M2	M1	M2	M1	M2
Bias Voltage (V)	0.7	1.9	0.7	1.95	0.73	2.05	0.75	2.1	0.85	2.1	0.9	2.2	0.95	2.2	1.05	2.2

Fig. 16. Proposed 2-by-8 embedded PA (right), the amp-cell, and its layout along with the matching network (left). Each 7-μm transistor has ten fingers, and each finger has a length of 0.7 μm.

exist in the equivalent circuit of the SPC [see Fig. 12(I)]. The components in the secondary of TF_2, can be transferred to its primary, and the same can be done to Cap_1. These transfers result in the simplified filter shown Fig. 12(II). Two tanks exist in the simplified equivalent circuit of the power combiner creating two resonant frequencies. These resonant frequencies can be designed to be far from each other to get a wideband performance [40].

The power combiner's input microstrip line is completely symmetric with respect to the slotline. At the middle of the structure, as shown in Fig. 10, two parasitic capacitors C_{P1} and C_{P2} couple the input and output microstrip lines. These capacitors see different impedances (Z_{P1} and Z_{P2}) and therefore are the only source of imbalance between the input impedances in the power combiner. However, the metal layers used for the input and output microstrips are different, and the length of the input microstrip in parallel with TL_{OUT} is minimized, and therefore, C_{P1} and C_{P2} are very small and the mismatch they cause between the input impedances is negligible. As shown in Fig. 13(a), the input impedances of the implemented SPC are very close to each other at 170–300 GHz. Fig. 13(b) illustrates the wideband performance of the SPC. The return losses at the input ports stay lower than -10 dB from 172 to 262 GHz, which results in 41.5% fractional bandwidth. The output pads are included in the simulations of Fig. 13.

The insertion loss of the combiner is 1.5 dB at 200 GHz, with a 1-dB bandwidth of 74 GHz. To adjust the response of the SPC, one can change the values of the filter components shown in Fig. 12 by altering the lengths/widths of the slot line and microstrip lines in Fig. 10. Different inductor sizes, $L_{i=1:4}$, in the SPC shown in Fig. 10 are increased, and the insertion losses, the input impedances, and the input reflection coefficients are simulated and shown in Fig. 14. The black curves in Fig. 14 correspond to the SPC shown in Fig. 10. Increasing the lengths of the open microstrip line and the shorted slotline results in lower center frequencies. The longer these lengths are, the larger their equivalent capacitance/inductances would be in Fig. 12, and the smaller the resonance frequencies of the tanks would become. Increasing L_3 increases the insertion loss and at the same time lowers the center frequency. Fig. 14(b) shows that the input ports of the SPC stay matched for over 60-GHz bandwidth.

VI. Implementation and Measurement Results

The chip microphotograph is shown in Fig. 15. The dimensions of the chip are 0.95 mm $\times$ 2.6 mm, where the active area including the input and output pads is 0.45 mm $\times$ 2 mm. Using the proposed matched cascode amp-cell, an embedded 2-by-8 PA is implemented in the TSMC 65-nm Bulk CMOS process at 200 GHz as shown in Fig. 16. The implementation of neutralizing capacitors for the proposed amp-cell would need very small capacitors with long transmission line routings, because of the amp-cell dimensions. Therefore, neutralizing circuit of the proposed amp-cell would become ineffective.

To maximize the dc efficiency and improve the power gain of the driver stages, the sizes of the transistors are reduced toward the input of the PA. The gate biasing voltages of M_1 and M_2 (Fig. 16) of the driver stages are selected to be slightly lower than the last stages, because it would improve the power gain and reduce the dc power consumption. In the last stages, higher biasing voltages are chosen to improve the output power of the PA. The first four driver amp-cells have a simulated power gain of 6.9 dB and an OP1dB of 3.1 dBm. The amp-cells of stages 5 and 6 have a simulated power gain of 5.9 dB and an OP1dB of 6.2 dBm.

The SPC shown in Fig. 10 is used at the output port of the two power amplification paths to boost the output power. The same SPC is used at the input port as well. To conserve the gain of amp-cells, all of them are matched to their complex conjugate impedances. A capacitor or inductor is used for jY_1 and jY_2 in the inter-stage matching networks when needed. All the PA cells are provided with a V_{Sup} of 2.4 V. With a correct gate biasing voltages, simulation shows that the maximum voltage swing on gate–source and gate–drain junctions is 1.1 V.

A PNA-X together with two VDI WR-5.1 frequency extender modules are used to measure the S-parameters of the

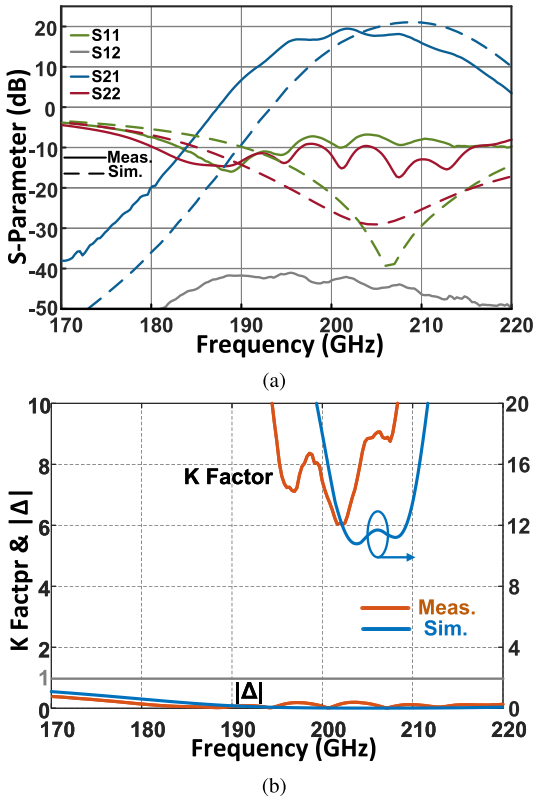


Fig. 17. Simulated and measured (a) small-signal S-parameters and (b) stability factors.

PA. The small-signal simulation and measurement results are shown in Fig. 17. The simulated S_{21} has a maximum of 20.7 dB at 209 GHz, and S_{11}/S_{22} is below −10 dB from 190 to 220 GHz. The measurement shows that the PA has a center frequency of 202 GHz, at which S_{21} peaks at 19.5 dB, with a 3-dB bandwidth of 13.4 GHz from 195.3 to 208.7 GHz. There is 7-GHz frequency shift between the simulated and measured S21. This shift is caused most likely by the inaccuracies in the device interconnects and passive components' modeling. The measured input and output reflection coefficients are less than −6.8 and −9.1 dB from 179.5 to 218.4 GHz, respectively. Simulated K and $|\Delta|$ satisfy unconditional stability requirements over all frequencies. The measurement results show that the PA is unconditionally stable and has a stability factor (K) larger than 1, and $|\Delta|$ smaller than 1 from 140 to 220 GHz.

Fig. 18 shows the large-signal measurement setup. At low input powers, the setup does not include the VDI WR4.3 amplifier, and the frequency extender, VDI WR-5.1 × 6, is directly connected to the S-bend. The output power of the frequency extender was measured and calibrated using an Erikson PM5 power meter from 180 to 220 GHz. Then, the S-bends and probes were added to the setup, the probes were landed on a through structure of a calibration kit, and the output power of the S-bend on the right side of Fig. 18 was measured across the same frequency band. Using these two sets of information, the losses of the S-bends and the probes were calibrated. Using all these calibrations

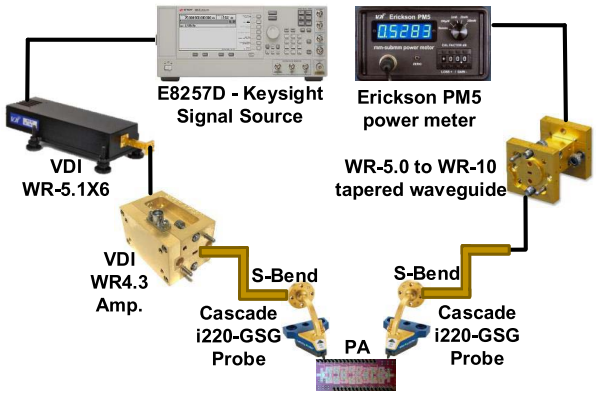


Fig. 18. Large-signal measurement setup.

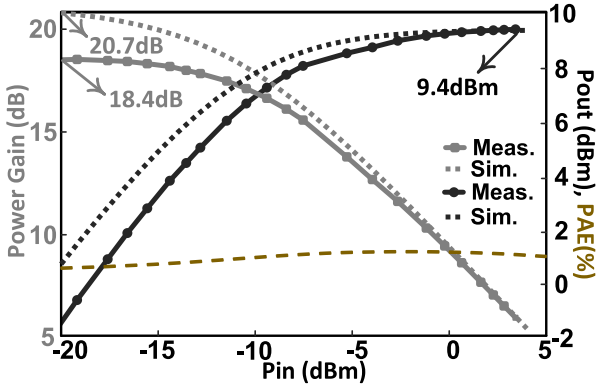


Fig. 19. (a) Power gain, output power, and PAE. Simulation at 209 GHz and measurement at 200 GHz. (b) Simulated and measured P_{sat}/OP1dB as a function of frequency.

and measurements, the output power and power gain of the PA were measured versus the input power across the band from 180 to 220 GHz. However, the output power of the frequency extender was not enough to saturate the PA. Hence, a VDI WR4.3 amplifier was added to the setup as shown in Fig. 18, and the output power of the VDI WR4.3 amplifier was calibrated similar to other blocks. Fig. 19(a) shows that the PA has an output 1-dB compression point of 6.3 dBm and an output saturated power of 9.4 dBm at 200 GHz. As shown in Fig. 19(b), the PA has a 1-dB P_{sat} bandwidth of 14 GHz

TABLE I
PERFORMANCE COMPARISON TO STATE-OF-THE-ART

Reference	**This work**	[33]	[41]	[42]	[43]	[44]	[45]
Technology	**65nm CMOS**	65nm CMOS	130nm BiCMOS	130nm BiCMOS	65nm CMOS	65nm CMOS	32nm SOI CMOS
f_{max} (GHz)	**400**	352	370	500	395	395	320
3dB Bandwidth (GHz)	**195-209**	251-263	200-220	200-255	275-284[1]	227.5-257.5	205-225
Gain (dB)	**19.5 (22.5**)**	9.2	25	12.5 (15.5**)	12	13.9	15**
OP1dB (dBm)	**6.3 (7.8*)**	-8	4	9 (10.5**)	-5.9	-5.1	2.7*
P_{sat} (dBm)	**9.4 (10.9*)**	-3.9	9.6	12 (13.5**)	-4.7	-3.3	4.6*
PAE max (%)	**1.03 (1.4**)**	1.35	0.5	2.14(3**)[2]	1.62	1.6	6**
V_{DD} (V)	**2.4**	1	3.3	3.3	0.85	0.85	1
DC power (mW)	**732**	27.6	1824[1]	740	17.85	23.8	40
Active area (mm^2)	**0.92 (0.52***)**	0.14	0.84[1]	0.83	0.056	0.053	0.06***
FOM[%]	**52.1 (57.9**)**	30	54	51 (55.5)	33	36.4	50.6**

PERFORMANCE COMPARISON TO STATE-OF-THE-ART.

*Loss of output balun/power combiner is de-embedded
**Loss of input and output balun/power combiner is de-embedded
*** Areas of input and output blauns as well as DC pads are not included
[1] Calculated from reported numbers and/or graphs
[2] Max. drain efficiency
[%] FOM=P_{SAT}[dBm]+Gain[dB]+10log(freq[GHz])+10log(PAE_{MAX}[%])

from 194 to 208 GHz and delivers more than 6 dBm to its load from 191 to 214 GHz. The output 1-dB compression point stays more than 3 dBm from 192 to 212 GHz. The power-added efficiency (PAE) reaches a maximum of 1.03% at output power of 8.77 dBm with a power gain of 10.74 dB, as shown in Fig. 19(a). Table I shows the summary of the proposed embedded PA performance compared with the state-of-the-art. The PA features the highest gain, P_{sat}, and OP1dB in CMOS technology at >200-GHz frequencies.

VII. CONCLUSION

The analysis and effect of power gain, and gain boosting by embedding on the PA output power are presented in this article. Equations for power contours of embedded amp-cells were derived and presented to help designers find the optimum embedding that maximizes the output power for a particular gain. Analyzing the power limitations of a cascode cell, a high-power, high-frequency, and embedded amp-cell was introduced. Then, a wideband, balanced, series power combiner was designed and used to further boost the output power. Using embedded matched cascode amp-cells and the SPC, a 200-GHz PA with 19.5-dB gain and 9.4-dBm P_{sat} was implemented in the 65-nm bulk CMOS, and its performance was reported.

APPENDIX I
EMBEDDING FOR MAXIMUM OUTPUT POWER

To find the coordinates of an equi-gain arc that results in the maximum output power, the equations of T-embedding in [33] must be generalized to move the amp-cell to any arbitrary coordinates in the gain plane. Once the generalized equations are derived, one can plug in all the coordinates of an equi-gain curve, and using the analysis in Section III find the coordinates with the maximum output power, that is, maximum G_L. The generalized equations of T-embedding are driven as follows. In these equations, (H,V) are any desired coordinates in the gain plane, and $Z_{i,j}$'s are the Z-parameters of the amp-cell

$$X_{TS} = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a},$$
$$B_{TP} = (C_5 \times X_{TS} + C_6)/(C_3 \times X_{TS} + C_4) \quad (2)$$

where

$$a = C_1 \times C_3 + C_5 \times C_7,$$
$$b = C_1 \times C_4 + C_2 \times C_3 + C_5 \times C_8 + C_6 \times C_7,$$
$$c = C_2 \times C_4 + C_6 \times C_8 \quad (3)$$

where

$$C_1 = U - H,$$
$$C_2 = \mathrm{U} \times \mathrm{Im}(Z_{12}) - V \times \mathrm{Re}(Z_{21}) - H \times \mathrm{Im}(Z_{21}),$$
$$C_3 = (H - U) \times \mathrm{A\text{-}V} \times B,$$
$$C_4 = (H - U) \times \mathrm{Im}(\Delta Z) + V \times \mathrm{Re}(\Delta Z),$$
$$C_5 = -V,$$
$$C_6 = -U \times \mathrm{Re}(Z_{12}) + H \times \mathrm{Re}(Z_{21}) - V \times \mathrm{Im}(Z_{21}),$$
$$C_7 = (H - U) \times B + V \times A,$$
$$C_8 = (U - H) \times \mathrm{Re}(\Delta Z) + V \times \mathrm{Im}(\Delta Z) \quad (4)$$

where

$$A = \mathrm{Re}(Z_{11}) + \mathrm{Re}(Z_{22}) - \mathrm{Re}(Z_{12}) - \mathrm{Re}(Z_{21}),$$
$$B = \mathrm{Im}(Z_{11}) + \mathrm{Im}(Z_{22}) - \mathrm{Im}(Z_{12}) - \mathrm{Im}(Z_{21}),$$
$$\Delta Z = Z_{11}Z_{22} - Z_{12}Z_{21}. \quad (5)$$

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