A Hybrid Modular Multilevel Converter Family with Higher Power Density and Efficiency

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***Abstract* - Modular multilevel converter (MMC) has many advantages of scalability, reliability and easy implementation, but suffers from large number of switching devices and capacitors. To improve the power density and efficiency for medium voltage applications, this paper introduces a hybrid modular multilevel converter (HMMC) family through the combination of active neutral-point-clamped converter (ANPC) and chain-link arm. Three topologies in HMMC family can effectively reduce chain-link voltage by half compared with traditional MMC. Single- and three-phase operation principles are presented to highlight this important features. Several critical metrics, such as component number, capacitor sizes and semiconductor losses, are compared between the conventional MMC and HMMC topologies at three different medium voltage levels. The result indicates the best topology from the HMMC family can save around 30% devices, 50% total capacitor and 32% power losses compared with traditional MMC. A simple single-phase control method is also mentioned to balance capacitor voltage. Finally, a single-phase HMMC experimental prototype is built to verify the effectiveness of three topologies.**

***Index Terms* – Hybrid modular multilevel converter (HMMC), active neutral-point-clamped converter (ANPC), semiconductor losses, comparison.**

I. Introduction

Modular multilevel converter (MMC) as shown in Fig. 1 has emerged as one of the promising topologies in recent years for medium or high voltage industrial applications, such as high voltage dc transmission (HVDC) [1]-[3], static synchronous compensators [4] and offshore renewable energy integration [5], solid state transformer (SST) [6] and medium voltage motor drives [7-9]. Compared to the conventional two-level or three-level voltage source converter (VSC), its features such as high flexibility and scalability for different voltage and power levels, low harmonics content and fault tolerant operation capability gives MMC a competitive edge over its counterparts [10]–[12].

However, in spite of these advantages, MMC still has some limitations. First, the number of IGBTs is doubled with the half-bridge (HB) sub-module (SM) and even fourfold with full-bridge (FB) SM. This significantly increases the system cost. Second, the use of low-voltage rating IGBTs in SM results in higher conduction losses for medium-voltage (MV) and high-voltage (HV) applications, leading to more devices in parallel in order to reach efficiency target. Third, a larger, bulky and heavy dc capacitor is required to suppress dc-link voltage ripple of each SM [13]. According to Siemens [14], in case of MMC converters used for different applications, about 75% of SM volume is occupied by the capacitors. As a result of the increased semiconductor count and capacitor value, the MMC is less compact than a two-level or three-level VSC of the same rating.

To address these challenges, some control methods, revised topologies and several hybrid converters have been proposed to improve the power density of MMC [15]. Multiple techniques are proposed to inject appropriate harmonics in the circulating current to reduce dc-link capacitor voltage ripple [16], [17], such as second and fourth harmonic current components. These methods could effectively reduce required capacitance, but the semiconductor device losses are increased at the same time [18]. Some control methods like asymmetric mode control [19] and switching cycle control [20] are also employed to reduce dc-link ripple. In addition, there are many efforts put to modify the MMC topology like FC-MMC [21], or MMC with star-connected FB SM branches [22]. Another method is trying to reduce the SM number directly. The alternate arm converter (AAC) with series-connected IGBTs and SM is proposed to implement a compact design [23-25]. However, the SM voltage balancing requires specific operation conditions and dc-link current ripple cannot be neglected. The modular embedded thyristor-directed converter (METDC) proposed recently in [26] and hybrid multilevel converter in [27], [28] adopt series interconnection of three phases at dc side, which helps to reduce the blocking voltage and device number. However, their ac and dc sides are strongly coupled together, and a high common-mode voltage insulation requirement transformer is required.

Apart from these topologies and control methods, a modular embedded multilevel converter (MEMC) using HV ~~thyristor isthyristor~~ is proposed in [29], [30], which combines the advantages of three level VSC and MMC. Based on the three-level wave

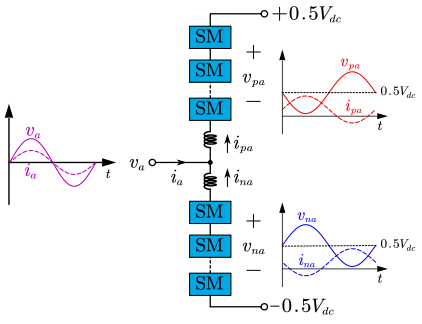


Fig. 1 Conventional single-phase MMC Structure and arm waveforms.

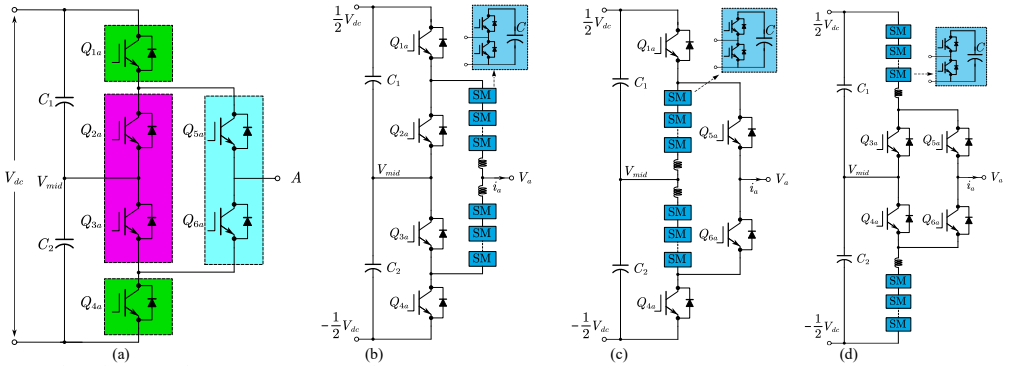


Fig. 2 Topology of (a) ANPC, (b) HMMC 1, (c) HMMC 2, (d) HMMC 3.

created by thyristor stack, the chain-link arm generates the multilevel waveforms to synthesize the sinusoidal output voltage and facilitate the thyristor commutation process. In this way, the maximum chain-link arm voltage could be reduced to 50% of MMC, leading to smaller number of semiconductor devices as well as total SM capacitors. Therefore, MEMC shows great potential in some applications which are sensitive to the converter size and power density, such as offshore windfarm and emerging electric ship tractions [31]. Through the same idea, [32] proposes a hybrid multilevel dc–ac converter (HMC) with series IGBTs and SMs, and operates the IGBT stacks to achieve soft-switching during the commutation. But both topologies require FB SMs to achieve thyristor commutation or IGBT soft switching under different power factor (PF) conditions. The commutation failure and subsequent damage on HV stacks can easily occurs in the field operation. [33] proposed a neutral-point-clamped MMC (NPC-MMC) which adds two dc side decoupling capacitors, so that NPC-MMC three phases can be controlled independently. However, using this method the sum of three-phase mid-point currents will not be zero, which means the dc side capacitor should be big enough to suppress the voltage ripple.

Extending the concept of [30-33], a three-level hybrid MMC (HMMC) family is proposed and investigated in this paper. As shown in Fig. 2, three pairs of switches in active neutral-point-clamped converter (ANPC) can be replaced by the chain-link arms, respectively, while the left four switches employs the low-speed high voltage IGBT stacks. In this way, three kinds of dc-ac HMMC topologies (HMMC 1, HMMC 2 and HMMC 3) are derived. Different from [30] and [32], small dc-side commutation capacitors C_1 and C_2 are added to facilitate IGBT stack commutation under different PF conditions, which can also enhance the firing signal fault tolerant capability. In order to investigate the benefit of the HMMC family, a comprehensive operational analysis and comparison with traditional MMC are conducted in this paper.

The outline of this paper is as follows. In Section II, the single-phase working principles and three-phase configuration are illustrated to highlight the features of reduced maximum arm voltage. The trapezoidal type arm current allocation is also presented for three topologies. Section III presents a comparison of studied three converters with HB-MMC and discusses the number of semiconductor and SM capacitor requirement in several specific MV cases. Besides, the semiconductor losses are approximated and calculated to compare the efficiency performance. Finally, section IV briefly describes the single-phase control scheme that was employed for studied converters, and experimental results are also provided to validate the effectiveness of three topologies.

Note that this paper focuses on steady-state analysis and hence the evaluation of the transient of the discussed converter will be addressed in separate papers.

II. Topology and Basic Operation Principles

A. Operation Principles of HMMC 1

In order to reduce the voltage stress and generate the basic three-level waveform, the IGBT stacks need to act according to the polarity of AC side voltage. Take phase a as an example, when V_a is positive, Q_{1a} and Q_{3a} are turned on, Q_{2a} and Q_{4a} are turned on as Fig. 3 (a). This phase works on P state, which means this phase is connected to the positive terminal and the midpoint. Therefore, the upper arm voltage V_{pa}^* and lower arm voltage V_{na}^* could be calculated by dc voltage V_{dc} and ac voltage V_a,

$$\begin{aligned} V_{pa}^* &= \frac{1}{2}V_{dc} - V_a \\ V_{na}^* &= V_a - V_{mid} \end{aligned} \tag{1}$$

On the contrary, when output voltage V_a is negative, Q_{2a} and Q_{4a} are turned on, Q_{1a} and Q_{3a} are turned off as Fig. 3(b). This phase works at N state, which means it is connected to the midpoint and the negative terminal. Then arm voltage is,

$$\begin{aligned} V_{pa}^* &= V_{mid} - V_a \\ V_{na}^* &= \frac{1}{2}V_{dc} + V_a \end{aligned} \tag{2}$$

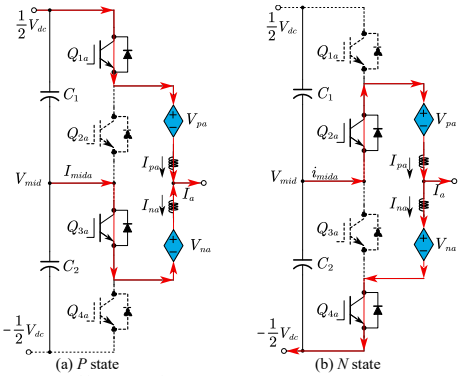


Fig. 3 Two working states of HMMC 1.

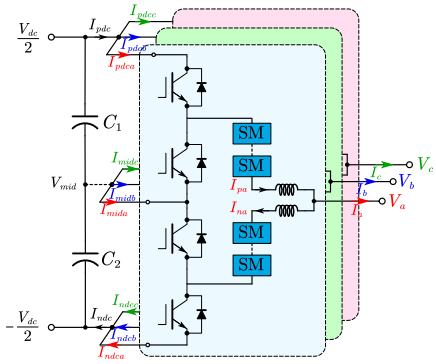


Fig. 4 Three-phase HMMC 1 structure.

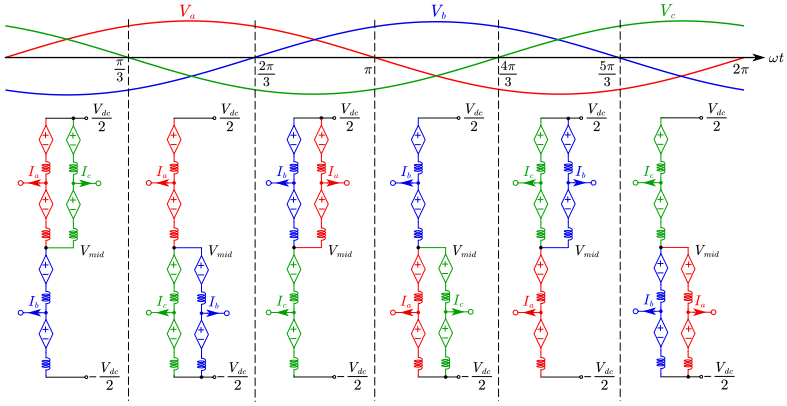


Fig. 5 Three-phase configuration of HMMC 1 during one fundamental period.

In addition, there is a *Z* state as the transition between *P* and *N* state with Q_{2a} and Q_{3a} turned on, which is not used in this paper. Compared to the original topology proposed in [24] and [26], the biggest difference in this topology are two dc side capacitors. It can help to commutate the IGBT when the state change happens at the zero crossing point of output voltage. Otherwise, the IGBT may have the problem of arm current conflict. As shown the three-phase HMMC 1 in Fig. 4, when phase *a* is at *P* state, the midpoint current of three phases I_{mida}, I_{midb} and I_{midc} without dc capacitors should satisfy

$$I_{mida} + I_{midb} + I_{midc} = I_{mida} + I_{midb} - I_{na} = 0 \tag{3}$$

But if phase *a* changes to *N* state suddenly, the midpoint becomes,

$$I_{mida} + I_{midb} + I_{midc} = I_{mida} + I_{midb} + I_{pa} \tag{4}$$

It means during the transient of IGBT action, the upper arm current I_{pa} should be opposite to the lower arm current I_{na}. Otherwise, sum of three-phase midpoint current is not zero and will cause voltage spike. Since each arm can be considered as a current source with individual inductor, it is very realize this requirement. Thus [30] utilizes *Z* state as a transition between *P* and *N* states to commutate the thyristors. While [32] uses similar method to realize soft-switching of IGBT stacks. However, *Z* state needs extra FB SMs to achieve current commutation between upper and lower arm, which increases semiconductor number and system volume. In this paper, two small commutation capacitors are placed across dc side to compensate upper and lower arm current difference. In this way, the *P* state can be changed to *N* state directly. Besides, it can protect the system when the IGBT firing signal is lost suddenly and the hard-switching is unavoidable.

Compared to the MMC, whose three phases are always connected in the fixed way, HMMC 1 has variable structures. Applying the working principle of phase *a* to all three phases could obtain all working states during one fundamental period, which can be divided into six segments. Then the three-phase structures in six segments are depicted in Fig. 5. It can be observed that in each segment, two phases are connected to positive (or negative) terminal in parallel to share the dc bus current. While the third phase is connected to another terminal

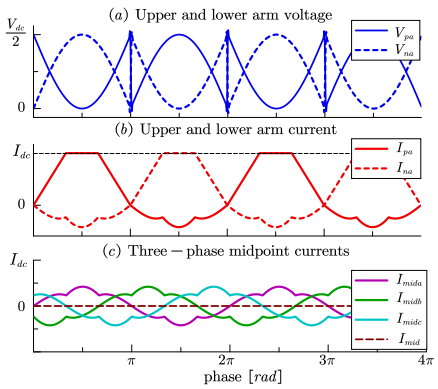
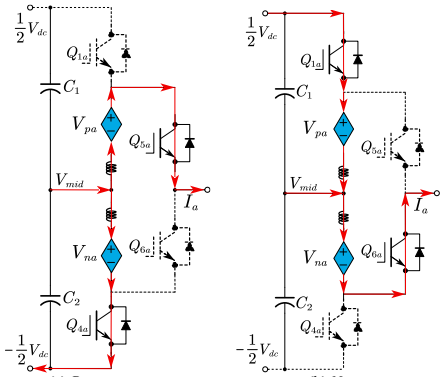
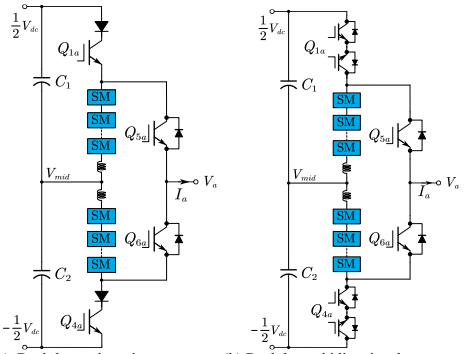


Fig. 6 HMMC 1 phase *a* arm and three-phase midpoint currents.



(a) *P* state (b) *N* state

Fig. 7 Two working states of HMMC 2.



(a) Buck-boost dc-ac inverter (b) Buck-boost bidirectional converter

Fig. 8 Buck-boost type HMMC 2.

and needs to support the whole dc bus current.

There are several methods to allocate the current between two parallel arms, which can be either half of dc bus current [30] or trapezoidal [32]. Different shape of arm current and power factor will influence the arm current RMS value. For simplicity, this paper selects a trapezoidal wave with current-overlap duration of $\pi/6$ and the expression of arm current I_{pa} is given in Appendix. If the midpoint voltage is zero, the arm waveforms of HMMC 1 could be plotted as Fig. 6. It can be observed that the maximum arm voltage is reduced by half compared to MMC. In another word, only half of SM will be needed to build HMMC 1 of same power rating, which means the power density can be increased a lot. Besides, even if SM number is reduced by half, the output voltage quality is not deteriorated with same voltage level number, because the output voltage is calculated by

$$V_a = \frac{V_{dc}}{4}\,\mathrm{sgn}(\sin(\omega t)) + \frac{1}{2}(v_{na} - v_{pa}) \tag{5}$$

where ωt is output voltage phase angle, *sgn*() represents the sign function. Due to the insertion of fundamental frequency square wave, the ac voltage level will be doubled based on the chain-link output. And the sum of three-phase midpoint currents keeps zero, which means the dc voltage ripple does not exist in theory, and the dc side capacitor could be small enough for only IGBT commutation functions. Considering the small value, it is neglected in the capacitance comparison of next section.

B. Operation Principles of HMMC 2

The IGBT stacks of HMMC 2 have a similar operation principle to minimize the arm voltage stress. Two working modes are presented as Fig. 7. When V_a is positive, Q_{4a} and Q_{5a} are turned on, Q_{1a} and Q_{6a} are turned off. This *P* state voltage is

$$\begin{aligned} V_{pa}^* &= V_a - V_{mid} \\ V_{na}^* &= \frac{1}{2}V_{dc} + V_{mid} \end{aligned} \tag{6}$$

When V_a is negative, Q_{1a} and Q_{6a} are turned on, Q_{4a} and Q_{5a} are turned off. This N state voltage is

$$\begin{aligned} V_{pa}^* &= \frac{1}{2}V_{dc} - V_{mid} \\ V_{na}^* &= V_{mid} - V_a \end{aligned} \tag{7}$$

In HMMC 1, arm voltage is always synthesized by dc and ac side voltage simultaneously. However, the arm voltage of HMMC 2 is determined by them alternately. In each phase, one arm provides the whole output ac current, while another arm should support half dc bus voltage. Therefore, dc and ac sides are totally decoupled. In another word, the limitation of modulation index no longer exists now. So if Q_{1a} and Q_{4a} are replaced by reverse-block IGBT (RB-IGBT) as Fig. 8(a), this HMMC 2 becomes a buck-boost type inverter. If they are changed to bidirectional switches as Fig. 8(b), HMMC 2 becomes directional buck-boost type converter. In addition, this kind of HMMC 2 possesses dc fault clearance capability due to the block of RB-IGBT or directional switches. Compared to the FB type MMC of same power rating, the

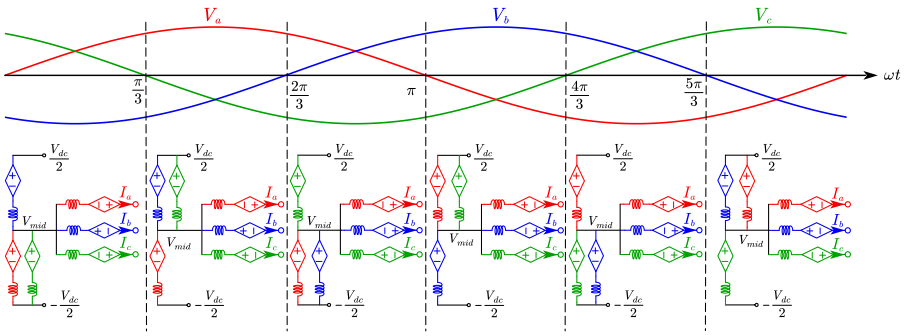


Fig. 9 Three-phase configuration of HMMC 2 during one fundamental period .

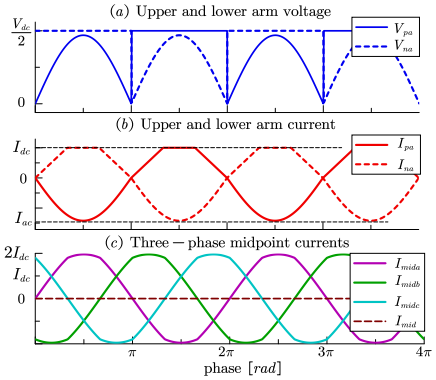


Fig. 10 HMMC 2 phase *a* arm and three-phase midpoint currents.

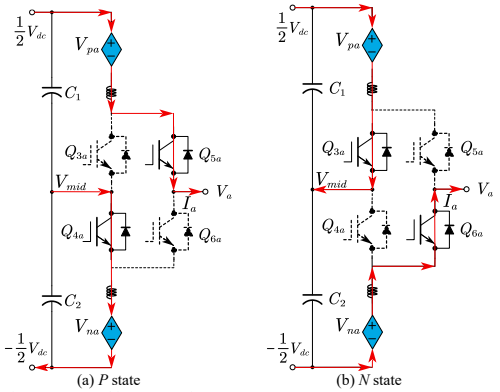


Fig. 11 Two working states of HMMC 3.

device number will be reduced further. In this paper, only HMMC 2 topology in Fig. 7 is compared with other family members and MMC in next section.

The three-phase working states of HMMC 2 are shown in Fig. 9. It can be seen that this configuration is different from the HMMC 1 with six arm always connected to the mid-point. But the common point is that there are two parallel arms to share DC bus current. Therefore, the trapezoidal waveform could still be used here to allocate current distribution. The corresponding arm waveforms are shown as Fig. 10. It should be noted that the SM number of HMMC 2 is reduced half compared to MMC, but unlike HMMC 1 its output voltage level is also reduced. So the switching frequency should be increased to guarantee same output quality.

C. Operation Principles of HMMC 3

HMMC 3 looks like AAC in [23-25], but it adds two more IGBT stacks and uses HB SMs instead of the FB SMs in AAC. The IGBT stacks of HMMC 3 acts according to the ac side voltage polarity, too. Two working states are presented in Fig. 11. Neglecting midpoint voltage, *P* and *N* state arm voltages could be derived as,

$$\begin{aligned} V_{pa}^* &= \frac{1}{2}V_{dc} - V_a, V_{na}^* = \frac{1}{2}V_{dc} + V_{mid}, (V_a > 0) \\ V_{pa}^* &= \frac{1}{2}V_{dc} - V_{mid}, V_{na}^* = \frac{1}{2}V_{dc} + V_a, (V_a < 0) \end{aligned} \tag{8}$$

Similar to HMMC 1, HMMC 3 has arm voltage determined by dc and ac voltage simultaneously during half fundamental period. Therefore, the ac voltage amplitude is still limited by the dc source.

The three-phase working states of HMMC 3 are shown in Fig. 12. Its configuration is also different from HMMC 1 and HMMC 2. Three upper arms are connected to positive bus while three lower arms are always connected to negative bus. So this configuration looks more similar to the conventional MMC. During each segment, four arm current could be determined easily. For example, when $\omega t \in [0, \pi/3)$, six arm currents should satisfy,

$$\begin{aligned} I_{pa} &= I_a, I_{pb} = I_{dc} + I_b, I_{pc} = I_c \\ I_{nb} &= -I_b, I_{na} + I_{nc} = I_{dc} + I_b \end{aligned} \tag{9}$$

A similar trapezoidal allocation could be used here to allocate the dc part I_{dc} sharing between I_{na} and I_{nc}, and an

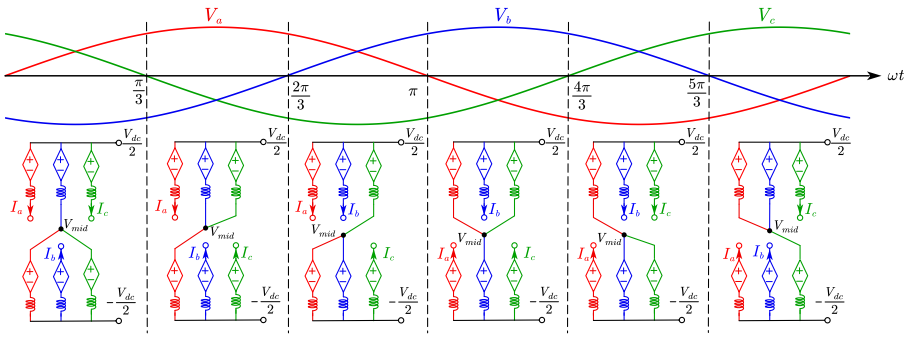


Fig. 12 Three-phase configuration of HMMC 3 during one fundamental period .

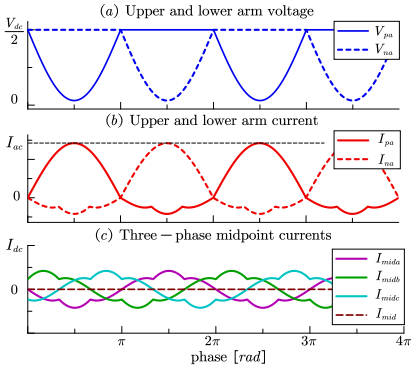


Fig. 13 HMMC 3 phase *a* arm and three-phase midpoint currents.

TABLE I
Electrical Parameters of Designed Converter

Description	Symbol	Value
Output voltage	V_{LL_rms} (kV)	6.9, 13.8 and 23
Output current	I_{ph_rms} (A)	250
Load phase angle	ϕ (rad)	$0 \sim 2\pi$
Output frequency	f_o (Hz)	60
Modulation index	M	$2/\sqrt{3}$
SM capacitor ripple	ε	10%

example of phase *a* waveforms are plotted as Fig. 13. It can be observed that HMMC 3 arm voltage is continuous instead of the discontinuous wave of HMMC 1 and 2, so the *dv/dt* should be smaller. But the voltage level of HMMC 3 is same with HMMC 2.

II. Topology Comparison

In order to identify parametric trends and strength and weaknesses of each topology, designing the converters at different operating conditions is more reasonable for a fair comparison. The design scenarios and criteria of medium voltage inverter are shown in Table I. A fundamental rms current I_{ph_rms} of 250 A with frequency of f_o=60 Hz was used, and the load phase angle was varied in the range from $0 \sim 2\pi$ to analyze all four quadrants.

TABLE II
Designed Converter's Specifications at 6.9-, 13.8- and 23- kV.

Topologies		Number of SMs Per arm	1.7 kV IGBT number	6.5 kV IGBT number	Switching frequency (Hz)
6.9 kV	MMC	10	120	--	960
	HMMC 1	5	60	12	960
	HMMC 2 & HMMC 3				1500
13.8 kV	MMC	19	228	--	480
	HMMC 1	10	120	24	480
	HMMC 2 & HMMC 3				960
23 kV	MMC	31	372	--	240
	HMMC 1	16	192	36	240
	HMMC 2 & HMMC 3				480

A. Number of Power Semiconductors

The first action is determining the magnitude of the voltage on the dc side. Voltage drops across the series inductor is neglected and the output voltage reference of phase *a* is,

$$V_a^* = M\frac{V_{dc}}{2}\sin(\omega_o t + \phi) + \frac{M}{6}\frac{V_{dc}}{2}\sin[3(\omega_o t + \phi)] \quad (10)$$

Considering the third harmonic injection with a 4% margin, the nominal dc voltage is calculated using the line-to-line voltage,

$$V_{dc} = 1.04 \times \sqrt{2}\, V_{LL\_rms} \quad (11)$$

So for three cases, the dc source voltage should be 10.15 kV, 20.3 kV and 33.8 kV, respectively. In this paper, Infineon IGBT module is used for SM power devices, which features a maximum collector-emitter voltage of 1.7 kV and continuous DC collector current of 300A. It is worth noting that 1.7 kV Si IGBT (FF300R17KE4) [34] is superior to 3.3 kV and 4.5 kV IGBT module of similar current rating, mainly due to lower switching loss. However, 6.5 kV IGBT module is better for the three-level IGBT stacks because of the low fundamental switching frequency, and a 250A Infineon module FZ250R65-KE3 [34] is selected here.

The number of SMs N in each arm is selected so that dc link capacitor voltage V_{SM}^* does not exceed 1.1 kV, which means

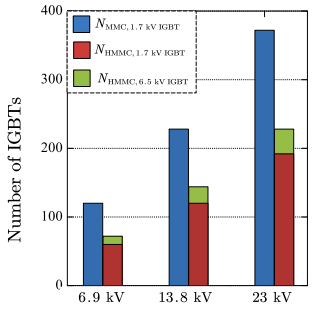


Fig. 14 Number of power semiconductors (1.6 kV and 6.5 kV IGBT) used in MMC and HMMC at different voltage ratings.

$$N_{MMC}=\frac{V_{dc}}{V_{SM}^{*}},\ N_{HMMC}=\frac{0.5V_{dc}}{V_{SM}^{*}},\ V_{SM}^{*}=1.1\mathrm{kV} \tag{12}$$

While the voltage stress for three-level IGBT stacks is $0.5V_{dc}$. Since all three HMMCs have same maximum arm voltage, the number of SM, IGBT and capacitor should be same. Then the corresponding figure of required IGBTs number at different voltage ratings are given in Fig. 14. It can be seen HMMC can save 30% device number.

The switching frequency of MMC refers to [35] as the benchmark. As explained earlier, HMMC 1 has same ac voltage level with MMC even if the SM number is reduced by half, so the switching frequency is selected the same. While the ac voltage of HMMC 2 and HMMC 3 is only synthesized by single arm, so their switching frequency should be higher to make sure the output THD is close. The related information is summarized in Tables II.

B. Capacitance Requirement

Capacitors in MMC are one of the important factors directly affecting the power density and cost. HMMC could reduce half of capacitor number successfully, but the capacitance value is still unknown. It is directly related to the energy fluctuation and limited by the capacitor voltage ripple coefficient ε, which is defined by

$$\varepsilon=V_{ripple}/2V_{SM}^{*} \tag{13}$$

Where V_{ripple} is the peak-to-peak amplitude of capacitor voltage ripple. Suppose the arm energy balancing is controlled well, then the capacitance C_{SM} could be calculated by,

$$\begin{aligned}&\frac{1}{2}C_{SM}(V_{SM}^{*}+\varepsilon V_{SM}^{*})^{2}-\frac{1}{2}C_{SM}(V_{SM}^{*}-\varepsilon V_{SM}^{*})^{2}=\frac{\Delta E}{N}\\&\Rightarrow C_{SM}=\frac{\Delta E}{2N\varepsilon V_{SM}^{*2}}\end{aligned} \tag{14}$$

Where ΔE is the maximum energy difference of each arm over one fundamental period. Multiplying voltage and current yields the arm output power, and the integration of power indicates the energy fluctuation of this arm.

$$E=\int_{0}^{\omega t}v_{pa}i_{pa} \tag{15}$$

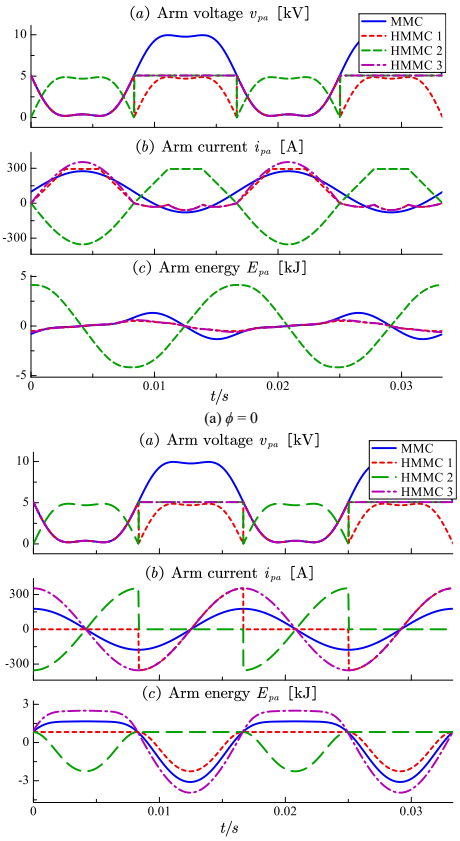


Fig. 15 Arm Waveforms of 6.9 kV MMC and three HMMC topologies at different output power factor.

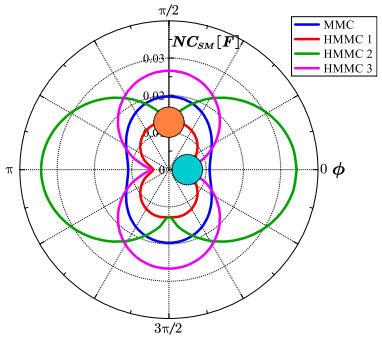


Fig. 16 Variation of arm capacitance of MMC and three HMMC topologies at different power factors.

Three HMMC topologies have different instantaneous arm power, which also varies at different power factors. Due to the symmetric characteristics of four topologies, only upper arm waveforms of phase *a* are discussed here. According to the aforementioned math expressions, arm voltage, current and energy variations of four topologies are plotted in Fig. 15. It can be seen the integration of arm power during one fundamental period is zero, which proves the natural arm energy balancing of four topologies.

If the capacitor voltage ripple coefficient ε is designed as 10%, the corresponding total capacitance in one arm NC_{SM} is calculated and plotted in Fig. 16. It can be observed the HMMC 1 has the smallest arm capacitance, which means it will possess the highest power density. And HMMC 3 has similar arm capacitance at high power factor range ($\phi \approx 0$ or π). While HMMC 2 has relative smaller arm capacitance at low power factor range ($\phi \approx \pi/2$ or $3\pi/2$).

C. Semiconductor Losses

In order to compare the converters from efficiency point of view, conduction and switching losses for semiconductors are calculated here. Considering the conductivity modulation effect in IGBT and diode, the on-state voltage drop is not linear with conducted current. Therefore, the conduction characteristics of IGBTs and diodes can be expressed as an exponential function with coefficients *a*, *b* and *c* [36], [37],

$$v = a + b \cdot i^c \tag{16}$$

Where the loss coefficients of 1.7 kV and 6.5 kV IGBT modules at junction temperature can be obtained from the IGBT module datasheet [34]. It should be noted that these coefficients are affected by temperature, and could be expressed by linear interpolation of junction temperature T_j.

$$a(T_j) = [a(125) - a(25)]\frac{(T_j - 25)}{100} + a(25) \tag{17}$$

SM conduction power loss distribution is mainly related to the operation sates and current flowing direction. Since the SM output voltage and current waveform are known, the conduction loss of one SM during one fundamental period could be derived. As shown in Fig. 17(a), the SM output voltage v_{sm} is expressed as v_{pa}/N, which means the duty-cycle of upper IGBT d_{UT} and lower IGBT d_{LT} is (neglecting capacitor voltage ripple),

$$d_{UT} = \frac{v_{SM}}{V_{SM}^*},\ d_{LT} = 1 - \frac{v_{SM}}{V_{SM}^*} \tag{18}$$

The upper arm current I_{pa} flows out of the IGBT stacks and flows in to the SM, which has four parts: the upper IGBT i_{UT} and diode i_{UD}, lower IGBT i_{LT} and diode i_{LD}. Compared to the HB SM, the three-level IGBT stacks only acts twice in a fundamental period, but the current direction also influences the conduction loss distribution. Fig. 17(b) only demonstrates the current distribution for upper arm and IGBT stacks of HMMC 1 phase *a* because all other five parts are symmetrical. It is obvious that the current distribution and power loss of IGBT and SM is unequal. For example, the conduction loss of upper IGBT in SM could be calculated by,

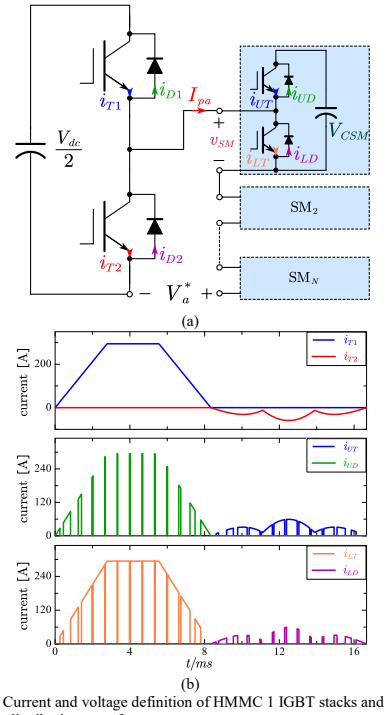


Fig. 17 (a) Current and voltage definition of HMMC 1 IGBT stacks and SM, (b) Current distribution waveforms.

$$P_{UT} = \frac{1}{T_o}\int_0^{T_o} i_{UT} \cdot v_{UT} dt = \frac{1}{T_o}\int_0^{T_o} i_{UT} \cdot (a + b \cdot {i_{UT}}^c) dt \tag{19}$$

Then the total conduction loss P_{con} can be given as,

$$\begin{aligned} P_{con} &= 6(P_{T1} + P_{D1} + P_{T2} + P_{D2}) \\ &\quad + 6N(P_{UT} + P_{UD} + P_{LT} + P_{LD}) \end{aligned} \tag{20}$$

In addition to the conduction loss, the switching loss should be calculated from the IGBT turn-on, turn-off and diode reverse recovery process. The datasheet of IGBT usually provides the turn-on and turn-off energies (E_{on} and E_{off}) curves related to the switching current at certain voltage. In practice, it can be approximated with quadratic function fitting as,

$$e_{on,off,rec} = \alpha i^2 + \beta i + \lambda \tag{21}$$

From the datasheets, the loss coefficients of 1.7 kV and 6.5 kV IGBT modules at junction temperature T_j=125°C_–are approximated. Similarly, these coefficients are related to the junction temperature T_j. Any SM operation state change corresponds to one time turn-on, turn-off loss of IGBT and reverse recovery loss of diode. Then the switching losses within one fundamental period are added together. For the three-level IGBT stacks, the action time is only twice per cycle and can be calculated in the same way.

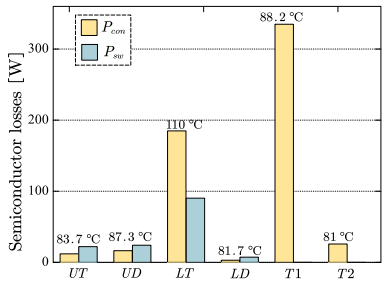


Fig. 18 Semiconductor losses distribution in HMMC 1.

$$P_{sw,SM} = \frac{\omega_o}{2\pi}\sum_{\gamma=1}^{N_{sw}}\left\{\frac{v_{CE\_on(off)}}{v_{CE,ref}}\cdot e_{on(off)}(i_C)\right\} + \frac{\omega_o}{2\pi}\sum_{\gamma=1}^{N_{sw}}\left\{\frac{v_{F\_rec}}{v_{F,ref}}\cdot e_{rec}(i_F)\right\} \tag{22}$$

In order to simulate the loss coefficients precisely, the junction temperature of the IGBTs should be calculated iteratively. And the thermal resistance of the heat-sink is selected so that its temperature T_h is kept at 80 °C. Then the precise semiconductor losses could be derived through the iterative approach at thermal steady state.

In this way, the semiconductor losses distribution of HMMC 1 at $\phi = 0$ is calculated and presented as Fig. 18. Obviously, LT takes most losses in inverter mode, and the results should be opposite in rectifier mode. Fig. 19 shows total losses variation of one arm (including IGBT stacks in HMMC) under different power factors. The conduction losses are strongly related with the arm RMS current. Benefiting from the high voltage 6.5 kV IGBT, the conduction losses of HMMC 1 are reduced a lot from MMC, especially in high power factor range. Similar to the capacitor voltage ripple tendency, HMMC 2 has smaller losses at low power factor, while HMMC 3 is more efficient under high power factor. As for switching losses, the SM switching losses are similar to guarantee same average switching frequency. While the high voltage IGBT stack switching losses are negligible at zero current crossing point at high power factor.

D. Arm Inductor and Redundant Operation

The arm inductors in HB-MMC have two functions, which can help suppress circulating current and limit the rate of rise of the current in the case of a dc-side fault [38]. The later one dominates and could be sized at 0.1 pu. Similar to the HB-MMC, HMMC 1 and 3 do not have the dc fault ride-through capability, so the arm inductor to limit fault current could follow the same design principle. While for HMMC 2, the fault current doesn't flow through the arm inductor. Then the arm inductors could be reduced to 0.02 p.u., and the topology in Fig. 8 should be used.

The redundant operation is also very important for this kind of modular topology. The series IGBT stack part can use the press-pack IGBT construction, whose short circuit failure

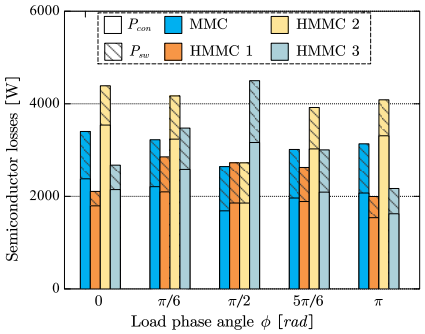


Fig. 19 Power losses per arm in four topologies.

TABLE III
Overall converter comparison between HMMC and MMC

Topology	MMC	HMMC		
		1	2	3
Device number	1 p.u.	0.5 p.u. (chain link, 1.7 kV) + 0.2 p.u. (IGBT stack, 6.5 kV)		
Capacitor	1 p.u.	0.5 p.u.	2 p.u.	0.6 p.u.
Arm current	1 p.u.	0.98 p.u.	1.48 p.u.	1.12 p.u.
Device losses	1 p.u.	0.68 p.u.	1.29 p.u.	0.85 p.u.

mode allows for the design of redundancy. And researchers from GE have proposed self-powered high voltage IGBT switch for the AAC topology, using the energy stored in a capacitive clamp snubber circuit [39]. So the series IGBTs is not a big issue in this application. As for the chain-link part, the redundant SMs in hot reserve or cold reserve operation modes have been proposed [40], [41], thus not discussed here.

Above all, the converter parameter of three HMMC topologies based on per-unit of MMC are listed in Table III. This table clearly shows that HMMC 1 has the best performance, especially under high power factor. It can save around 30% devices, 50% total capacitor and 25% power losses compared to the conventional MMC.

IV. Experimental Verification

A. Single-phase Control Scheme

The basic control scheme of MMC has been extensively explained [1-3] and will not be discussed in this paper. The structure of cascaded control strategies of HMMC is presented as the block diagram in Fig. 24. It consists of four parts, SM capacitor voltage control, current loop, arm voltage feed forward and individual SM capacitor balancing. Generally, the average and the differential voltage across the SM capacitors are regulated by two pair of PI controllers G_{ave} and G_{diff}. The former generates a dc current reference i_{dca}^* to maintain the average of SM capacitor voltage in one phase at the rated value V_{SM}^*. While the latter is employed to balance the upper and lower arm capacitor energy. Similar to MMC, HMMC 1 has continuous circulating current flowing through both upper and lower arms. So a fundamental frequency reference can be used for arm capacitor voltage balancing. However, there is no circulating current in HMMC 2 and HMMC 3 upper and lower

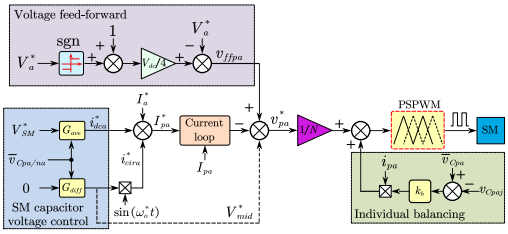


Fig. 20 Block diagram of cascaded control system for single-phase HMMC.

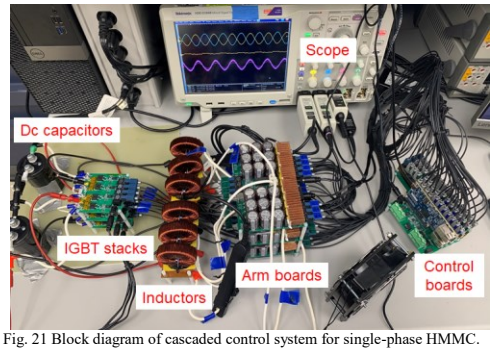


Fig. 21 Block diagram of cascaded control system for single-phase HMMC.

TABLE IV
Electrical parameters of single-phase HMMC system

Parameters	Symbol	Values
DC bus voltage	V_{dc}	400 V
AC voltage amplitude (phase)	V_o	180 V
AC voltage frequency	f_o	60 Hz
AC load	R	24 Ω
Arm inductance	L_{arm}	3 mH
Arm equivalent resistance	R_{arm}	0.02 Ω
SM voltage	V_{sm}	70 V
SM capacitance	C	1.32 mF
Number of SM per arm	N	3
Carrier (sampling) frequency	f_c	14.4 kHz

arms, because the ac output current is determined by one arm current. Therefore, the midpoint voltage V_{mid}^* is adopted here and is added to the output of current loop.

The voltage feed-forward control is added to improve the dynamic response performance. Fig. 20 only gives the v_{ffpa} block diagram of HMMC 1, but other two topologies can be derived easily from the previous operation principles. The reference of output current I_a^* is either directly given or calculated according to the output power command. It should be noted that the current loop reference I_{pa}^* is not the sum of three components I_a^*, i_{dca}^* and i_{cira}^* directly. This synthesis should use the information of working states to generate the waveforms shown in Fig. 6.

B. Experimental Results

In order to verify the effectiveness of proposed control scheme, a HMMC system with 3 HB SMs per arm was built and the electrical parameters are given in Table IV. Single-phase HMMC 1 configuration is presented in Fig. 21. HMMC 2 and 3 could be obtained easily by changing the wire connection of IGBT stacks and chain-link. The converter is controlled by a central DSP TMS320F28388d running with a sampling frequency of f_c. The SM uses 300_V MOSFET while three-level stack utilizes 450V discrete IGBT. The sampling circuit employs an 8-channel ADC to measure 6 capacitor voltages and 2 arm currents every period of T_c, and sends them back to the controller through SPI communication. Different phase offset values are assigned to the PWM registers to generate phase-shift carriers.

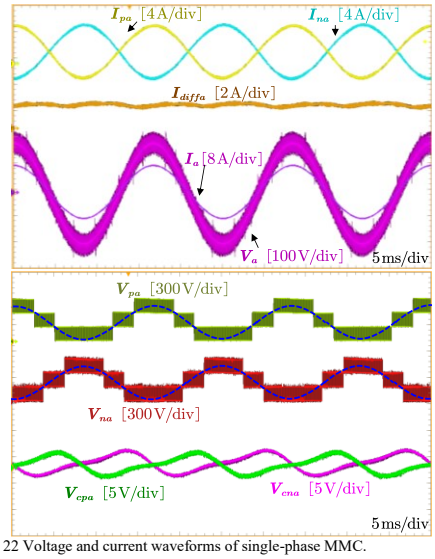


Fig. 22 Voltage and current waveforms of single-phase MMC.

The steady state waveforms of traditional HB-MMC are shown as Fig. 25. It should be noted that the dc bus input voltage of MMC is the same as HMMC, but the maximum arm voltage is twice of HMMC, which means the dc link capacitor voltage should be doubled to 140_V, so the chain-link arm voltage level number is 4. From the experimental waveforms, the differential current with dc and ac frequency components is regulated well to balance upper and lower arm capacitor voltage. Due to the limitation of scope channels, only one SM capacitor voltage from upper and lower arms is measured, and the dc bias is added to highlight the ripple amplitude. It can be seen the voltage ripple is 4 V due to higher dc link capacitor voltage.

Different load characteristics experiments are conducted to verify the effectiveness of HMMC 1. Resistive, resistive-inductive and resistive-capacitive loads are connected to the output of HMMC 1 while the output voltage amplitude are kept the same. Fig. 23(a) depicts the pure load test results, which have only half of arm voltage compared to MMC in Fig. 22. It can be seen arm currents are regulated smoothly as the reference in Fig. 6 and output current is satisfactory with low

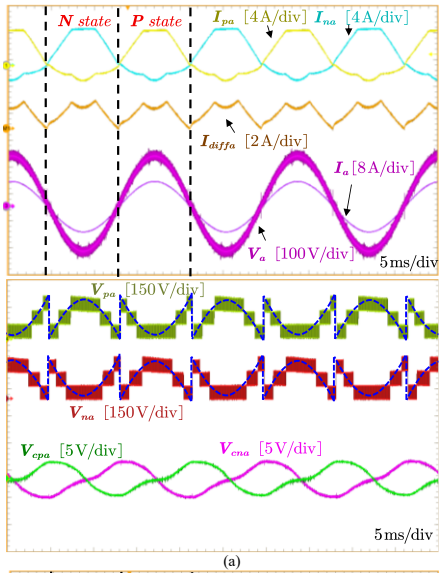


Fig. 23 Voltage and current waveforms of single-phase HMMC 1, (a) resistive load, (b) resistive-inductive load, (c) resistive–capacitive load.

THD. This phase works at *P* and *N* state alternately, so that the arm voltage stress is only half of the MMC of same dc bus voltage, which verifies the benefit of this topology. The

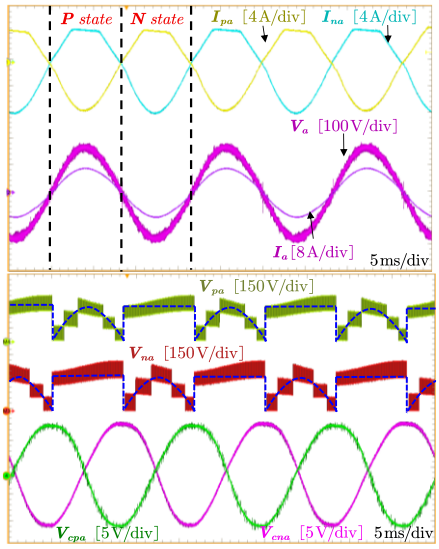


Fig. 24 Voltage and current waveforms of single-phase HMMC 2.

differential current contains not only dc component and first order harmonics but also higher order harmonics because of trapezoidal current allocation. The SM voltage ripple is 7.5 V, lager compared to MMC owing to the lower dc voltage bias based on Eq. (12). Fig. 23(b) presents the results when a 15 mH inductor is connected in series with load resistor, whose arm currents have a step in the voltage zero crossing point. Since the point overlaps with the arm voltage step, it will introduce ac output current distortion due to the arm voltage out of range. Fig. 23(c) shows the waveforms of a 100 μF capacitor paralleled with the load resistor. Similarly, there are arm current step and ac current distortion as well.

The experimental results of HMMC 2 are presented in Fig. 24. It matches the previous analysis that ~~this topologies~~this topology has the highest capacitor voltage ripple among three HMMC family members, because the capacitor keeps charging or discharging during half cycle. And it is found the current loop regulator is more difficult to design due to bigger capacitor voltage ripple. The four-level arm voltage output can also indicate the capacitor voltage variation. Due to the larger arm current accompanied with higher arm voltage, the power losses of HMMC 2 are also higher compared with HMMC 1 and 3.

The experimental results of HMMC 3 are shown in Fig. 25. Compared to last two topologies, there is no voltage step observed at the output voltage zero-crossing point, which means the high *dv/dt* can be avoided. HMMC 3 has similar arm voltage waveform to AAC, but does not have the 'sweet-spot' operation limitation. Besides, the dc bus inductor is unnecessary because the sum of three phase dc current keeps stable naturally. The SM capacitor voltage ripple magnitude is

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similar to HMMC 1. But other inductive or capacitor load experiments are omitted here.

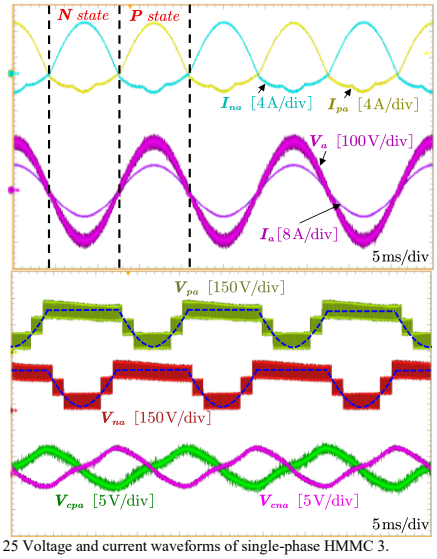

Fig. 25 Voltage and current waveforms of single-phase HMMC 3.

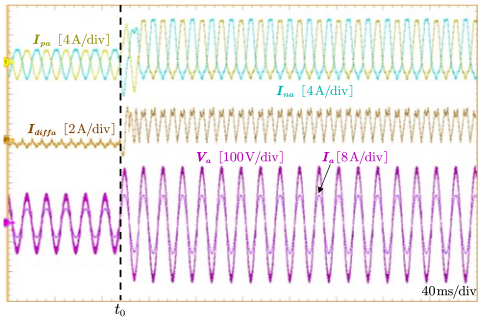

Fig. 26 Voltage and current waveforms of single-phase HMMC 1 when there is a step of output voltage reference.

In order to evaluate the dynamic response of HMMC 1, the amplitude of the output voltage reference is changed from 90 V to 180_V, and the corresponding arm waveforms are presented in Fig. 26. The differential current average value represents the dc input current, and settles at larger point after V_a^* steps. Obviously, the HMMC 1 system is stable and the response is fast due to good control parameters design.

V. Conclusion

In this paper, a family of HMMC with higher power density and efficiency is introduced. Through the combination of low speed high voltage device in three-level stacks and high speed low voltage device in SMs, three HMMC topologies with only half of arm voltage stress are derived. Since three topologies have different connection method, different arm references are used for them to make sure dc bus current is stable. In order to evaluate the performances of three HMMC topologies, several criteria including semiconductor number, capacitor size and power losses are calculated and compared comprehensively. It can be concluded that HMMC 1 possesses the superior performance among three topologies. Under high power factor, this topology can save around 30% devices, 50% total capacitor and 32% power losses compared to conventional MMC. And the output voltage quality does not have any deterioration due to same voltage level. In this way, the power density, efficiency, and construction cost could be improved a lot and HMMC will have greater potentials in various MV and HV power conversion applications.

Appendix

The trapezoidal current allocation is shown in Fig. 6, and the equation of arm current I_{pa} could be expressed as,

$$I_{pa}=\begin{cases} I_{dc}\cdot \omega t \big/ \left(\frac{\pi}{3}\right),\ \omega t\in\left[0,\frac{\pi}{3}\right) \\ I_{dc},\ \ \omega t\in\left[\frac{\pi}{3},\frac{2\pi}{3}\right) \\ I_{dc}-I_{dc}\cdot\left(\omega t-\frac{2\pi}{3}\right)\big/\left(\frac{\pi}{3}\right),\ \omega t\in\left[\frac{2\pi}{3},\pi\right) \\ I_{dc}\cdot(\omega t-\pi)\big/\left(\frac{\pi}{3}\right)+i_a,\ \omega t\in\left[\pi,\frac{4\pi}{3}\right) \\ I_{dc}+i_a,\ \omega t\in\left[\frac{4\pi}{3},\frac{5\pi}{3}\right) \\ I_{dc}-I_{dc}\cdot\left(\omega t-\frac{5\pi}{3}\right)\big/\left(\frac{\pi}{3}\right)+i_a,\ \omega t\in\left[\frac{5\pi}{3},2\pi\right) \end{cases} \tag{1}$$

Similar formula could be derived easily for HMMC 2 and HMMC 3.

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