Performance Evaluation and Analysis for Resonant Switched Capacitor Converter

2021 IEEE Applied Power Electronics Conference and Exposition (APEC) | 978-1-7281-8949-9/21/$31.00 ©2021 IEEE | DOI: 10.1109/APEC42165.2021.9487181

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***Abstract*— In this paper, a new method helps compare and analysis different topology is proposed. Also, a new method that can analyze and derive the minimum device power loss for the resonant switched capacitor topology is developed. By applying total semiconductor power loss index (TSLI), the optimum total die size needed for the specific topology with fixed power level and switching frequency can be calculated. Thus, the minimum device power loss can be reached at same time. Besides, TSLI can also help to determine which topology has a lower semiconductor device power loss when operating under same condition.**

Keywords*— *Switched-capacitor converter, Die area, Figure of Merit, Topology comparison, Power loss analysis

I. Introduction

Resonant switched capacitor converters have received more attention due to the high power density and efficiency compared with the traditional approaches. Different topologies will use various voltage ratings device and operating at different optimized output power. Thus, it is important to evaluate these topologies deliberately. In [1], VA rating comparison which using the product of the average current flows through the device and the maximum voltage across it as the indicator for the converter device power loss index. The comparison is not considering the gate drive loss and the output capacitance loss. Besides the VA rating is not accurately shows the conduction loss. A new Figure-of Merit of multi-level converter properties is proposed in [2]. The power loss analysis is based on bridge-leg. However only the switching loss and conduction loss are included. In [3] the FoM based loss analysis for choosing the most appropriate GaN device is demonstrated. But the method is limited only to the device level selection. PDFOM is proposed in [4] for selecting the better device to achieve a better converter power density. However, the effect factors could be further reduced. [5]-[7] mention another resonant and soft-switching Figure-of Merit, however it is simplified to converter ZVS operation using GaN device.

In this paper, a new method which composed by the total device power rating (TDPR) and the total semiconductor power loss index (TSLI). TDPR is proposed in [8]-[10]. It is offering a more direct and instantons method to compare different topology. TSLI is proposed to reflect the relationship between converter device power loss and the total device die area. By utilizing TSLI, the best operating total die size of converter can be derived. This can achieve lowest device power lost under the fixed operating power and frequency. The theoretical derived process of TSLI is shown in the next section followed by the real application case and test result verification.

II. Proposed Converter Evaluation Method

Fig. 1 shows the proposed method mechanism. When comparing different topologies, the first step is deriving the TDPR. This is a faster topology evaluation method than TSLI. If TDPR can differentiate the topologies and no device selection is need, then the topology comparison is finished. However, if the TDPR gives the same result for different topologies or the device selection is needed, then the calculation of TSDL is required. This can help figure out which is the appropriate topology for certain application.

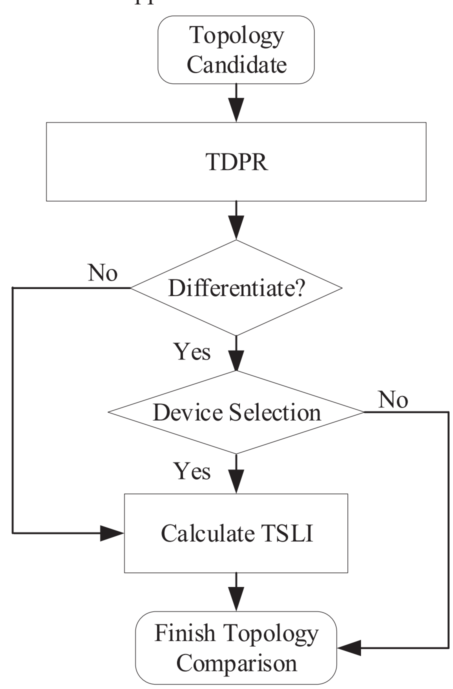

Fig. 1: Proposed topology comparison method

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A. Total Device Power Rating(TDPR)

Total device rating is first proposed in [11]. The device rating is defined as the device voltage stress times the device current stress. By adding up all device rating, the total device rating for the converter is derived. TDPR is the proposed in [8]-[10]. It is defined as the product of the device voltage stress and the average current flowing through the device. In this paper, a normalized value is adopted by using the converter output power. The TDPR can be calculated using (1) where P_o is the converter output power, N is the total number of devices, V_i is the voltage stress of the *i*-th device and the I_{avg_i} is the average current flow though the *i*-th device.

$$\mathrm{TDPR} = \frac{1}{\mathrm{P_o}}\sum_{i=1}^{N} \mathrm{V_i I_{avg\_i}} \tag{1}$$

B. Total power loss index (TSLI)

Total power loss index (TSLI) is first proposed in [12] to describe the relationship between the device power loss and the total the area usage. By reaching the minimum TSLI, the optimized semiconductor device die area usage of the topology operating under certain condition can be achieved. Since most of the resonant switched capacitor converter can achieve ZCS operation, the power loss on the device is consist of conduction loss, gate drive loss and the output capacitor loss. TSLI is derived based on these losses.

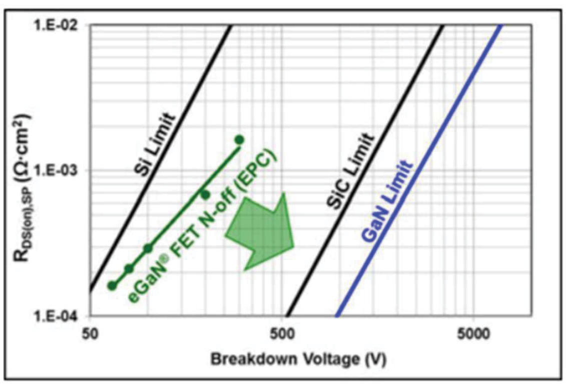

Fig. 2: On-resistance times die area versus breakdown voltage

To generate the connection between the device power loss and the die area, the production of on-resistance $R_{ds(on)}$ and die area A_{die} is used. It is an index that company use to reflect the device technology [5].It is the similar definition of B-FOM [13]. Fig. 1 [5] shows the theoretical limit of $R_{ds(on)}{\cdot}A_{die}$ versus breakdown voltage V_B for Si, SiC and GaN. Also, the relationship for current EPC eGaNFET $R_{ds(on)}{\cdot}A_{die}$ versus breakdown voltage V_B is demonstrated. Based on the curves, the theoretical Si and GaN limits and current EPC eGaNFET properties are presented in Eq. (1), (2) and (3), respectively.

$$R_{ds(on)} \cdot A_{die} = 1 \times 10^{-5} \cdot (V_B)^2 \tag{2}$$
$$R_{ds(on)} \cdot A_{die} = 3 \times 10^{-7} \cdot (V_B)^{1.983} \tag{3}$$
$$\mathrm{R_{ds(on)} \cdot A_{die}} = 3 \times 10^{-6} \cdot (\mathrm{V_B})^2 \tag{4}$$

Thus, the general relationship of $R_{ds(on)}$ and A_{die} can represent in Eq. (4) where k is the constant corresponding to different semiconductor material and X is an exponent that close to 2. The unit for $R_{ds(on)}{\cdot}A_{die}$ is $\Omega \cdot mm^2$ and V_B is V. In this way, the $R_{ds(on)}$ could be represented by Eq. (5).

$$\mathrm{R_{ds(on)} \cdot A_{die}} = \alpha(\mathrm{k, V_B}) = \mathrm{k} \cdot (\mathrm{V_B})^{\mathrm{X}} \tag{5}$$
$$\mathrm{R_{ds(on)}} = \frac{\mathrm{k}\cdot(\mathrm{V_B})^2}{\mathrm{A_{die}}} \tag{6}$$

Therefore, the device conduction loss P_{cond} can be defined by the device die area A_{die} using Eq. (6), I_{RMS_S} is the switch RMS current. It is related to the converter operating condition.

$$\mathrm{P_{cond}} = \left(\mathrm{I_{RMS\_S}}\right)^2 \cdot \mathrm{R_{ds(on)}} = \left(\mathrm{I_{RMS\_S}}\right)^2 \cdot \frac{\alpha(\mathrm{k,V_B})}{\mathrm{A_{die}}} \tag{7}$$

In [14], the new device FOM is proposed to describe the relationship between $R_{ds(on)}$ and Q_g for different manufacturer technologies and it is shown in Eq. (7). Then, the device gate drive loss P_{gate} can be defined by the device die area A_{die} using Eq. (8), V_{gs} is gate-source voltage and f_s is the switching frequency.

$$\mathrm{HDFOM} = \sqrt{\mathrm{R_{ds(on)} \cdot Q_g}} \tag{8}$$
$$\mathrm{P_{gate}} = \mathrm{Q_g \cdot f_s \cdot V_{gs}} = \frac{\mathrm{A_{die}}\cdot(\mathrm{HDFOM})^2}{\mathrm{k}\cdot(\mathrm{V_B})^2} \cdot \mathrm{f_s \cdot V_{gs}} \tag{9}$$

Fig.3 [7] shows the simplified version of HDFOM for the EPC GaNFET and the state of art Si MOSFET. It displays the relationship between the HDFOM^2 and half of the blocking voltage with 20A rated current.

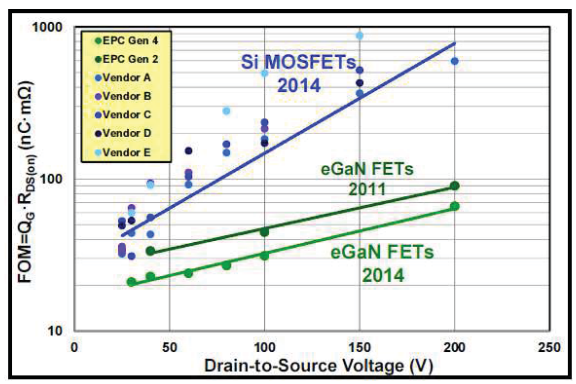

Fig. 3: Simplified HDFOM vs half of blocking voltage

In [15], another device FOM is proposed to describe the relationship between $R_{ds(on)}$ and C_{oss} with certain manufacturer technologies and it is shown in Eq. (9). The device output capacitance loss P_{coss} and the device die area A_{die} can be defined by using Eq. (10), V_{ds} is device voltage stress and assume is the half of the V_B.

$$\mathrm{P_{Coss}} = \mathrm{C_{oss} \cdot f_s \cdot V_{ds}^2} = \frac{\mathrm{A_{die}}\cdot}{\mathrm{NHFFOM}\cdot\mathrm{k}\cdot(\mathrm{V_B})^2} \cdot \mathrm{f_s} \cdot (0.5\mathrm{V_B})^2 \tag{10}$$

For the specific device operating in ZCS mode, the power loss will be

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$$P_{loss} = P_{cond} + P_{gate} + P_{Coss} \quad (11)$$

To make a reasonable analysis, in one converter assuming all device is using same manufacture technology. Different voltage stress device will have the same property in terms of power loss, which means the power loss per unit area should be the same. We define τ as the power loss per unit area, then as shown in Eq. (12)

$$\tau = P_{loss}/A_{die} = (P_{cond} + P_{gate} + P_{Coss})/A_{die}$$
$$= \left(I_{RMS\_S}\right)^2 \cdot \frac{\alpha(k,V_B)}{{A_{die}}^2} + \frac{(HDFOM)^2}{k\cdot(V_B)^2} \cdot f_s \cdot + \cdot$$
$$\frac{1\cdot}{NHFFOM\cdot k\cdot(V_B)^2} \cdot f_s \cdot (0.5V_B)^2 \cdot \quad (12)$$

For one topology working under the certain condition, when all device using the same manufacturer technologies, the relationship between the die area A_{die} and the device voltage stress V_{ds} can be derived, as shown in Eq. (13). Assuming V_{ds} is the half of the $V_{B.}$

$$A_{die} = \beta(V_B) \quad (13)$$

Therefore, for a specific switched capacitor topology, if the operation condition is fixed, the TSLI is the normalized power loss for every switching device and it can be generated as Eq. (14), N is the number of switching device.

$$TSLI = \quad (14)$$
$$\frac{1}{P_o}\sum_{i=1}^{N}(P_{cond}\{\beta(V_B)\} + P_{gate}\{\beta(V_B)\} + P_{Coss}\{\beta(V_B)\})$$

Thus, the most optimized total device die area with the minimum power loss can be derived when the $\frac{dTSLI}{dA_{die}} = 0$. The optimized $A_{die\_optimized}$ is shown as Eq. (15)

$$A_{die\_optimized} = \quad (15)$$
$$\sqrt{\frac{HDFOM^2 f_s V_{gs}/(V_B)^X + f_s/4NHFFOM\cdot k\cdot(V_B)^{X\text{-}2}}{I_{RMS\_S}{*}k\cdot(V_B)^X}}$$

As analyzed above, TSLI is related to the output power, switching frequency, conversion ratio and the device manufacture technology. For one fixed topology, when the output power, switching frequency and conversion ratio are fixed, theoretically it is possible to derive an optimized total die area to achieve the minimized total device power loss with the certain device manufacture technology. In other words, for different topologies, assuming using the same device manufacture technology, when the total device power loss is the under same operating conditions, the one with smaller total die area can achieve more efficient die utilization and potentially lower device manufacturing costs.

Besides, TSLI can also be used to figure out the minimum device power loss operating frequency when the converter operating power conversion ratio is fixed. Similarly, the best operating conversion ratio can also be derived when the converter is working under certain frequency and power. These two different evaluation perspectives based on the above TSLI parameter can provide more comprehensive understandings for switch capacitor topologies to achieve smallest total device power loss with an optimized total semiconductor die area.

III. Application Examples

A. Total Device Power Rating Application

The TDPR is derive for buck, flying capacitor, ZCS-series parallel [16], cascaded voltage divider (CVD) [17], switch-tank converter (STC) [18], switch-tank modular converter (STM) [19] and multilevel modular switched-capacitor resonant converter (MMSCRC) [20] topology with 2X,4X,6X and 8X. All the converters operate with the 48V input voltage, 250kHz and 480W condition.

As shown in the Fig3. The TDPR for the flying capacitor and the buck is the same. TDPR cannot differentiate the two topologies. Similarly, the STC, STM and the MMSCRC also have the same TDPR. In this case, TSLI should be used as the

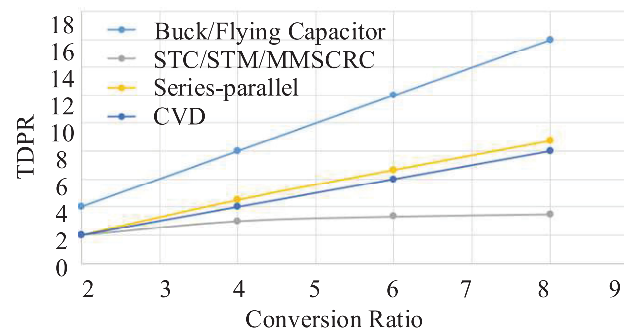

Fig. 3: TDPR vs converter conversion ratio

comparison method. And with the increase of the conversion ratio, the TDPR of the STC increment is the smallest. This is indicating that STC will be a better choice.

B. Total power loss index (TSLI) Application

Five types of switch capacitor resonant convert: ZCS-series-parallel, STC, CVD, MMSCRC and STM are selected to verify TSLI. The converter topology is shown in Fig. 4, Fig. 5 Fig. 6, Fig.7 and Fig.8 respectively. All converters are operating at 480W,48V-12V and 250kHz.ZCS is achieved for all converters.

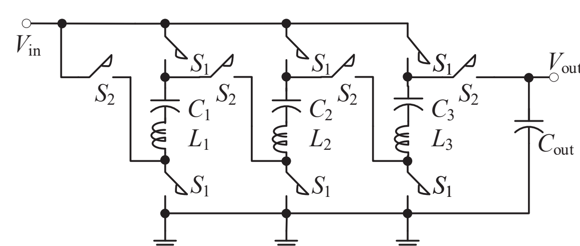

Fig. 4: 4 to 1 series-parallel converter

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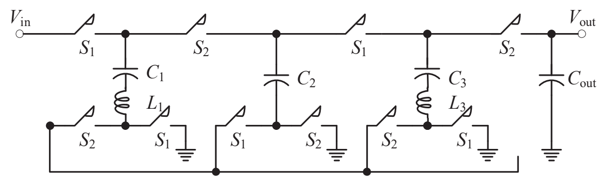

Fig. 5: 4 to 1 STC converter

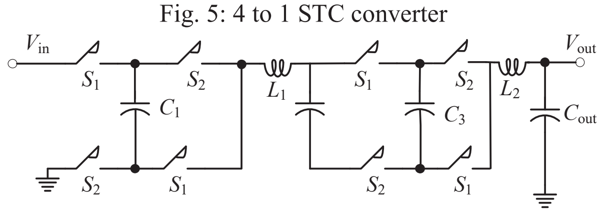

Fig. 6: 4 to 1 cascaded voltage divider converter

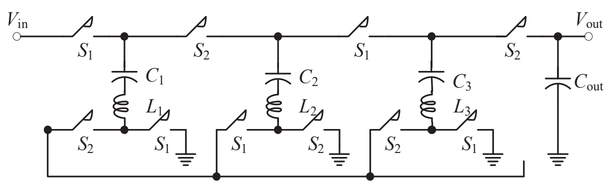

Fig. 7: 4 to 1 MMSCRC converter

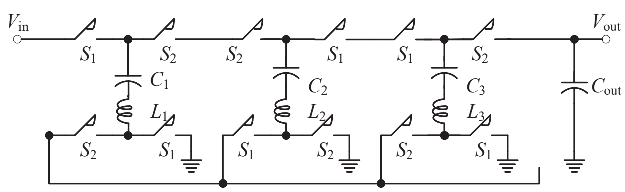

Fig. 8: 4 to 1 STM converter

Fig.9 is obtained from Infineon OptiMOS 5 series and EPC GaNFET. It shows the relationship between the NHFFOM and the device blocking voltage and the following analysis is based on it.

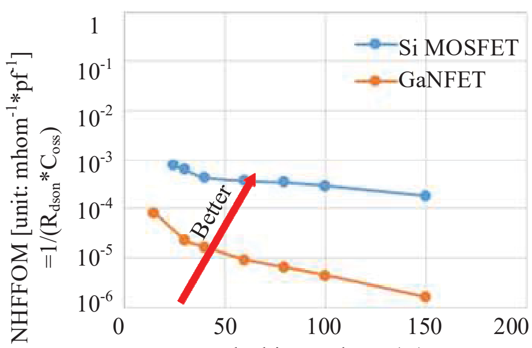

Fig. 9: NHFFOM for OptiMOS 5 and eGaNFET

Fig.10 shows the trend for TSLI regarding total device die area for STC, MMSCRC, series-parallel, CVD and STM converter when following the ideal Si device properties described in Eq. (2). As shown in the figure, under the given operating conditions, when using the ideal Si devices, the STC and MMSCRC have the smallest TSLI when total die area is less than 220mm^2. This indicates the better device power loss performance and less device power loss. When the total device die area is larger than 220mm^2, the STM will have a better performance. Besides, when the total semiconductor device die area is around 170 mm^2, the STC and MMSCRC convert will have the best performance in terms of device power loss. The STM convert best operating point occurs when total die area is

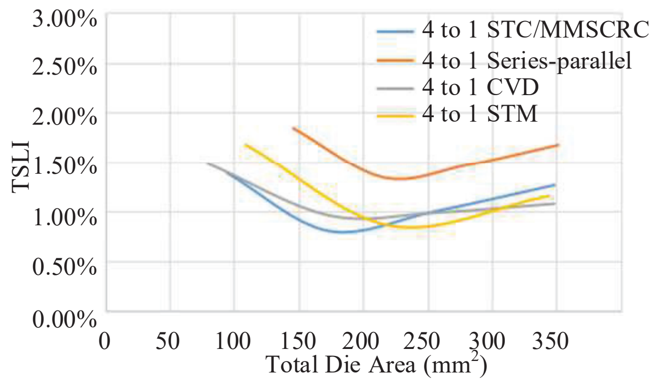

Fig. 10: TSLI vs total die area for ideal Si device

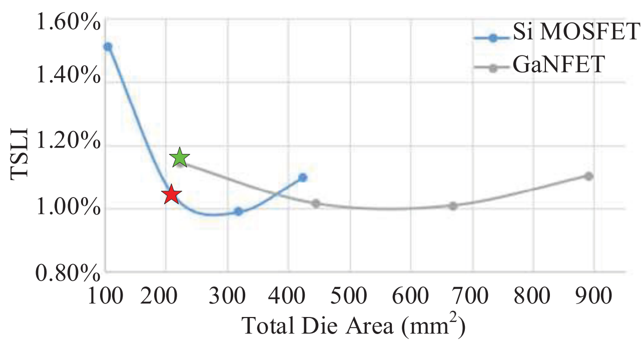

Fig. 11: TSLI vs total die area for 6 to 1 STC

around 240 mm^2. The CVD converter most optimized total die area occurs at around 200mm^2. For series parallel around 225 mm^2 is the best operation point.

The example of using TSLI to find the topology best die area usage with fixed operation condition is shown in Fig.11. The design target is to design a 6 to 1 STC with 330 kHz, 600W. The figure is generated based on the real device information. Using the Infineon BSZ013NE2LS5I datasheet as the Si device technology reference and the EPC2023 as the GaNFET technology reference. Assuming the device HDFOM and NHFFOM is a fixed number if the same device technology is used. Also, the $R_{ds(on)}$ consider to be a positive correlation with the V_{ds} and a negative correlation to the A_{die}. The device information under the design criteria for the analysis is shown in Table I.

TABLE I. DEVICE INFORMATION

Part#	*A_{die}(mm^2)*	*R_{dson}(mhom)*	*Q_g(nC)*	*Coss(nF)*
BSZ013NE2LS5I	6.6	1.25	18	1.2
EPC2023	13.92	1.45	19	1.53

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Based on the figure cand the table, several conclusions can be drawn:

- For the given operating condition and the device technology, the best operating point for the Si device converter occurs when total die area is 350mm^2 and for the GaNFET, the optimized total die area is around 550mm$^{2.}$
- The Si device will only have better performance than GaNFET when the total die area is between 250~450mm^2.
- TSLI can also help to decide whether the interleaved version should be adopted. It is possible that the interleaved version converter with larger total die area is closer to the $A_{die\_optimized}$ point, which means it will have less power loss.

Si version prototype is built as shown in Fig.12. The equivalent operating point of the prototype is the red star in Fig.11. It is a 2-phase interleaved version design, and the equivalent total die area is 211.1 mm^2. It is not reaching the best operating point since considering the device count has to be integer and a 3-phase design will pass the best operating point. Passing the best operating point will lead to the cost increasing and the decrease of the converter power density.

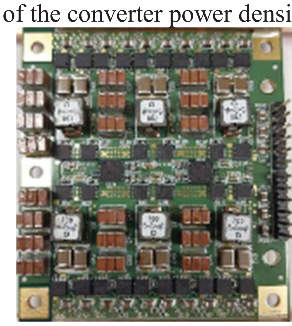

Fig. 12: 6 to 1 Si prototype

A GaNFET version prototype is also developed. It is a single-phase design, and the total die area is 222.72mm^2, the green star in Fig.9. The converter will have less power loss if a 2-phase design is adopted.

IV. Conclusion

In this paper, a new method to evaluate and compare different topologies is described. It combines the TDPR and TSLI and provide different path for different level of comparison. Also, TSLI is discussed in this paper. It is a tool for selecting proper topology for certain application. Besides, it can be used as a most suitable device selection tool for certain topology under given operation condition. Moreover, design the converter total die area by approaching the optimized values from the left, the best total die area of the converter is achieved. This can help decide the number of interleaving phases of the design converter.

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