

A 60-GHz Digital Sub-Sampling Integer-N Phase-Locked Loop

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Abstract—Digital phase-locked loops (DPLL) are finding new applications in highly demanding contexts such as frequency synthesis for millimeter-wave (mm-wave) communications and clock generation for ultra-high-speed wireline transceivers. In a typical DPLL, however, a time-to-digital converter (TDC) with fine time resolution, high linearity and high dynamic range is required to meet stringent noise and spur performance requirements, which negatively impacts the power consumption in a DPLL. A bang-bang phase-detector (BPD) outperforms a multi-bit TDC in terms of its' jitter-power tradeoff, but its' highly non-linear phase detection characteristic limits the locking speed of the loop. This research explores the design of a 60 GHz digital sub-sampling phase-locked loop that uses a BBPD loop for frequency tracking and a coarse TDC loop for fast frequency acquisition. A prototype of the DPLL is designed in a 28-nm CMOS technology and extensive simulation results are provided.

Keywords—Digital phase-locked loop, bang-bang phase-detector, time-to-digital converter, frequency divider, DCO.

I. INTRODUCTION

Recent rapid growth in mm-wave wireless local/personal area networks and 5G cellular communications at several frequency bands including 28, 36, 45, 60, 73, and 79 GHz raises new challenges in the design of frequency synthesizers [1]. All digital phase-locked loops (ADPLLs) are emerging as attractive alternatives to their analog counterparts. One key advantage of ADPLLs is their scalability with process changes or shrinks due to the lack of charge pumps and analog filters. In addition, digital calibration algorithms are naturally easier to implement in ADPLLs. However, the main bottleneck of ADPLLs is the need for a time-to-digital converter (TDC) with high time resolution, high linearity and high dynamic range. Effectively, the TDC serves as a replacement for the phase detector in an analog PLL. Such stringent specifications require complicated and power hungry TDCs.

Another direction in implementing of ADPLLs is the adoption of a 1-bit TDC, also referred to as a bang-bang phase detector or a binary phase detector (BPD) [2]. Due to its simple implementation, as shown in [3], BPD can possibly improve the jitter-power trade-off of ADPLLs. While the BPDs can provide more information to speed up locking procedure in analog PLLs, the locking is much slower in all-digital synthesizers which is a results because only the sign of phase error is provided.

The phase noise of PLL can be divided into two parts: the digital-controlled oscillator (DCO) usually dominates out-of-band noise, while the reference clock, phase detector and frequency divider dominate the in-band noise. To achieve minimum output jitter, the loop bandwidth is chosen equal to the intersection frequency of oscillator phase noise and the amplified in-band noise [4], which means the two types of noise contribute equally to the output jitter. Aiming at reducing the in-band noise, a sub-sampling [5] technique is proposed to improve the loop gain by feeding back the oscillator's outputs directly to the phase detector without using a divider in the core loop. An auxiliary loop is usually required to guarantee correct frequency is locked onto since the sub-sampling loop can lock to any harmonics of reference clock.

In the USA, 27.5–28.35 GHz is one of the bands of significant interest for 5G systems [6], and in order to avoid the injection pulling and to ease the generation of quadrature phases, the on-chip oscillator might operate at twice the frequency of the transceiver, so we choose 60 GHz as our target frequency. At this frequency range, the required RMS jitter is usually less than 0.5ps [7], thus implementing a TDC would be challenging because a TDC with a high resolution (e.g. resolution < 1ps) will be susceptible to process variations since 1ps delay is much less than the fanout-of-4 delay of modern CMOS technologies.

A recent work proposed an architecture which combines a BPD loop with a coarse TDC loop operating at 30 GHz [8]. Inspired by this work, we further investigate the feasibility of this architecture operating at 60 GHz in a 28nm CMOS technology. Simulation results indicate that the DCO can achieve 10% tuning range (57.51 GHz to 63.57 GHz). The overall system draws 20.55 mA from 1V supply.

This paper is organized as follows. Section II presents this synthesizer's architecture and behavioral simulation. Section III shows the circuit design. Section IV describes the simulation results, while Section V concludes this paper.

II. ARCHITECTURE AND SPECIFICATIONS

A. Architecture

Fig. 1 depicts the architecture of our frequency synthesizer. The blue curve is the TDC-loop, which is designed for frequency acquisition, while the black curve represents the sub-sampling

BPD-loop for frequency tracking. A key advantage of this combination is that only a coarse TDC required. Once the time error between DCO and reference clock is small (i.e. less than TDC resolution in here), the TDC stops toggling and the bang-bang loop takes charge of locking. The proportional path of Digital Filter #1 is connected to the DCO's varactor directly without additional delay. The integral path of digital Filter #1 passes a second order Delta-sigma modulator and a 4-bit DAC to tune the capacitor array of DCO. The output of digital Filter #2 is the summation of proportional path and integral path with one delay, and this output also controls a capacitor array in DCO.

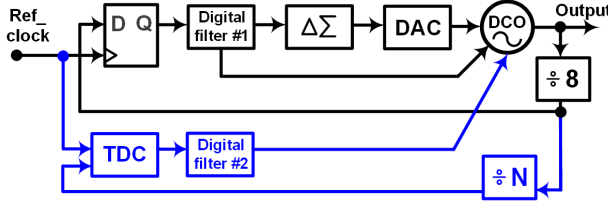


Fig. 1. System level representation of the designed PLL

B. Behavioral Simulation

The design procedure is based on a bilinear transformation for the TDC-loop as proposed in [9]. In brief, this design method is based on the analogy between an analog charge pump PLL and a digital PLL. Since the TDC-loop is responsible for coarse frequency tuning, we choose $K_{DCO} = 100$ MHz/LSB, and TDC resolution $\Delta_{TDC} = 0.5$ ns. The loop latency is induced by the digital filter #2. The closed-loop response is shown in Fig. 2.

The transfer function for digital filter #2 is $H_2(z) = (\alpha/(1-z^{-1}) + \beta) z^{-1}$. For practical implementation, we chose to round the coefficients of the digital filters to be represented in 2^n format with $n = 16$ unsigned bits. In this paper, by using $\alpha = 8$, $\beta = 64$, we can achieve a 10.6 MHz closed-loop bandwidth with 51 degree phase margin, where α is the coefficient of integral path of filter #2 and β is the coefficient of proportional path of filter #2. In addition, we make those values programmable with 2^{-1} resolution step by using shift left / shift right operations.

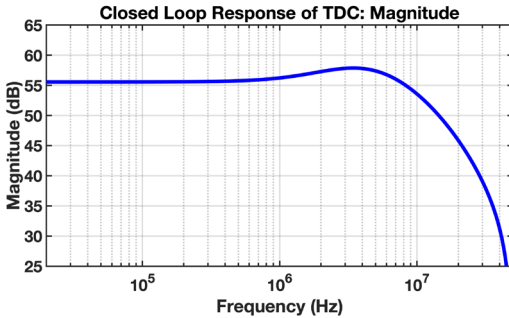


Fig. 2. Behavioral simulation for TDC-loop with loop latency = z^{-1}

The design of BPD-loop is more complicated because the gain of bang-bang phase detector is inversely proportional to the magnitude of the rms jitter at its input [10]. A closed-form gain of BPD is derived in [11] based on the time-series methodology, but that expression is too complicated to provide

intuition for loop design. In this design, we used a simpler expression from [12] to calculate loop parameters.

$$\text{Jitter}_{\text{opt}} \approx 1.1547 \times (1+D) \times (N \times \beta \times K_T) \quad (1)$$

The minimum output jitter is given in (1), where D is the loop latency, N is the division ratio of the loop, β is the coefficient of the proportional path of the loop filter, K_T is the DCO resolution which is given by $(1/f_{DCO})K_{DCO}$, the unit of K_{DCO} is kHz/LSB.

The transfer function for filter #1 is $H_1(z) = \beta + (\alpha z^{-1}/(1-z^{-1}))$. It is convenient to pick $\alpha = 0.5$ for filter #1 because the minimum variation of the DCO period is $2\alpha K_T$. Then if we set phase margin to 60 degree and assume the loop has one loop latency, then the optimal β which minimizes the output jitter is 8 [12]. Fig. 3 plots the DCO granularity we need to reduce the jitter. Here we intend to achieve 100 kHz/LSB so that the optimal jitter of the loop can be less than 400 fs.

Fig. 4 plots the output phase noise of the bang-bang PLL. In clock generation applications, usually the DCO is the dominant noise source; therefore, we assumed the reference clock has -130 dBc/Hz white phase noise, then we try to sweep the jitter from DCO, and Fig. 4 shows that to achieve -100 dBc/Hz at 1 MHz offset, the cycle jitter of the free running DCO should be less than 2 ps. If the reference clock is the dominant source, e.g. in clock and data recovery circuits, the model in [12] does not hold because the white noise assumption for input signal is not true, Markov Chains-Based time model is used to analyze this case [10].

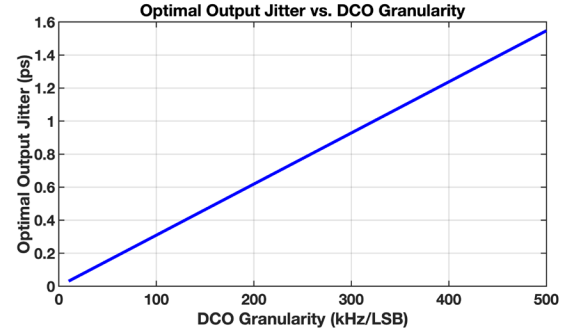


Fig. 3. Optimal output jitter of BPD-loop versus DCO granularity

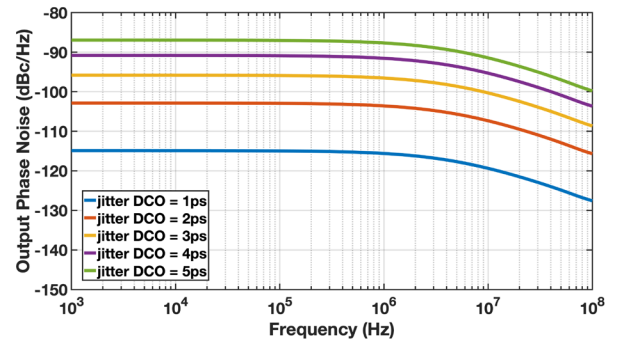


Fig. 4. Output phase noise of BPD-loop versus DCO jitter

III. CIRCUIT DESIGN

The key blocks of this design are the divider, the digital filter, the TDC and the digital-controlled oscillator (DCO). In this section, we will go over these blocks.

A. Divider

Current mode logic (CML) is employed to perform ultra-high-speed frequency division, which is the $\div 8$ block in Fig. 1. This divider is added to reduce the sub-sampling ratio so that the BPD-loop can lock easier. The first stage consumes most of the power in this divider because it handles the highest frequency (60 GHz). Following stages can be scaled down to save power. The jitter accumulation is the fundamental disadvantage of asynchronous dividers, but it can be easily overcome by adding a synchronizing flip-flop at the end of the chain [13]. In this case, the output jitter is only the one generated by the last synchronizer. The signal swing of CML stages is around 300mV, and the power consumption of all three stages is 5.39mW.

The feedback divider that allows unity steps in the modulus is usually implemented by pulse swallowing divider [14]. Basically, the $\div 2/3$ and $\div 2$ form a $\div N/(N+1)$ prescaler ($N=4$ here) and it counts by $N+1$ input cycles, gives one pulse to swallow counter $\div S$. The $\div S$ then changes the modulus control of prescaler to N . At last, the fixed modulus counter $\div P$ counts $P \cdot S$ input cycles before resetting $\div S$. Overall, this divider provides a divide ratio of $(NP+S)$. Caution must be paid to the critical timing path. When the $\div 5$ operation of the prescaler is finished, the divider would have at most three input cycles to change modulus to four. An addition pipelining stage could be added to relax this constraint if necessary [15].

Since we are using 100 MHz reference clock with 60 GHz DCO, here we choose $N = 4$, $P = 17$, $S = 1 \sim 15$. Thanks to the high speed of 28nm process, we are able to synthesize this divider with standard digital cells, this significantly reduces its power consumption to 0.65 mW.

Before connecting to the CML $\div 8$ divider, we add one CML-to-CMOS stage to convert the voltage levels, and one differential-to-single stage. The CML-to-CMOS is simply an inverter with AC-coupling and a resistor connecting its output to input. The differential-to-single stage is a differential pair loaded by a current mirror.

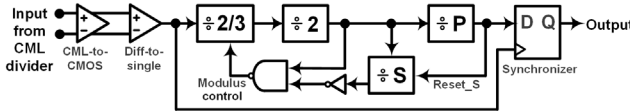


Fig. 5. Pulse swallow divider

B. Digital Filters

Two different digital filters are used in this design; Filter #1 and Filter #2 as shown in Fig. 1. It has been shown that increasing the loop latency by one clock cycle increases the output jitter by a factor ranging from 10% to 100% when the loop gain varies between 0.1 and 0.8 [16]. Also, loop stability is compromised if more delays are added to the loop. For the TDC-loop, the retiming stage is necessary because glitches generated by an 8-bit or 16-bit adder can significantly disturb the DCO.

This is not true for BPD-loop since the BPD only has 1 bit, thus the proportional path does not require the retiming stage.

C. Time-to-Digital Converter (TDC)

Since only a coarse TDC is needed, a classic delay-line topology (Fig. 6) was chosen. It should be pointed out that if we only use one delay line, then the output will always be zero as long as V_2 leads V_1 , as shown in Fig. 7 (b). A typical method to avoid this zero-gain issue is to use two TDCs. A mid-tread quantization is preferred because the TDC-loop is supposed to stay in quite when the phase error is small. A 3-bit TDC with resolution $\Delta T_{TDC} = 0.5$ ns is picked here. The delay elements are implemented as inverters with a capacitor load. Monte Carlo simulation is performed to make sure more than 90% of the delays of samples lie within 0.5 ± 0.025 ns.

For the sampling flipflops, we exploit the StrongArm latch [17] for its simple structure. Synthesized digital circuit performs bubble correction and binary code conversion.

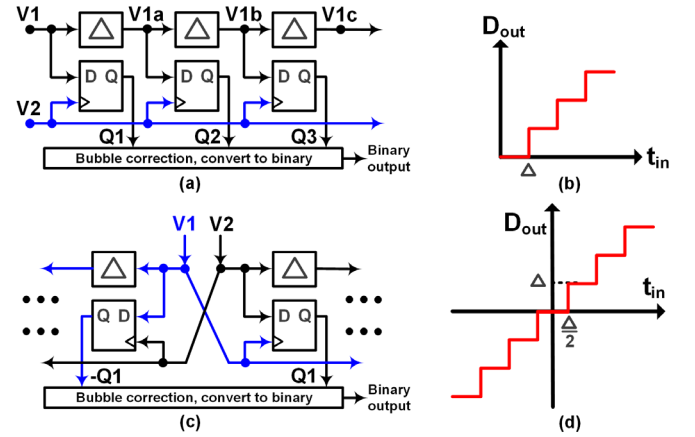


Fig. 6. Delay-line TDC: (a)(b) single delay-line TDC and its input-output characteristic. (c)(d) Use of two TDCs to avoid zero-gain issue.

D. Digital-Controlled Oscillator (DCO)

The DCO topology shown in Fig. 7 is similar to [18]. The DCO is designed to cover 57.51 GHz to 63.57 GHz with fine frequency granularity. The inductor is built by top thick metal layer to achieve high Q.

The top capacitor array C_0 , which is implemented by metal finger capacitors with wide trace to improve the Q. The capacitor bank is controlled by a scan chain to achieve very coarse tuning. Capacitor array C_1 is controlled by 5-bit binary signals from TDC-loop which are converted to thermometer code to select capacitor unit, this guarantees the monotonicity of the switching.

To achieve fine tuning step, reducing the value of capacitor usually is not enough since there is a minimal capacitance we can achieve based on the given DRC rules, and this value is not too much less than 1 fF. However, to achieve 100 kHz level granularity with 60 GHz center frequency, capacitor around 10 aF is needed. Capacitive degeneration technique [19] is proposed to easy this problem. The key idea of this technique is that by putting a capacitor C_2 to the source node of the cross

coupled pair, we can attenuate the effect of the capacitor by a factor of $(g_m/(2\omega C_2))^2$, where g_m is the transconductance of the cross coupled pair, and ω is the operating radian frequency. The attenuation factor is set to around 100 in this design. The two varactors are controlled by 4-bit DACs. The finest tuning frequency we achieved in this design is around 150 kHz by using minimum size of NMOS as C_4 .

To avoiding locking to the harmonics during the loop switching, the tuning range of the Bang-Bang loop is designed to be much smaller than the TDC-loop's. Once the TDC-loop is locked, the TDC outputs a constant code such that the loop is operating at around 60 GHz, while the Bang-Bang loop does not have enough tuning range to lock to harmonics.

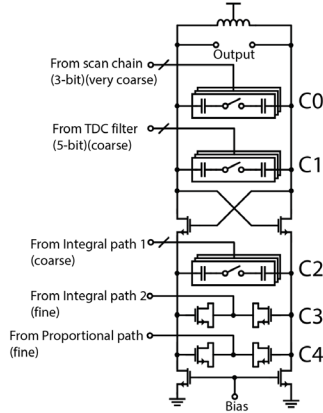


Fig. 7. DCO: (a) Filter to DCO paths. (b) Schematic of DCO.

IV. SIMULATION RESULTS

Fig. 8 shows the frequency tuning characteristic of DCO versus C_0 and C_1 . It shows that we are able to cover 57.51 GHz to 63.57 GHz frequency bands with about 200 MHz overlap between two consecutive control words.

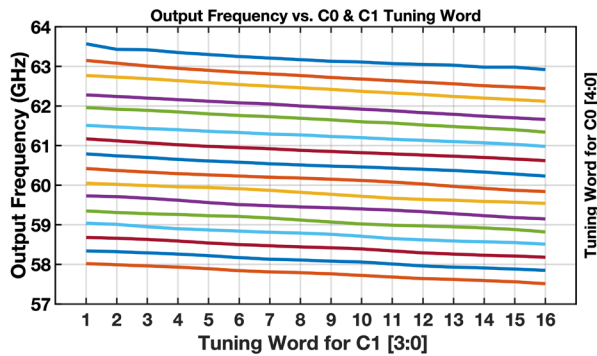


Fig. 8. DCO Frequency tuning versus tuning word of C_0 and C_1 .

The switches of capacitor array are sized to provide enough quality factor. Fig. 9 shows that the Q drops significantly when all switches of C_0 are switched on, this suggests that at the Q at this frequency range is really limited by the switch instead of inductor or capacitor. Looking for better switch topology might be able to improve the performance of the DCO in the next step. For example, [20] provides a good alternative switch.

Fig. 9 shows the phase noise performance of the free running DCO. We are able to achieve -89.08 dBc/Hz and -115.29 dBc/Hz at 1 MHz and 10 MHz offset frequency respectively. The DCO consumes 8.76 mA from a 1V supply. The breakdown of power consumption of each block is listed in table I.

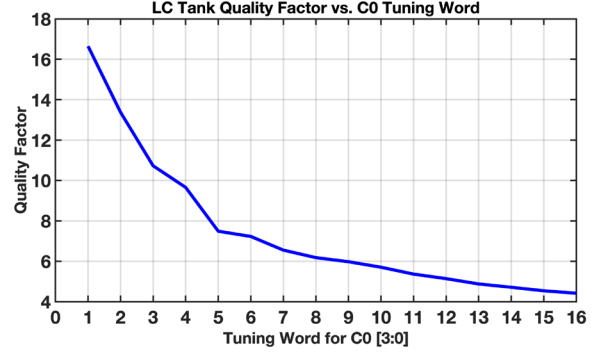


Fig. 9. Q of tank vs. tuning word of C_0 . The Q drops significantly as we switch ON more capacitor units.

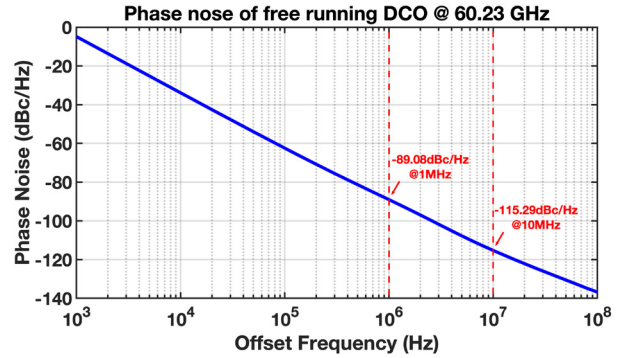


Fig. 10. Phase noise of free-running DCO at 60.23 GHz. The phase noise at 1 MHz and 10 MHz offset are -89.08 dBc/Hz and -115.29 dBc/Hz respectively.

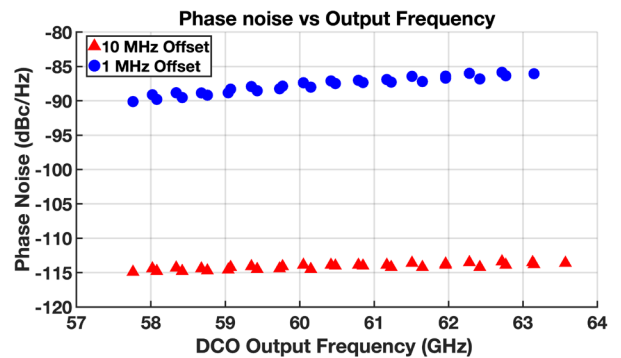


Fig. 11. DCO Phase noise vs output frequency

V. CONCLUSION

In this paper, we show the design of a 60 GHz frequency synthesizer based on the combination of TDC and bang-bang phase detection. The simulation results indicate that we are able to achieve a power consumption lower than 30 mW at this

frequency range due to the simplicity of the TDC and the low power frequency divider.

TABLE I. POWER CONSUMPTION

Block	Power Consumption (mW)
Total	20.55
DCO	8.76
DCO buffers	2.91
CML divider	5.39
Pulse swallow divider	0.65
TDC	0.13
Digital filters	1.18
DSMs	1.53

TABLE II. PERFORMANCE SUMMARY AND COMPARISON

	[1]	[21]	[22]	This work
Technology (nm)	65	65	40	28
Supply voltage (V)	1	1	0.9	1
Ref frequency (MHz)	100	40	40	100
Fout (GHz)	50.2-66.5	55.6-65.2	53.8-63.3	57.5-63.6
Tuning range	28%	16%	16%	10%
PN @ 1MHz (dBc/Hz)	-94.5~-88	-92	-88.3	-90.1~-84.5*
Power (mW)	46	32	42	20.18
FOM @ 1MHz (dBc/Hz)	-172.3	-172.2	-168.1	-171.5
FOM _T @ 1MHz (dBc/Hz)	-181.3	-173.2	-172.3	-171.6
$FOM = PN(\Delta f) - 20 \log \left(\frac{F_{out}}{\Delta f} \right) + 10 \log \left(\frac{Power(mW)}{1mW} \right)$				
$FOM_T = PN(\Delta f) - 20 \log \left(\frac{F_{out} \times TR}{\Delta f \times 10\%} \right) + 10 \log \left(\frac{Power(mW)}{1mW} \right)$				

* Phase noise of DCO is used here to estimate PLL's performance

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