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LETTER

High-current recessed gate enhancement-mode ultrawide bandgap $Al_xGa_{1-x}N$ channel MOSHFET with drain current 0.48 A mm^{-1} and threshold voltage +3.6 V

Shahab Mollah*, Kamal Hussain, Abdullah Mamun, Mikhail Gaevski, Grigory Simin, MVS Chandrashekhar, and Asif Khan

[1]Department of Electrical Engineering, University of South Carolina, Columbia, SC-29208, United States of America

*E-mail: mmollah@email.sc.edu

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We report a recessed-gate enhancement-mode Al_2O_3-ZrO_2/$Al_{0.6}Ga_{0.4}N$/$Al_{0.4}Ga_{0.6}N$ metal-oxide-semiconductor heterostructure field-effect transistor (MOSHFET) with drain current as high as 0.48 A mm^{-1} at a gate-source voltage of +12 V. This was enabled by a pseudomorphic HFET structure with graded back barrier for strain management and to screen the growth interface from the channel. The device exhibited a threshold-voltage (V_{TH}) of 2.75 ± 0.57 V with absolute maximum V_{TH} = 3.6 V, a +12.2 V shift from that for a depletion-mode MOSHFET fabricated on the same wafer. A 3-terminal breakdown voltage of 700 V was measured in the off-state, showing the viability of E-mode UWBG AlGaN for power electronics.

Supplementary material for this article is available online

Since the first demonstration of depletion and enhancement-mode AlGaN/GaN high electron mobility transistors (HEMTs), significant progress has been made in increasing their performance.[1–3] These advances have resulted from improving the material quality in the lattice mismatched growth of $Al_xGa_{1-x}N$ over sapphire/SiC/Si, the adoption of new device designs and the ability to form insulating gates on the $Al_xGa_{1-x}N$ barrier layers.[4–6] The depletion-mode (D-mode) HEMTs a.k.a heterostructure field-effect transistors (HFETs) and metal-oxide semiconductor HEMTs (MOS-HEMTs), a.k.a. MOSHFETs are now established commercial products with applications in RF/microwave power amplifiers. In a number of applications, enhancement-mode (E-mode) HFETs are preferable as they provide short-circuit protection power switches,[7] eliminate the need of negative bias,[8] and are useful in direct-coupled field-effect-transistor logic[9] etc.

Achieving E-mode operation in AlGaN-GaN HFETs has been accomplished by: (i) decreasing the barrier thickness,[2,10,11] (ii) adding cap layers,[12,13] and (iii) using fluoride-based treatment.[14,15] Kanamura et al. reported GaN MOSHFET with the highest peak drain current of 0.8 A mm^{-1} (at V_G = +10 V) and OFF-state breakdown voltage of 320 V at V_G = 0 V.[10] Using linear extrapolation for threshold-voltage (V_{THLE}) they obtained V_{THLE} = +3 V. Asubar et al. demonstrated GaN MOSHFETs with V_{THLE} ~ +5 V and a peak current of 425 mA mm^{-1}.[16]

Several research groups are developing ultrawide bandgap (UWBG) $Al_xGa_{1-x}N$ channel HFETs for high-temperature, high-voltage, and high-power applications. UWBG $Al_xGa_{1-x}N$ layers have higher breakdown field[17–19] which leads to a higher Baliga figure of merit.[20,21] Devices with channel alloy compositions of 40% or higher have been reported,[22–26] with currents as high as 1.3 A mm^{-1}.[27] Recently using fluorine treatment, Klein et al. reported E-mode UWBG $Al_{0.7}Ga_{0.3}N$ channel HFET with V_{TH} = +0.5 V (at I_{DS} = 0.1 mA mm^{-1}) with a peak current of only 35 mA mm^{-1} (at V_G = +6.6V).[28]

Here, we report a novel pseudomorphic $Al_{0.6}Ga_{0.4}N$/$Al_{0.4}Ga_{0.6}N$ HEMT structure with graded back barrier to manage strain arising from lattice mismatch between AlN and $Al_{0.4}Ga_{0.6}N$ without releasing strain through dislocations and cracks. This is in contrast with traditional AlGaN/GaN HEMTs which are metamorphic in nature, with the GaN channel ideally being fully relaxed.

This structure was grown over a 3 μm thick, high-quality AlN/sapphire template [Fig. 1(a)]. To achieve pseudomorphic registry, the total thickness beginning from the AlN template to the top surface was reduced to approximately half of our past design to reduce the total built-in strain.[24] The back interface is now closer to the channel, potentially causing more traps. To solve this problem, the graded back barrier $Al_xGa_{1-x}N$ (x from 1 to 0.4) layer was introduced to screen the growth interface from the channel while serving as a strain management layer by gradually varying the alloy composition as opposed to an abrupt junction. It was followed by an 1850 Å thick undoped $Al_{0.4}Ga_{0.6}N$ channel and a silicon doped n-$Al_{0.6}Ga_{0.4}N$ barrier layer. A 20 nm thick reverse composition graded Si-doped $Al_xGa_{1-x}N$ (x from 0.6 to 0.3) layer was also deposited on top of the barrier to assist with ohmic contact formation, by presenting an effective Schottky barrier of 0.62 eV for $Al_{0.3}Ga_{0.7}N$ compared to 2.7 eV[29] for $Al_{0.6}Ga_{0.4}N$. The epilayer growth was carried out using low pressure metalorganic chemical vapor deposition (LP-MOCVD) as described elsewhere.[30] The back-barrier design enables a reduction in leakage currents by screening the substrate-epilayer growth interface, which improves the ON–OFF ratios, drain-currents, and the sub-threshold swing (SS).[31,32] Figure 1(b) shows the simulated energy band diagram of structure epilayer structure of Fig. 1(a) in the cases of barrier recess (bottom) and without barrier recess (top). For recessed barrier structure, the bottom of the conduction band is above E_f, indicating absence of 2DEG at V_G = 0 V which means normally-off operation, while for structure without barrier recessing there is clear dip of E_c below E_f.

The processing consisted of inductively coupled plasma reactive ion etching (ICP-RIE) for mesa-isolation followed by the formation of source drain ohmic-contacts. Zr/Al/Mo/Au (150/1000/400/300 Å) was deposited with E-beam evaporation and annealed for 30 s at 950 °C under N_2 ambient using rapid thermal annealing.[33]

For this study, perforated channel (PC) layout,[34,35] was used to reduce access resistances. In the PC design, the gate area consists of the alternating regions of conducting straits separated by non-conducting islands where the channel material is completely removed (only under the gate but

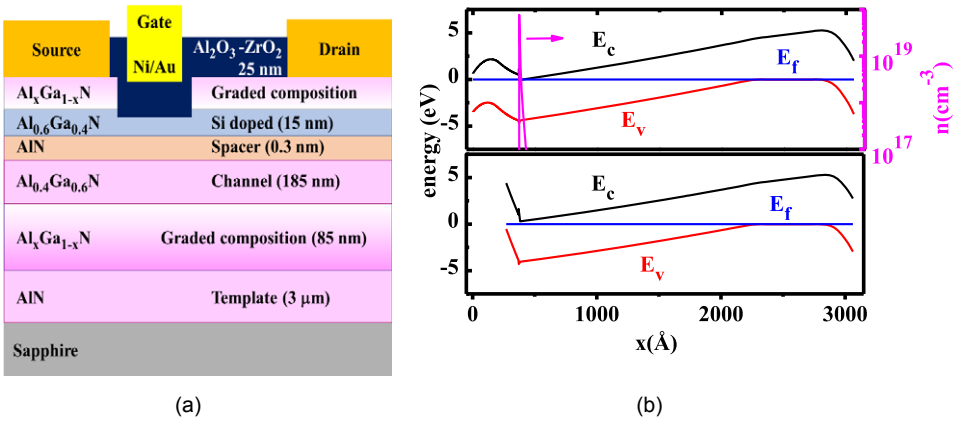

Fig. 1. (Color online) (a) Schematic layout of recessed gate MOSHFET and (b) band diagram for epilayer structure of Fig. 1(a): without recessed barrier (top) and recessed barrier (bottom).

not in the G–S and G–D regions). The current flowing out of the gate straits therefore spreads out into larger area G–S and G–D regions which leads to smaller gap and contact access resistances (see supplementary information for more details available online at stacks.iop.org/APEX/14/014003/mmedia). The maximum reduction of the access resistances, by a factor of 2–3, occurs when the gap between the straits is around twice the width of the straits and the gate-drain distance is larger or comparable to the strait width.[34] Accordingly, for the PC design we selected the width of the straits $W_S \approx 3.75\ \mu$m, with blocking gaps between them $W_B \approx 8.25\ \mu$m (see supplementary information). These dimensions were confirmed using scanning electron micrographs. This geometry corresponds to an optimal island/gap ratio of 2–2.5 as was determined following the procedure outlined in Refs. 27, 34, 35. In addition, in the PC layout, the reduction in average power density reduces the device temperature and also enables higher channel currents. The 250 nm deep current blocking islands were formed using a Cl_2 based RIE process with an etch rate of $\sim 10\ \text{nm s}^{-1}$ after the formation of the source-drain ohmic contacts. Measurement on test structure shows that islands are completely insulating. The threshold voltage of PC device was found to be same as that of non-perforated control device.

Next the barrier was recessed to ~10 nm thickness using a slow ICP-RIE etching process with BCl_3/Cl_2 gas mixture followed by chemical treatment of etched surface with tetramethylammonium hydroxide (TMAH) solution to smooth out the surface as has been done with III-nitrides previously[27] The etch rate of $1\ \text{nm s}^{-1}$ was calibrated using atomic force microscopy. Then a 25 nm thick ZrO_2–Al_2O_3 insulator (ZrO_2 followed by Al_2O_3) stack was deposited in the recess region using atomic layer deposition technique before the formation of the Ni/Au gates. The gate-length, gate-source and gate-drain spacings were respectively $L_G \approx 2.0\ \mu$m, $L_{SG} \approx 1.5\ \mu$m and $L_{GD} \approx 2.5\ \mu$m. The transistor surface was protected with PECVD deposited 400 nm thick SiO_2 film for high-voltage breakdown measurements.

TLM was used to estimate the sheet-resistance (R_S) and the contact resistance to be ~1700 Ω/□ and ~1.7 Ω-mm respectively. The R_S value was within 10% of that measured using rf-eddy current approach. Then PC devices were measured and the drain currents were normalized to the conducting portion of the channel width which is 15.6 μm (W_S) for a 50 μm ($W_S + W_B$) width unperforated device.[27,34,35] Figure 2(a) inset shows the source-drain characteristic curves for the recessed-gate Al_2O_3–ZrO_2/PC-MOSHFET with $L_G \approx 2.0\ \mu$m, $L_{SG} \approx 1.5\ \mu$m and $L_{GD} \approx 2.5\ \mu$m. A peak current of $0.48\ \text{A mm}^{-1}$ was measured at a gate bias of +12 V while it is $0.15\ \text{A mm}^{-1}$ when normalized to the full channel width ($W_S + W_B$). Even

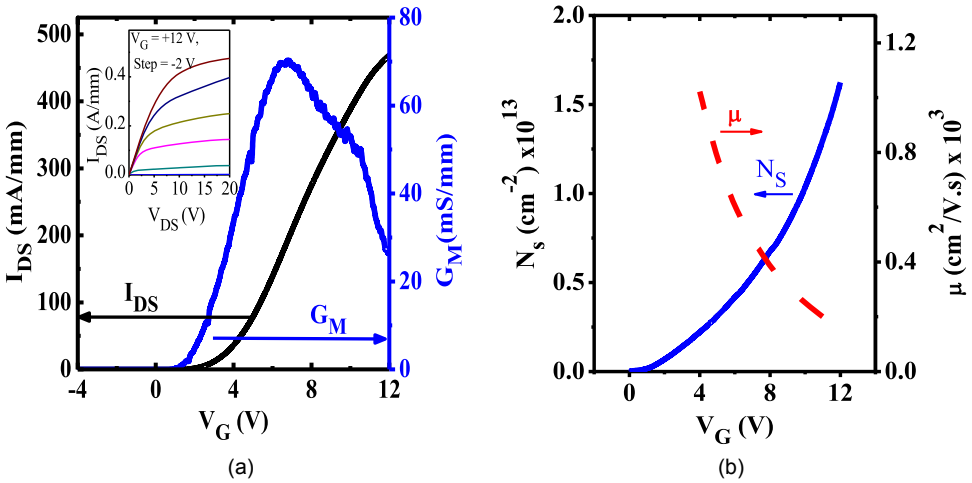

Fig. 2. (Color online) (a) Transfer characteristics of a recessed-gate E-mode Al_2O_3–ZrO_2/PC-MOSHFET with $L_G = 2\ \mu$m, $L_{SD} = 6\ \mu$m and gate-width $W_G = 50\ \mu$m. Inset shows the source-drain *I–V* characteristics and (b) Ns and μ-V_G dependencies for the device of Fig. 2(a).

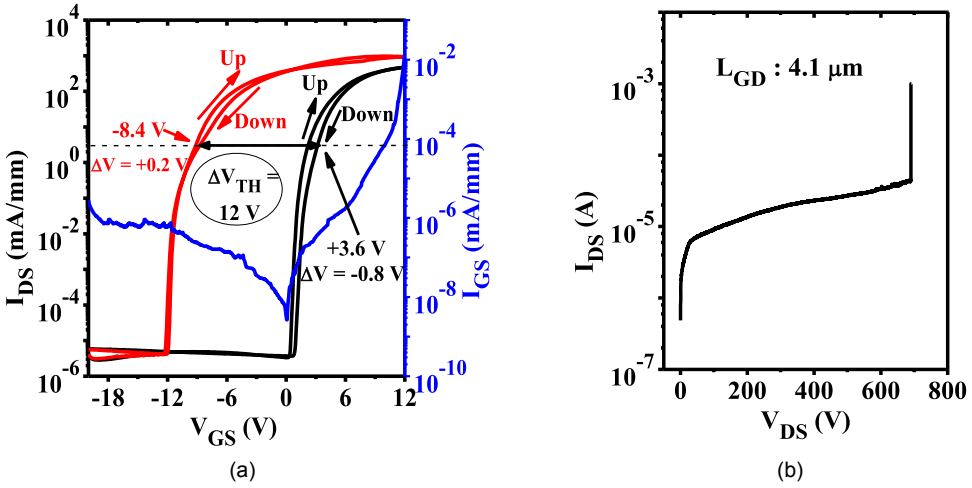

Fig. 3. (Color online) (a) Semi-log double-sweep transfer characteristics measured at $V_{DS} = +20$ V for the E-mode device of Fig. 3. The transfer curve for a D-mode device at $V_{DS} = +20$ V is shown for comparison. Also plotted is the gate leakage current of the E-mode device. (b) Breakdown voltage data for the E-mode device of this study.

with normalized to full channel width, the current density is the highest reported value till date for UWBG AlGaN channel E-mode devices. Pulsed *I–V* measurement was done using DIVA D-265 dynamic IV analyzer with a pulse duration of 500 ns and low duty cycle of 0.1% to avoid self-heating. At $V_G = +10$ V, the pulsed current was found to be 0.38 A mm^{-1} (see supplementary information), a slight increase from 0.36 A mm^{-1} DC current. We estimated an ON-resistance (R_{ON}) of 18 Ω mm. In Fig. 2(a) we find $V_{TH} = +3.6$ V, from linear extrapolation, with a transconductance of 70 mS mm^{-1} ($L_G \approx 2.0$ μm). To estimate the V_{TH} variation, ten random devices were measured, spread over 1.5 cm to be representative of the whole quarter of a 2″ wafer. The mean $V_{TH} = 2.75$ V with a standard deviation of 0.57 V (Fig. 4). The V_{TH} variation across the wafer could be due to following two reasons: (i) recess depth variation (ii) variation of sheet resistance across the wafer. The most likely cause is recess depth variation ~2 nm, which would cause ~0.6 V V_{TH} shift,[36] potentially accounting for the observed variation. The sheet resistance variation is most likely caused by variations in carrier mobility across the wafer, as *C–V* measurements on the as-grown wafers showed similar N_s across the sample.

To determine the factors leading to the high drain current we extracted the gate voltage dependencies of N_S and μ as described in.[33,37] Figure 2(b) shows N_S reaching 1.6×10^{13} cm^{-2} at $V_G = +12$ V. μ is as high as 1050 cm^2 V^{-1}. s^{-1} near threshold $V_G = 4$ V and decreases to 200 cm^2 V^{-1}. s^{-1} at V_G +12 V, consistent with past reports.[38] Figure 3(a) compares the semi-log transfer characteristics for the device of Fig. 2(a) measured at $V_{DS} = +20$ V with that for an identical geometry D-mode device (no gate-recess) fabricated on the same wafer, showing a V_{TH} shift of +12.2 V due to the gate recess. The E-mode device shows a hysteresis of 0.8 V between forward and reverse sweep of gate voltage, higher than that of D-mode (0.2 V) indicating higher trap charges at semiconductor/oxide interface or bulk.[39] We speculate this higher trap density might be from barrier recessing. This is supported by the slight increase in SS) increase after barrier recess from 105 ± 8 mV/decade for the non-recessed control devices to 138 ± 19 mV mV/decade. The best E-mode device showed SS = 128 mV/decade and an ON/OFF ratio > 1.5×10^8, while $I_{GS} < 10$ μA mm^{-1} over the entire V_G range [Fig. 3(a)]. Three terminal

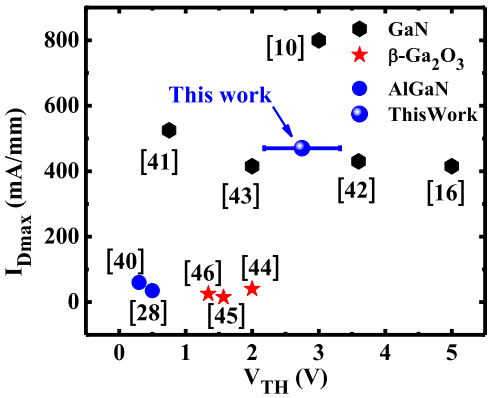

Fig. 4. (Color online) Comparison of our reported results with I_{DMAX} and V_{TH} of some normally-off wide bandgap GaN as well as UWBG AlGaN and Ga_2O_3 channel HEMTs reported in literature.

breakdown voltage at $V_G = 0$ V for a device with $L_{GD} = 4.1$ μm, was found to be +700 V [Fig. 3(b)] which is above +600 V, required for power devices in automotive applications, and has not been reported for UWBG AlGaN E-mode devices.[28,40]

We benchmark the Al_2O_3–ZrO_2/$Al_{0.4}Ga_{0.6}N$ channel E-mode devices against other wide (GaN) and UWBG (β-Ga_2O_3 and AlGaN) channel E-mode devices in Fig. 4, where for GaN channel we only included devices with $I_{DS} > 400$ mA mm^{-1}.[41–46] Our results show highest current density among UWBG materials while compare favorably to some of the best values for GaN despite the greater maturity of GaN-channel HFET technology.

In summary, using recessed gate technology in combination with a new pseudomorphic back barrier structure with reverse graded top contacts and PC design, we have reported an Al_2O_3–ZrO_2/$Al_{0.6}Ga_{0.4}N$/$Al_{0.4}Ga_{0.6}N$ E-mode MOSHFET with drain currents as high as 0.48 A mm^{-1}. This demonstrates that UWBG AlGaN channel E-mode devices are promising for power electronics.

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ORCID iDs Shahab Mollah https://orcid.org/0000-0002-2848-2959 Kamal Hussain https://orcid.org/0000-0001-7344-345X Abdullah Mamun https://orcid.org/0000-0002-6210-7829 Mikhail Gaevski https://orcid.org/0000-0003-1172-0516 Asif Khan https://orcid.org/0000-0002-4542-6553

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