A Real-Time Adaptive IGBT Thermal Model Based on an Effective Heat Propagation Path Concept

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***Abstract*—The information of junction temperature is crucial for operation management of insulated-gate bipolar transistor (IGBT) modules. In practice, junction temperature is typically estimated by using an electrothermal model. IGBT modules are subject to various aging processes during operation, some of which, e.g., substrate solder crack, changes the thermal impedance of the IGBT module. However, in the literature little work has included the aging effect into online thermal behavior modeling of IGBT modules. This paper proposes an Effective Heat Propagation Path (EHPP)-based real-time adaptive thermal model for IGBT modules, where the EHPP is proposed to quantify the impact of substrate solder cracks on the heat propagation inside the IGBT modules. A straightforward relationship between substrate solder crack and the degree of nonuniformity of case temperature distribution is established. This relationship is then used to approximate the EHPP of the IGBT module in different substrate solder health conditions in real time using the measured nonuniformity of case temperature distribution. Based on the change of the EHPP, the parameters of a thermal equivalent circuit (TEC) model, e.g., an improved Cauer-type TEC, are adjusted online and in real time to track the thermal behavior changes of the IGBT modules caused by substrate solder cracks, leading to a real-time substrate-solder-aging-adaptive thermal model. The proposed real-time adaptive thermal model is validated by simulation studies and experimental tests for a commercial IGBT module.**

***Index Terms*—Adaptive thermal model, effective heat propagation path (EHPP), insulated-gate bipolar transistor (IGBT), real time, solder aging**

I. Introduction

THE information of junction temperature T_j is crucial for operation management [1] and condition monitoring [2] of IGBT modules in real-world applications. Accurate junction temperature information can be used to prevent over-temperature, reduce thermal stress [3], and estimate the remaining useful life [4], [5] for an IGBT module. IGBT modules have a complex multilayered structure and the junctions of IGBTs are not accessible in practice. In most applications, junction temperature is typically estimated by using an electrothermal model, which consists of power loss estimation and a thermal behavior model. Recently, much work [6]-[15] has been carried out on computationally efficient thermal behavior modeling for power semiconductor devices when the devices are healthy.

However, IGBT modules are subject to various aging processes during operation, which can alter the thermal behaviors of the modules and degrade the accuracy of T_j estimation. For example, the process-induced solder void and fatigue-introduced solder crack are two major failure mechanisms affecting heat propagation inside IGBT modules [17]. The IGBT modules with significant process-induced solder voids may be screened out at the production line. However, the substrate solder is more critically subject to fatigue, commonly leading to solder cracks [18] and degradation of heat propagation inside an IGBT module. In consequence, the thermal resistance of the IGBT module will increase, leading to a higher T_j when the operating point and cooling condition remain the same. In this case, using a thermal model developed for a healthy IGBT will result in an underestimation of T_j. Thus, a thermal model that is adaptive to aging of IGBT modules is desired for effective operation management of IGBT modules in real-world applications.

However, in the literature little work has included the aging effect into the thermal behavior modeling of power semiconductors, such as power MOSFETs and IGBT modules. An attempt to update a Foster-type thermal equivalent circuit (TEC) model for a power MOSFET during solder aging process with the aid of using temperature sensitive electrical parameters (TSEPs) was presented in [19]. The threshold voltage of the power MOSFET was selected as the TSEP for online junction temperature measurement. By comparing the measured and estimated junction temperatures, the percentage increase in the total thermal resistance from junction to case can be calculated. Each resistance of the Foster-type TEC was then simply multiplied by the same percentage increase based on the assumption of a linear degradation in each layer in the multilayered package. However, using TSEPs can be impractical in many applications, as a complex and costly circuitry is typically required to monitor the very small drift in TSEPs against a noise background. Moreover, since it is difficult to characterize the change of the heat propagation inside the multilayered package caused by solder aging, the parameters of the thermal model cannot be effectively updated online to track the dynamic thermal behavior of the device during solder aging. Thus, it is still an open question to

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develop thermal models for power semiconductors including IGBT modules that are adaptive to aging of the devices online.

The authors' previous work [20] focused on fatigue-introduced substrate solder crack and introduced a new concept called Effective Heat Propagation Path (EHPP) to interpret the effect of substrate solder crack on the heat propagation inside an IGBT module. First, the non-cracked area in the substrate solder layer of an IGBT module for heat flow propagation was estimated through an Inverse Heat Conduction Problem (IHCP) of the baseplate layer using the measurable nonuniformity of case temperature distribution. A simple implementation to obtain the information of the nonuniformity was to place two thermocouples on the bottom surface of the baseplate of an IGBT module and measure the differences of the two measured case temperatures at a certain operating condition. Then, the EHPP was approximated using a thermal spread angle method and the estimated non-cracked area in the substrate solder layer. Finally, based on the approximated EHPP, the resistances and capacitances of a Cauer-type TEC model can be adjusted online during the substrate solder aging process, leading to an adaptive thermal model. However, the measured nonuniformity of case temperature distribution in [20] depends on the operating condition of the IGBT module. Therefore, the method in [20] requires case temperature measurements at various operating conditions for practical applications. In addition, no details on how to approximate the EHPP and update the parameters of the TEC model using the approximated EHPP were provided in [20]. Furthermore, only simulation results were reported in [20] to validate the adaptive thermal model; no experimental result was provided.

The method of using case temperatures measured at two different locations for solder aging monitoring in the authors' previous paper [20] has been followed by other researchers [21], [22]. In [21], once a change in solder health status was indicated by case temperatures, the measurement of junction temperature using a TSEP was performed, and then the thermal resistance from junction to case was recalculated. The goal of that approach was to perform a TSEP acquisition when necessary to reduce the interruptions to power converter operations. In [22], the health status of the solder layer in an IGBT module was monitored by using the temperature gradient of the baseplate, which was obtained by dividing the case temperature difference between two points on the baseplate by their distance and power loss. Though the temperature gradient of the baseplate was claimed to be independent of the operating conditions of power converters, the calculation of power loss still requires operating conditions and junction temperature information. Moreover, for the adaptive TEC model presented in [22], only the thermal resistances were updated by using the same method in [19], which requires junction temperature measurement and cannot capture the changes in the dynamic thermal behavior of the IGBT module caused by solder cracks.

This paper significantly extends the authors' previous work in [20] by using an improved solder aging indicator to estimate the remaining non-cracked area in the substrate solder layer for the EHPP approximation, providing details on how to approximate the EHPP and how to update the parameters of a TEC model using the approximated EHPP, adding new simulation results obtained from the improved solder aging indicator, and adding experimental test results. The improved solder aging indicator is directly calculated from the case temperatures measured at two different locations on the bottom surface of baseplate without the need for the information of power loss and junction temperature of the IGBT module (both are required in [22]) and, thus, is independent of operating conditions of the power converters. Therefore, the relationship between the improved solder aging indicator and different solder health statuses established at a certain operating condition can be used to update the parameters of the TEC at any operation conditions in real time. This eliminates the need in [20] for establishing the relationships between case temperature differences and different solder health statuses at various operating conditions. The proposed solder-aging-adaptive thermal model is validated by both simulation and experimental results for a commercial IGBT module.

II. EHPP-Based Thermal Behavior Characterization for IGBT Modules

Due to the geometry complexity and differences in the materials' properties, the heat propagation inside an IGBT module is a complex, dynamical process. This section presents the concept of the EHPP to simplify the analysis of this process. Then, the change of the thermal resistance from junction to case caused by substrate solder cracks can be interpreted by the change of the EHPP, which can be monitored by the degree of the nonuniformity of the case temperature distribution. In this way, the impact of substrate solder cracks on the thermal behavior of IGBT modules can be effectively quantified by using the EHPP in real time with case temperature measurements.

The EHPP is defined to be the thermal path in an IGBT module through which most heat flows, as illustrated in Fig. 1. During the operation of the IGBT module, the heat can be assumed to be generated at the top surface of a die and spreads down through different layers to the bottom of the baseplate, which is cooled by a heat sink or a cold plate. Compared to the top surface of the die, the EHPP covers a larger area at the bottom surface of the baseplate, which is called baseplate hot area A_{hot}. The temperature inside A_{hot} is much higher than that in the remaining area of the bottom surface of the baseplate. A_{hot} can be viewed as the thermally effective contact to the

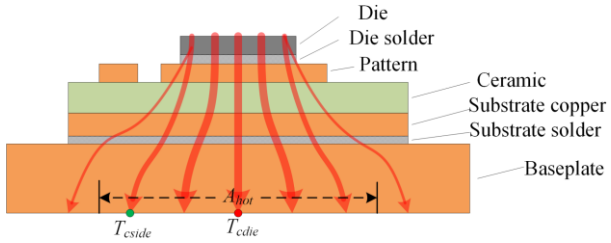

Fig. 1. The EHPP in a healthy IGBT module (wires and terminals are not shown).

heat sink or the effective heat removal area. The following paragraphs describe how the EHPP and A_{hot} change with substrate solder aging and derive the relationship between the change of the case temperature distribution and the remaining non-cracked solder area in the substrate solder layer.

A crack usually initializes from the edge of the substrate solder layer and then propagates to the center [24]-[26]. The crack will not significantly affect the heat propagation inside the IGBT module or the thermal resistance from junction to case R_{thjc} of the IGBT module until it encroaches the EHPP. In this case, the IGBT module is in a dangerous status in which the heat flows are forced to concentrate to the remaining non-cracked portion of the substrate solder layer, as illustrated in Fig. 2. Both the EHPP and A_{hot} shrink, resulting in the increase of the IGBT module's R_{thjc} and the degradation of heat removal at the bottom surface of the baseplate.

Assuming that the same amount of heat is generated at the top surface of the die, the shrink of the A_{hot} can be indicated by an increase in the nonuniformity of the case temperature distribution at the bottom surface of the baseplate. The degree of the nonuniformity can be reflected by the changes in the case temperature T_{cdie} at the location right beneath the die (i.e., in the middle of the A_{hot}) and the case temperature T_{cside} at the location inside the A_{hot} but near the edge of the A_{hot}. If the A_{hot} shrinks, T_{cdie} will increase due to more concentration of the heat flows; while T_{cside} may increase but with an increment much less than that of T_{cdie} or even drop as its location tends to move out of the A_{hot} or away from the main EHPP.

However, it is still not straightforward to establish the relationship between T_{cdie}, T_{cside}, the remained non-cracked area A_r in the substrate solder layer, and the change of the EHPP caused by substrate solder cracks, because an IGBT module involves multilayer thermal conduction and heat storage and spreading. To establish an effective relationship, this paper simplifies the problem to a baseplate layer IHCP, which utilizes the measurable case temperatures to inversely estimate the remaining non-cracked solder area. By neglecting the heat spreading in the thin substrate solder layer, the heat flux flowing through the substrate solder layer to the baseplate is perpendicular to the baseplate top surface. Then, the A_r in the substrate solder layer is equivalent to the heat flux area on the top surface of the baseplate. Fig. 3 shows the change in the heat flux on the baseplate top surface due to the aging of the substrate solder. Assume that the cooling condition is stable such that the boundary condition on the bottom surface of the baseplate is stationary. Then, since the heat flux is concentrated at center, the total heat propagating through the EHPP at a specific heat generation rate of the IGBT module is specific and the IHCP solution, A_r, is unique. Thus, at a specific heat generation rate, A_r can be monitored by tracking the changes in T_{cdie} and T_{cside}, which, however, usually change with the heat generation rate of the IGBT module.

In practice, the heat generation rate or power loss, P_{loss}, of an IGBT module may change from time to time due to the change of the operating condition. Therefore, it is not convenient to estimate A_r over time directly using T_{cdie} and T_{cside} due to the varying operating condition, especially during the aging process of the IGBT module. This issue is resolved by relating A_r to an operating-condition independent parameter k_{cs}, which is defined as follows.

$$k_{cs} = \frac{R_{eqth,cdie}}{R_{eqth,cside}} = \frac{(T_{cdie} - T_a)/P_{loss}}{(T_{cside} - T_a)/P_{loss}} = \frac{T_{cdie} - T_a}{T_{cside} - T_a} \quad (1)$$

where $R_{eqth,cdie}$ and $R_{eqth,cside}$ are the equivalent thermal resistances from the two locations on the baseplate to the ambience, respectively; and T_a is the ambient temperature. Although the equivalent thermal resistance is defined to be similar to a thermal resistance such as R_{thjc}, it characterizes the relationship between the temperature rise from ambient to a point in the IGBT module and the power loss based on the linear thermal behavior of the IGBT module. The detailed definition and explanation of the equivalent thermal resistance can be found in the authors' previous work [23]. The parameter k_{cs} in (1) describes the degree of the nonuniformity of the case temperature distribution at the bottom surface of the baseplate. The power loss needed for monitoring the changes in $R_{eqth,cdie}$ and $R_{eqth,cside}$ is cancelled when calculating k_{cs}, as shown in (1). Therefore, the value of k_{cs} is independent of the heat generation rate of the IGBT and can be easily calculated just using T_{cdie}, T_{cside}, and T_a, and the calculation does not need of the information of junction temperature. This means that if the relationship between k_{cs} and A_r at a certain operating condition through the aging process is obtained, the relationship can be applied to various operating conditions at any junction temperature during the aging process. In practice,

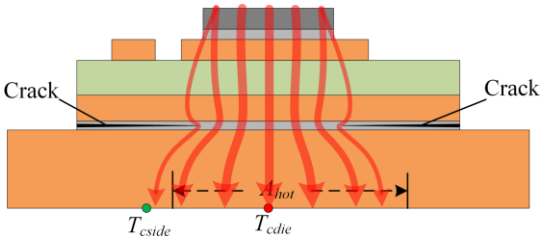

Fig. 2. The EHPP in an IGBT module when cracks developed from the edge to the center in the substrate solder layer.

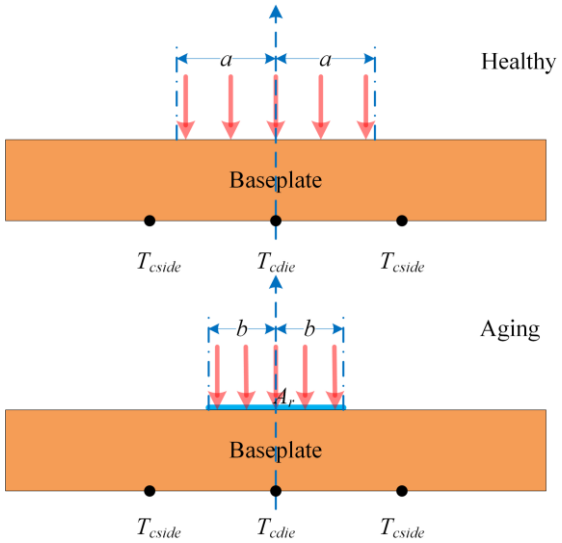

Fig. 3. Estimation of the effective heat flux area on the top surface of the baseplate using case temperatures by the IHCP.

a look-up table can be conveniently built via a numerical method, such as finite element analysis (FEA), or an accelerated aging test at a certain operating condition to relate k_{cs} to A_r. Then, according to k_{cs} calculated by (1), A_r can be determined in real time according to the look-up table for various operating conditions without the need for the junction temperature information. The changes of k_{cs} and/or A_r can be used for online solder aging monitoring under various operating conditions.

III. Proposed EHPP-Based Real-Time Adaptive Thermal Model for IGBT Modules

Once the health condition of the substrate solder of an IGBT module is quantified online using A_r via the information of k_{cs}, the next question is how to model the thermal behavior of the IGBT module adaptively by incorporating the substrate solder aging effect. The FEA method can provide a high-fidelity thermal model, which, however, requires extensive time and memory to implement. This paper proposes an EHPP-based real-time substrate-solder-aging-adaptive TEC model for IGBT modules. In the proposed model, a physics-based improved Cauer-type TEC [8] is used to represent each layer of the EHPP inside an IGBT module. Thick layers, such as the ceramic layer, may be subdivided into 3-4 sublayers and each sublayer is modeled by using a resistor-capacitor (RC) pair. This improved Cauer-type TEC has a slightly higher order than the traditional TECs but is more accurate to characterize the thermal behavior of IGBT modules. Using the improved Cauer-type TEC can significantly reduce the error in junction temperature estimation caused by the lumped thermal capacitance model [8]. Then, the focus can be placed on the impact caused by solder aging and the adaption of the RC parameters based on the EHPP. The EHPP shown as the dashed-line area in Fig. 4 for an IGBT module with multiple dies in parallel is approximated by using the heat spreading angle technique [27]. The impact of substrate solder cracks on the thermal behavior of the IGBT module is interpreted via the change of the EHPP. Assuming that only the EHPP through the substrate solder layer and its two adjacent layers, i.e., the substrate copper layer and baseplate layer, is altered by the substrate solder cracks, then the area A_c of the EHPP through the bottom surface of the ceramic layer is constant.

The values of the RC parameters of the proposed adaptive Cauer-type TEC thermal model shown in Fig. 5 are calculated based on the approximated EHPP illustrated in Fig. 4. Since the thermal cross-coupling between IGBT and free-wheeling diode is very weak, the typical cross-coupling thermal resistance can be less than one tenth of the R_{thjc} of the IGBT. Thus, the impact of solder crack on the thermal cross-coupling between IGBT and free-wheeling diode is not modeled in the proposed adaptive TEC thermal model and can be simply modeled in the heatsink thermal model [28]. The heat spreading angles in the pattern layer and the ceramic layer are the same and denoted as θ_x, which is assumed to be 45°, a typical value used in practice. The heat spreading in the substrate solder layer is neglected owing to the relatively low thermal conductivity of solder and the relatively thin thickness of the substrate solder layer. The heat spreading angle θ_{bp} in the baseplate depends on the cooling condition and is given as a function of the ratio between the total thickness of all the heat-spreading layers beneath the die and the side length of the die [29]. Therefore, only the heat spreading angles, θ_{adj1} and θ_{adj2}, in the substrate copper layer need to be determined according to the status of the substrate solder crack. Once A_r in the substrate solder layer is obtained, θ_{adj1} and θ_{adj2} can be calculated using the side length l_c of A_c and the side lengths l_{r1} and l_{r2} of A_r, respectively, and the thickness $d_{sub,cop}$ of the substrate copper layer. For the typical case shown in Fig. 4, θ_{adj1} and θ_{adj2} can be calculated by:

$$\theta_{adj1} = \tan^{-1}\left(\frac{l_{r1} - l_c}{d_{sub,cop}}\right) \tag{2}$$

$$\theta_{adj2} = \tan^{-1}\left(\frac{l_{r2} - l_c}{2d_{sub,cop}}\right) \tag{3}$$

Note that θ_{adj1} and θ_{adj2} could be negative if l_{r1} and l_{r2} are smaller than l_c when solder crack develops into some severe conditions.

It is suggested to subdivide the silicon and ceramic layers into 3 and 4 sublayers, respectively [8]. The thermal resistance and capacitance of any layer or sublayer denoted by x can be calculated by:

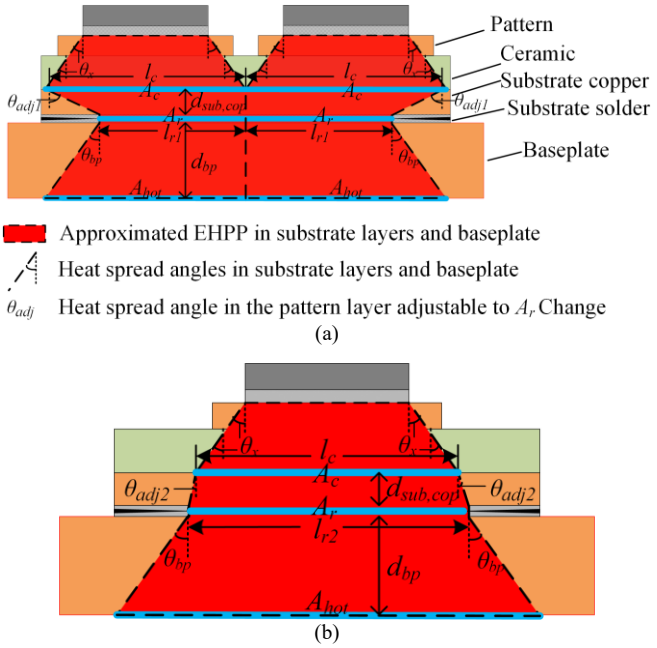

Fig. 4. The approximated EHPP for a multi-die IGBT module with substrate solder cracks: (a) front view; and (b) side view.

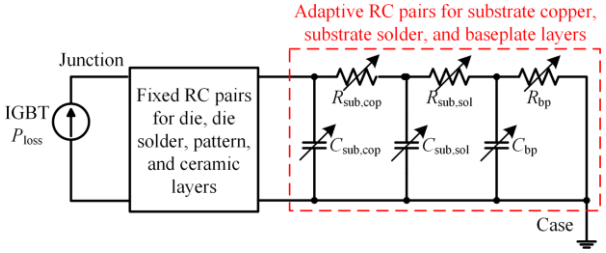

Fig. 5. The proposed adaptive Cauer-type TEC thermal model.

$$R_{th,x} = \int_0^{d_x} \frac{1}{k_x A_x(z)} dz \tag{4}$$

$$C_{th,x} = \int_0^{d_x} c_{v,x} A_x(z) dz \tag{5}$$

where $R_{th,x}$, $C_{th,x}$, d_x, k_x, $c_{v,x}$, and z are the thermal resistance, thermal capacitance, thickness, thermal conductivity, and volumetric specific heat of the material and the vertical distance from the top surface to the bottom surface of the layer or sublayer x, respectively; and $A_x(z)$ is the horizontal cross-section area at the distance z in the layer or sublayer x, which is calculated according to the geometry information, including the heat spreading angle, of the layer or sublayer [30].

For the solder crack condition illustrated in Fig. 4, the $A_x(z)$ in the pattern and ceramic layer or sublayer shown can be calculated by:

$$A_x(z) = (l_x + 2z \tan\theta_x)^2 \tag{6}$$

where l_x is the side length of the area of the EHPP through the top surface of the layer or sublayer x. Their thermal resistances and capacitances after some manipulations of the symbolic integration (4) and (5) can be calculated by:

$$R_{th,x} = \frac{d_x}{k_x l_x (l_x + 2d_x \tan\theta_x)} \tag{7}$$

$$C_{th,x} = c_{v,x}\left(l_x^2 d_x + 2l_x d_x^2 \tan\theta_x + \frac{4}{3} d_x^3 \tan^2\theta_x\right) \tag{8}$$

Due to the limited distance between parallel dies, the EHPP typically cannot further expand between the two dies in the substrate copper layer. As illustrated in Fig. 4, the EHPP in the substrate copper layer expands from three of the four top sides of the layer, excluding the side between two dies. The parameters of the substrate copper layer can be calculated as follows:

$$A_{sub,cop}(z) = (l_c + z\tan\theta_{adj1})(l_c + 2z\tan\theta_{adj2}) \tag{9}$$

$$R_{sub,cop} = \frac{1}{k_{cop}(2l_c \tan\theta_{adj2} - l_c \tan\theta_{adj1})} \ln \frac{l_c^2 + 2l_c d_{sub,cop} \tan\theta_{adj2}}{l_c^2 + l_c d_{sub,cop} \tan\theta_{adj1}} \tag{10}$$

$$C_{sub,cop} = c_{v,cop} d_{sub,cop} \cdot \left(l_c^2 + \frac{2}{3} d_{sub,cop}^2 \tan\theta_{adj1} \tan\theta_{adj2} + \frac{1}{2} l_c d_{sub,cop} \tan\theta_{adj1} + l_c d_{sub,cop} \tan\theta_{adj2}\right) \tag{11}$$

where k_{cop} and $c_{v,cop}$ are the thermal conductivity and volumetric specific heat of copper. The parameters of the baseplate can be calculated using similar equations:

$$A_{bp} = (l_{bp1} + z\tan\theta_{bp})(l_{bp2} + 2z\tan\theta_{bp}) \tag{12}$$

$$R_{bp} = \frac{1}{k_{cop}(2l_{bp1} - l_{bp2})\tan\theta_{bp}} \ln \frac{l_{bp1} l_{bp2} + 2l_{bp1} d_{bp} \tan\theta_{bp}}{l_c^2 + l_{bp2} d_{bp} \tan\theta_{bp}} \tag{13}$$

$$C_{bp} = c_{v,cop} d_{bp} \cdot \left(l_{bp1} l_{bp2} + \frac{2}{3} d_{bp}^2 \tan^2\theta_{bp} + l_{bp1} d_{bp} \tan\theta_{bp} + \frac{1}{2} l_{bp2} d_{bp} \tan\theta_{bp}\right) \tag{14}$$

where d_{bp} is the thickness of the baseplate layer, and l_{bp1} and l_{bp2} are the top side lengths of the EHPP through the baseplate calculated by:

$$l_{bp1} = l_{r1} \tag{15}$$

$$l_{bp2} = l_{r2} \tag{16}$$

The proposed EHPP-based real-time parameter adaption process for the TEC model is illustrated in Fig. 6. First, T_{cdie}, T_{cside}, and T_a are acquired to calculate k_{cs} using (1). If there is a change in k_{cs}, it indicates a change in the substrate solder health status. Then, A_r is determined using the lookup table that relates k_{cs} to A_r built offline, as described in Section II. Once A_r is updated, l_{r1} and l_{r2} are known. Then, θ_{adj1} and θ_{adj2} can be recalculated using (2) and (3), respectively. With the updated θ_{adj1} and θ_{adj2}, the RC parameters of the substrate copper and baseplate layers can be updated using (9)-(16). The RC parameters of the substrate solder layer can be simply recalculated by substituting $A_x(z)$ with A_r in (4) and (5). It should be noted that the whole parameter adaption process requires neither power loss calculation nor junction temperature information. Therefore, the RC parameters of the proposed TEC model can be easily updated at any operation condition of the power converter and any junction temperature of the IGBT.

IV. Simulation Validation

A commercial half-bridge IGBT module CM400DY-12NF made by POWEREX is studied to validate the proposed EHPP-based real-time adaptive TEC model. The geometry information of the module is provided by POWEREX. Each IGBT switch consists of two parallel dies placed on a direct bond copper (DBC) substrate stack.

An FEA thermal model of the test IGBT module, as shown in Fig. 7, is built in Autodesk Simulation Multiphysics, which is a commercial FEA software platform. In the FEA thermal

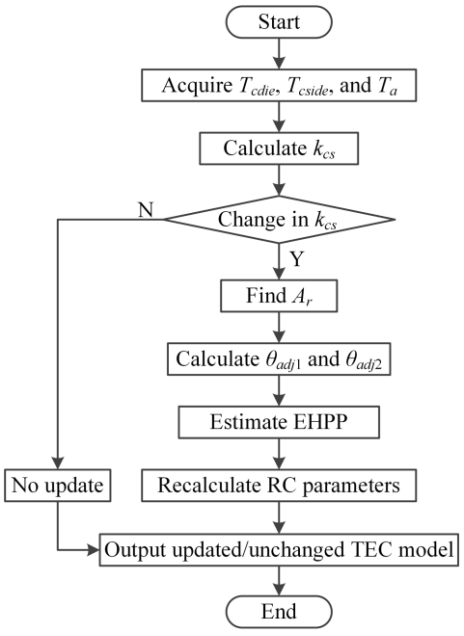

Fig. 6. Flowchart of the proposed EHPP-based real-time parameter adaption process for the TEC model.

model, a fine mesh is used for the IGBT module; while a relatively coarse mesh with 20044 nodes is used for the cold plate. The total mesh of the FEA thermal model of the IGBT module with the cold plate has 79787 nodes. The IGBT module is operated as a leg in a two-level three-phase inverter with the following operating condition: the DC-link voltage is 400V, I_c = 400 A, f_{sw} = 5 kHz, the power factor PF = 0.8, the modulation index M = 1, and the line frequency f_o = 60 Hz.

The substrate solder is assumed to have a uniform crack from the edge to the center (as the results in [25] suggest). Fig. 8 illustrates the geometry of the IGBT module viewing from the baseplate with the locations of the case temperature measuring points. Since the two dies are connected in parallel in one switch, the power losses generated by the two dies are assumed to be the same.

The effectiveness of using the nonuniformity of the case temperature distribution k_{cs} as an indicator of substrate solder aging is evaluated by the FEA thermal model for five solder crack statuses: 1) healthy condition; 2) a slight aging in the substrate solder with a 2 mm crack; 3) a minor aging in the substrate solder with a 4 mm crack; 4) an intermediate aging of the substrate solder with a 5 mm crack; and 5) a dangerous aging status with a 6 mm crack in the substrate solder. As shown in Fig. 9, the thermal resistance from junction to case, R_{thjc}, and the degree of the nonuniformity of the case temperature distribution, k_{cs}, increase with the development of the substrate solder crack. The increases in R_{thjc} and k_{cs} in the 2 mm solder crack case are not noticeable. However, in the next two statuses where the solder cracks become more severe, both R_{thjc} and k_{cs} increase more noticeably. Compared to the healthy case, the values of k_{cs} and R_{thjc} increase by 16.3% and 22.9%, respectively, in the dangerous 6 mm solder crack case.

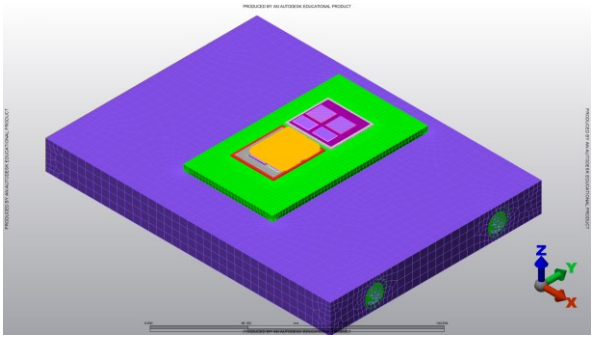

Fig. 7. The FEA thermal model of a CM400 IGBT module built in Autodesk Simulation Multiphysics.

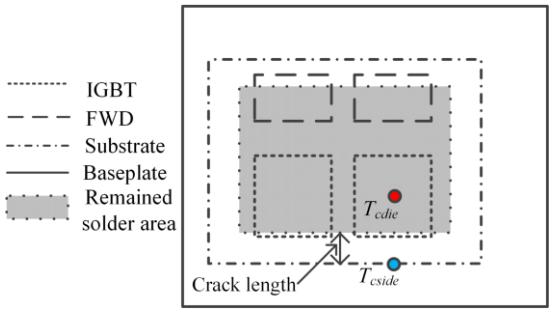

Fig. 8. Baseplate side view of a half of the IGBT module.

These results prove that k_{cs} is a sensitive indicator of the substrate solder aging process and the value of R_{thjc} should be adjusted during the substrate solder aging process.

Then, the process illustrated in Fig. 6 is used to update the RC parameters of the proposed adaptive thermal model for the five substrate solder crack statuses. The values of the adaptive RC parameters for the substrate copper, substrate solder, and baseplate layers and R_{thjc} at the five solder crack statuses are listed in Table I. It can be seen that the RC parameters of the substrate copper layer only change slightly as the solder crack develops. The increases in $R_{sub,sol}$ and R_{bp} contribute to the majority of the increase in R_{thjc}. Fig. 10 compares the values of R_{thjc} calculated by the FEA thermal model and the proposed adaptive thermal model. The results show a good match between the two models, where the error between the two models is less than 3%.

To examine the performance of the proposed adaptive thermal model for real-time dynamic junction temperature

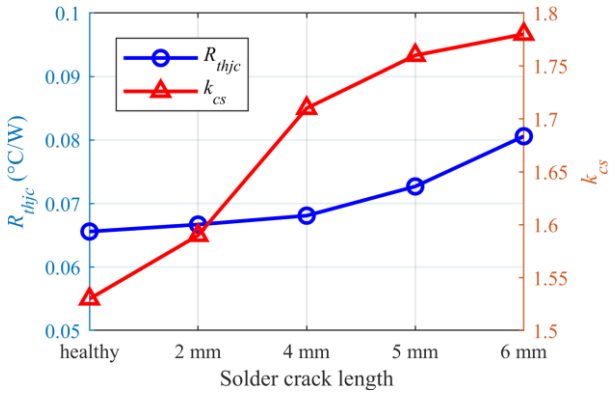

Fig. 9. Evolution of R_{thjc} and k_{cs} during the substrate solder crack development.

TABLE I
CALCULATED ADAPTIVE RC PARAMETERS AT DIFFERENT SOLDER CRACK STATUSES

Crack length (mm)	0	2	4	5	6
$R_{sub,cop}$ (°C/W)	0.0020	0.0020	0.0021	0.0022	0.0024
$R_{sub,sol}$ (°C/W)	0.0137	0.0137	0.0143	0.0159	0.0189
R_{bp} (°C/W)	0.0202	0.0202	0.0210	0.0229	0.0264
$C_{sub,cop}$ (J/°C)	0.2794	0.2794	0.2730	0.2592	0.2390
$C_{sub,sol}$ (J/°C)	0.1770	0.1770	0.1692	0.1526	0.1286
C_{bp} (J/°C)	2.4754	2.4754	2.3826	2.1878	1.9140
R_{thjc} (J/°C)	0.0665	0.0665	0.0680	0.0716	0.0782

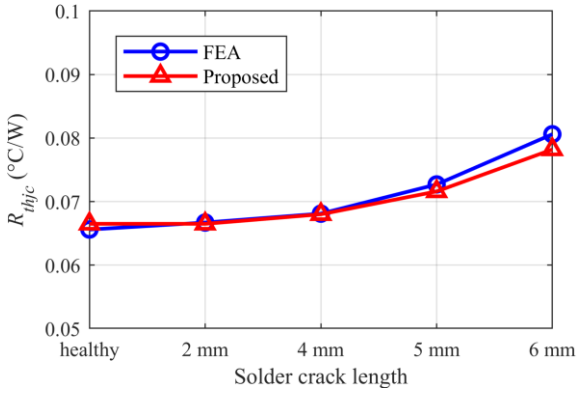

Fig. 10. Comparison of R_{thjc} calculated by the FEA method and the proposed model.

estimation, the junction-to-case temperature difference ΔT_{jc} obtained from the FEA thermal model, the proposed adaptive TEC model, and a traditional Cauer-type TEC model are compared in Fig. 11 for the healthy, 4 mm crack, 5 mm crack, and 6 mm crack statuses. In the traditional TEC model, each layer in the IGBT module is modelled by an RC pair with fixed values. Though the traditional TEC model is not as accurate as the improved Cauer-type TEC, it can provide fairly good estimation when the device is healthy. However, with the development of the solder crack, the maximum error of the traditional TEC model with respect to the FEA model increased to 6 ℃ and 8.5 ℃ at 5 mm and 6 mm crack statuses, respectively. For the healthy and 4 mm crack statuses, the maximum error of the proposed model with respect to the FEA model is around 1 ℃. When the crack increases to 5 mm, the maximum error of the proposed model is only 1.6 ℃, which is less than 25% of the traditional TEC model. For the dangerous 6 mm crack, the maximum error of the proposed model is less than 2 ℃, which is only 5% of the maximum junction-to-case temperature difference and is less than 24% of the traditional TEC model. These results clearly show that the proposed adaptive TEC model is superior to the traditional TEC model and can accurately estimate the junction temperature in real time over the IGBT module's lifespan by considering the substrate solder aging effect using the proposed EHPP-based parameter adaption method.

V. Experimental Validation

Experimental tests are conducted to further validate the proposed adaptive TEC model and method. Fig. 12 shows the experiment setup, which consists of an oscilloscope for steady-state and transient electrical signal acquisition, such as I_c and V_{ce}, a DC source for generating gate signals for the test IGBT module, a programmable high-power DC source for providing test currents, a liquid recirculating chiller for providing the inlet coolant at 20 °C for cooling the IGBT module via a cold plate, a National Instruments (NI) data acquisition system for acquiring T_j, T_{cdie} and T_{cside} measured by thermocouples with insulation, and a control system developed in LabVIEW™ operating on a desktop computer. A thermocouple is carefully attached on the top surface of an IGBT die for measuring T_j. The locations of the two case temperature measuring points are show in Fig. 13. Shallow grooves filled with thermal grease are carved on the bottom surface of the baseplate for installation of the thermocouples.

A thermal cycling test is designed to accelerate the aging process of the substrate solder, where the thermal cycles are excited by the power loss in the IGBT module. The IGBT module is placed on an air-cooled heatsink, as shown in Fig. 14, and is powered by a relatively small current pulse of 80 A through each of the two switches. In each thermal cycle, the 80 A current is applied to the IGBT module for 3 minutes to gradually heat it up while keeping T_j below 125 °C. Then, the

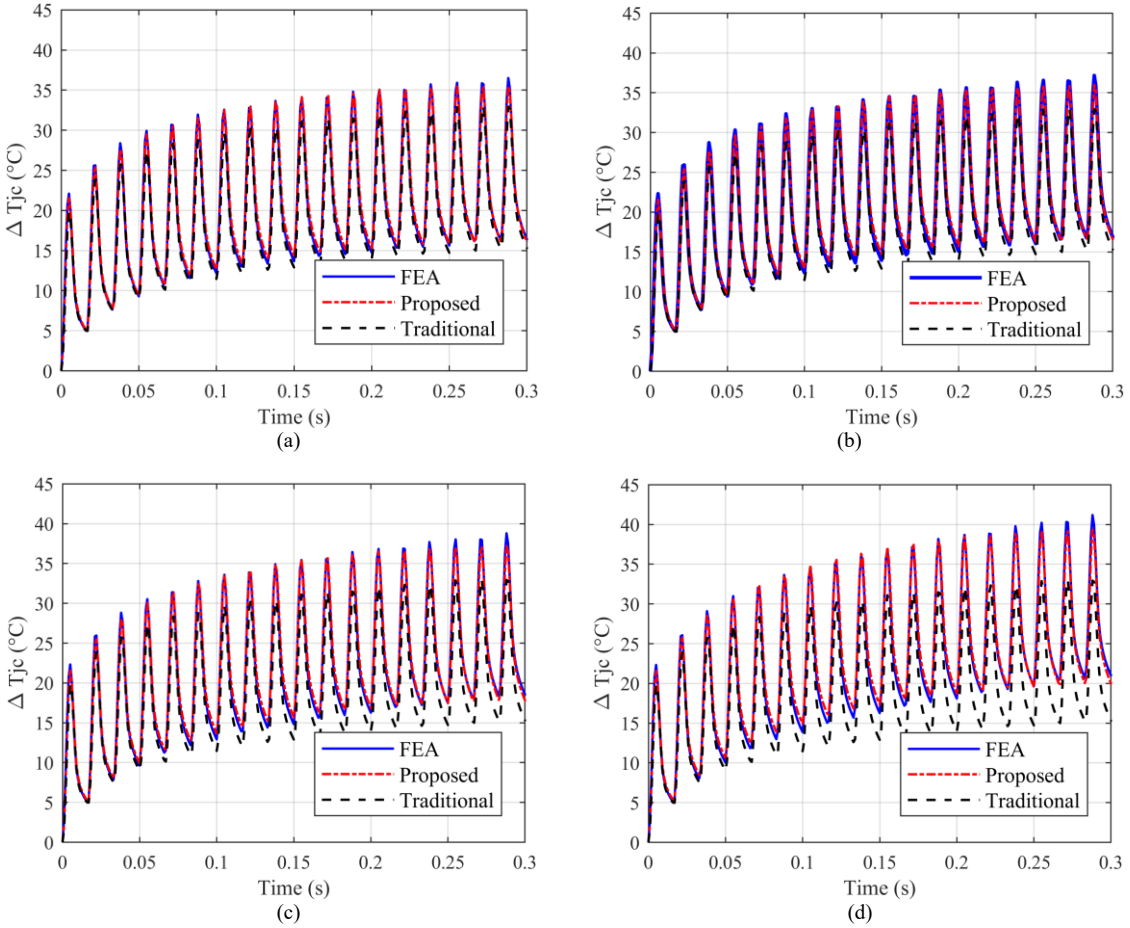

Fig. 11. Comparison of $\Delta T_{jc}(t)$ estimated by the FEA thermal model, the proposed adaptive TEC model, and a traditional Cauer-type TEC model for different solder crack statuses: (a) healthy; (b) 4 mm solder crack; (c) 5 mm solder crack; and (d) 6 mm solder crack.

IGBT module is cooled down in the next 5 minutes. The variation of T_{cside} in one thermal cycle is about 80 °C.

The thermal cycling test is interrupted after certain cycles to: 1) inspect the changes of R_{thjce} and k_{cs}; and 2) examine the performance of the proposed adaptive TEC model by comparing the junction temperatures estimated by the model and measured by thermocouples. During the inspection test, the IGBT module is remounted on the cold plate with the mounting torque recommended by the datasheet and is powered by a 200A DC current. The value of R_{thjce} is calculated using the measured T_j, T_{cdie}, and V_{ce}. The test results are shown in Fig. 15. After 2600 thermal cycles, R_{thjc} only increases by 6.5% from 0.0659 °C/W to 0.0702 °C/W, and the value of k_{cs} increases by 9.6%. After that R_{thjc} increases by 10.9% and k_{cs} increases by 11.5% after 4600 thermal cycles. Finally, k_{cs} increases by 14.1%, while R_{thjc} increases by 15.2% at the end of the test. The trend of change of k_{cs} obtained from the experiment agrees with that from the simulation. The last two values of k_{cs} indicate that maintenance may be needed for the IGBT module. The experimental results prove that the substrate solder aging of the IGBT module can be effectively monitored by the proposed method using k_{cs}.

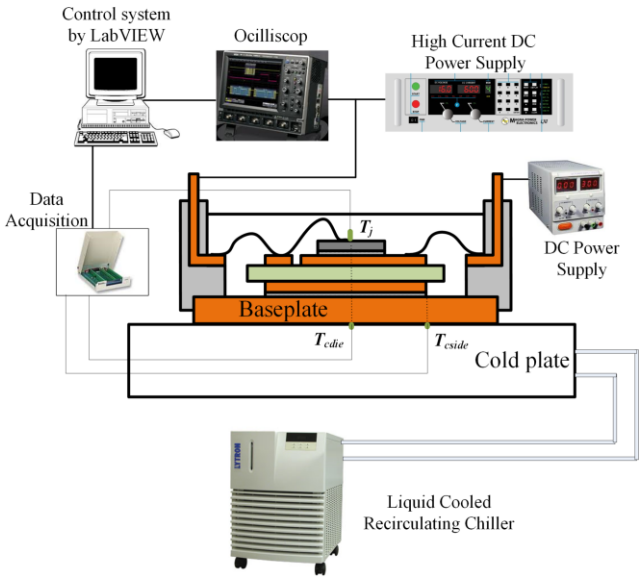

Fig. 12. Experiment setup for validation of the proposed adaptive TEC model and method.

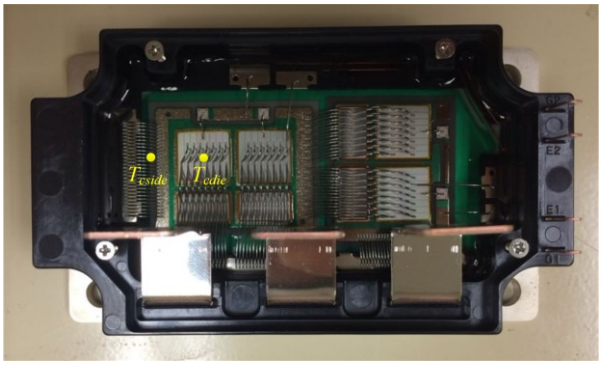

Fig. 13. The test IGBT module with the positions of the two thermal sensors placed on the bottom surface of the baseplate (top view from the upper side of the module).

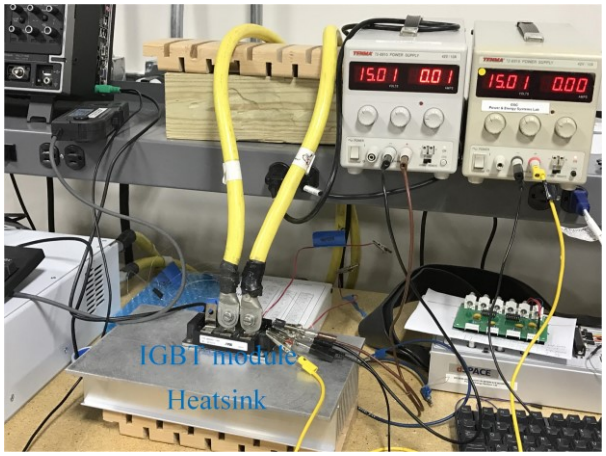

Fig. 14. The IGBT module placed on an air-cooled heatsink.

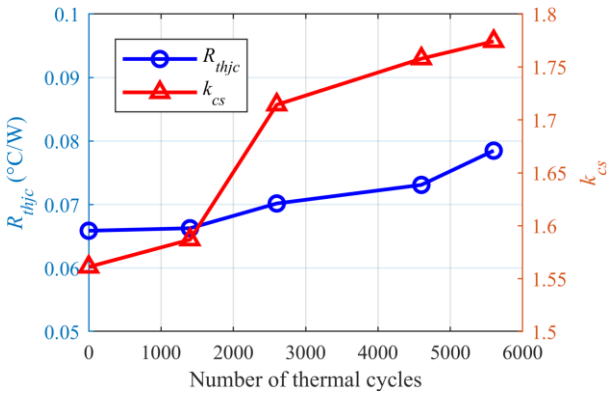

Fig. 15. Evolution of R_{thjc} and k_{cs} during the thermal cycling test of the IGBT module.

TABLE II
INTERPOLATED SOLDER CRACK LENGTH AND CALCULATED ADAPTIVE RC PARAMETERS

Number of cycles	0	1400	2600	4600	5600
Calculated k_{cs}	1.5612	1.5869	1.7143	1.7578	1.7742
Crack length (mm)	1.0054	1.9245	4.0423	4.8484	5.6828
$R_{sub,cop}$ (°C/W)	0.0020	0.0020	0.0021	0.0022	0.0023
$R_{sub,sol}$ (°C/W)	0.0137	0.0137	0.0144	0.0155	0.0178
R_{bp} (°C/W)	0.0202	0.0202	0.0211	0.0225	0.0252
$C_{sub,cop}$ (J/°C)	0.2794	0.2794	0.2726	0.2624	0.2452
$C_{sub,sol}$ (J/°C)	0.1770	0.1770	0.1688	0.1564	0.1360
C_{bp} (J/°C)	2.4754	2.4754	2.3760	2.2310	1.9990
R_{thjc} (J/°C)	0.0665	0.0665	0.0681	0.0707	0.0759

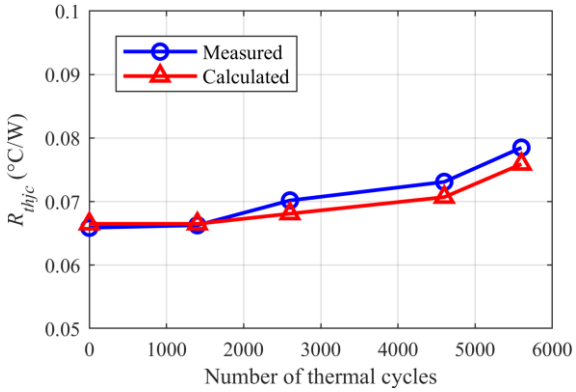

Fig. 16. Comparison of measured and calculated values of R_{thjc} during the thermal cycling test of the IGBT module.

The relationship between the substrate solder crack length and the measured value of k_{cs} is obtained by interpolating the FEA results shown in Fig. 9. Then, A_r is determined and the parameters of the proposed adaptive TEC model are updated in real time using the EHPP-based method proposed in Section III. The interpolated crack lengths based on k_{cs} and recalculated RC parameters are listed in Table II. Fig. 16 compares the measured and calculated values of R_{thjc}. The maximum error occurs at the 4600th thermal cycle, but is still less than 3.5%. The results show that the value of R_{thjc} during the substrate solder aging process is updated accurately by using the proposed EHPP-based method.

The transient performance of the proposed adaptive TEC model is examined by comparing with the traditional Cauer-type TEC model when the IGBT module conducts a 150 A and a 300 A currents alternately every 2 s. The power loss of the IGBT is calculated by multiplying I_c and V_{ce}, which are captured by the oscilloscope. In real-world applications, the power loss can be obtained by using the power converter's operating conditions, lookup tables of the output characteristic and switching energies of the IGBT, and estimated T_j. As the proposed method does not require P_{loss} and T_j to update the RC parameters of the thermal model, the P_{loss} and T_j can be calculated iteratively following the steps in [31] once the thermal model is updated. As the increase in R_{thjc} during the first 1400 thermal cycles is negligible, only the results in four of the five health statuses are compared in Fig. 17. When the substrate solder is healthy, the values of T_j estimated by the proposed and traditional models are both very close to the measured T_j. At the 2600th and 4600th thermal cycles, the maximum errors of the estimated T_j with respect to the measured T_j are only around 2.5 °C when using the proposed model, but increase to 5 °C and 9 °C, respectively, when using the traditional model. At the end of the test, the peak T_j increases from 91 °C to 104 °C, which is underestimated by only 2.5 °C by the proposed model but is underestimated by 14 °C by the traditional model. The results show that the proposed adaptive thermal model can provide much more accurate junction temperature estimation during the transient thermal cycling process and different substrate solder aging statues of the IGBT module. The traditional model, however, will significantly underestimate the junction temperature during the substrate solder aging process and, therefore, may fail to trigger the alarm to prevent possible overtemperature failure of the power converter.

VI. Conclusion

This paper presented an EHPP-based TEC model for IGBT modules, where the parameters of the model were made adaptive online and in real time to substrate solder cracks inside the IGBT modules. The concept of the EHPP was introduced to effectively characterize the thermal behavior of IGBT modules using the heat spreading angle technique. The impact of substrate solder cracks on the thermal behavior of IGBT module was then interpreted by using the change of the EHPP approximated based on the change of the nonuniformity

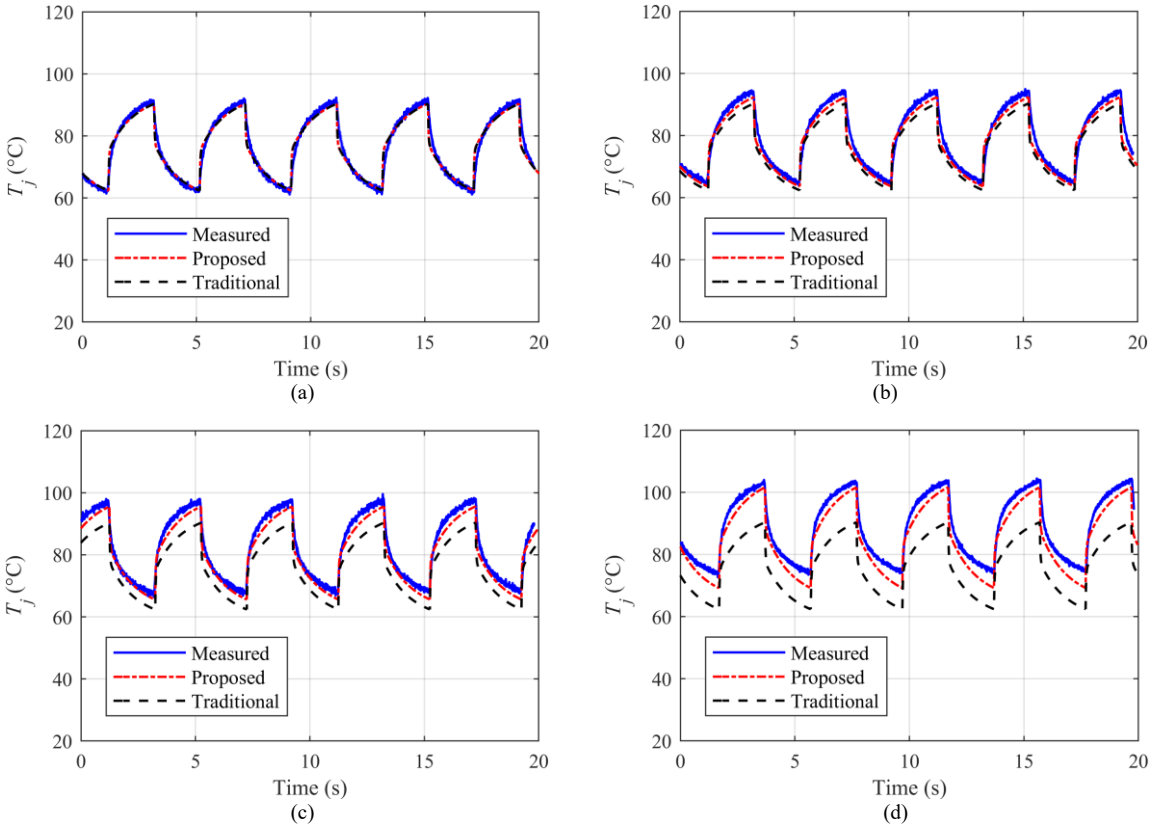

Fig. 17. Comparison of the measured $T_j(t)$ and the $T_j(t)$ estimated by the proposed adaptive TEC model and a traditional Cauer-type TEC model at different thermal cycles: (a) healthy substrate solder; (b) 2600 thermal cycles (R_{thjc} increased by 6.5%); (c) 4600 thermal cycles (R_{thjc} increased by 11%); and (d) 5600 thermal cycles (R_{thjc} increased by 15.2%).

of the case temperature distribution. The approximated EHPP was then used to adapt the RC parameters of the TEC model online and in real time. Simulation studies and experimental tests have validated the effectiveness of using the nonuniformity of the case temperature distribution to indicate the severity of substrate solder cracks and the effectiveness of using the proposed adaptive thermal model to achieve improved junction temperature estimation during the solder aging process of the IGBT module. The proposed model can be used for effective online condition monitoring, control, and thermal and health management of IGBT modules and associated power electronic systems.

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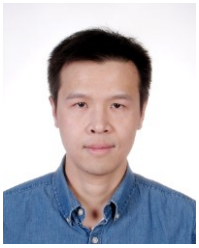

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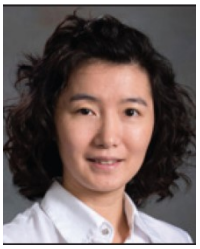

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