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Run-time Mapping of Spiking Neural Networks to Neuromorphic Hardware

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Abstract

Neuromorphic architectures implement biological neurons and synapses to execute machine learning algorithms with spiking neurons and bio-inspired learning algorithms. These architectures are energy efficient and therefore, suitable for cognitive information processing on resource and power-constrained environments, ones where sensor and edge nodes of internet-of-things (IoT) operate. To map a spiking neural network (SNN) to a neuromorphic architecture, prior works have proposed design-time based solutions, where the SNN is first analyzed offline using representative data and then mapped to the hardware to optimize some objective functions such as minimizing spike communication or maximizing resource utilization. In many emerging applications, machine learning models may change based on the input using some online learning rules. In online learning, new connections may form or existing connections may disappear at run-time based on input excitation. Therefore, an already mapped SNN may need to be re-mapped to the neuromorphic hardware to ensure optimal performance. Unfortunately, due to the high computation time, design-time based approaches are not suitable for remapping a machine learning model at run-time after every learning epoch. In this paper, we propose a design methodology to partition and map the neurons and synapses of online learning SNN-based applications to neuromorphic architectures at run-time. Our design methodology operates in two steps – step 1 is a layer-wise greedy approach to partition SNNs into clusters of neurons and synapses incorporating the constraints of the neuromorphic architecture, and step 2 is a hill-climbing optimization algorithm that minimizes the total spikes communicated between clusters, improving energy consumption on the shared interconnect of the architecture. We conduct experiments to evaluate the feasibility of our algorithm using synthetic and realistic SNN-based applications. We demonstrate that our algorithm reduces SNN mapping time by an average 780x compared to a state-of-the-art design-time based SNN partitioning approach with only 6.25% lower solution quality.

Keywords Spiking Neural Networks (SNN) · Neuromorphic computing · Internet of Things (IoT) · Run-time · Mapping

1 Introduction

Internet of things (IoT) is an emerging computing paradigm that enables the integration of ubiquitous sensors over a wireless network [3]. Recent estimates predict that over 50 billion IoT devices will be interconnected via the cloud over the next decade [22]. In a conventional IoT, data collected from sensors and actuators are transferred to the cloud and processed centrally [34]. However, with an increase in the number of connected IoT devices, processing on the cloud becomes the performance and energy bottleneck [41].

Edge computing is emerging as a scalable solution to process large volumes of data by executing machine learning tasks closer to the data source e.g. on a sensor or an edge node [40]. Processing on edge devices allows real-time data processing and decision making, and offers network scalability and privacy benefits as data transferred to the cloud over a possibly insecure communication channel is minimized [31, 32].

Spiking neural networks (SNNs) [29] are extremely energy efficient in executing machine learning tasks on event-driven neuromorphic architectures such as TrueNorth [2], DYNAP-SE [36], and Loihi [19], making them suitable for machine learning-based edge computing. A neuromorphic architecture is typically designed using *crossbars*, which can accommodate only a limited number of synapses per neuron to reduce energy consumption. To build a large neuromorphic chip, multiple crossbars are integrated using

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a shared interconnect such as network-on-chips (NoC) [7]. To map an SNN to these architectures, the common practice is to partition the neurons and synapses of the SNN into clusters and map these clusters to the crossbars, optimizing hardware performance such as minimizing the number of spikes communicated between crossbar, which reduces energy consumption [16].

Most prior works on machine learning-based edge computing focus on supervised approaches, where neural network models are first trained offline with representative data from the field and then deployed on edge devices to perform inference in real-time [39]. However, data collected by IoT sensors constantly evolve over time and may not resemble the representative data used to train the neural network model. This change in the relation between the input data and an offline trained model is referred to as *concept drift* [23]. Eventually, the concept drift will reduce the prediction accuracy of the model over time, lowering its quality. Therefore, there is a clear need to periodically re-train the model using recent data with adaptive learning algorithms. Examples of such algorithms include transfer learning [38], lifelong learning [43] and deep reinforcement learning [33].

Mapping decisions for a supervised SNN are made at design-time before the initial deployment of the trained model. However, in the case of online learning, when the model is re-trained, (1) synaptic connections within the SNN may change, i.e. new connections may form and existing connection may be removed as new events are learned, and (2) weights of existing synaptic connections may undergo changes after every learning epoch. In order to ensure the optimal hardware performance at all times, a *run-time* approach is required that remaps the SNN to the hardware after every learning epoch. Prior methods to partition and map an SNN to neuromorphic hardware, such as PSOPART [16], SpiNeMap [6], PyCARL [4], NEUTRAMS [25] and DFSynthesizer [42] are design-time approaches that require significant exploration time to generate a good solution. Although suitable for mapping supervised machine learning models, these approaches cannot be used at run-time to remap SNNs frequently. For online learning, we propose an approach to perform run-time layer-wise mapping of SNNs on to crossbar-based neuromorphic hardware. The approach is implemented in two steps. First, we perform a layer-wise greedy clustering of the neurons in the SNN. Second, we use an instance of hill-climbing optimization (HCO) to lower the total number of spikes communicated between the crossbars.

Contributions: Following are our key contributions.

- We propose an algorithm to partition and map online learning SNNs on to neuromorphic hardware for IoT applications in run-time;
- We demonstrate suitability of our approach for online mapping in terms of the exploration time and total number of spikes communicated between the crossbars, when compared to a state-of-the-art design time approach.

The remainder of this paper is organized as follows, Section 2 presents the background, Section 3 discusses the problem of partitioning a neural network into clusters to map on to the crossbars neuromorphic hardware and describes our two-step approach. Section 5 presents the experimental results based on synthetic applications. Section 6 concludes the paper followed by a discussion in Section 7.

2 Background

Spiking neural networks are event-driven computational models inspired by the mammalian brain. Spiking neurons are typically implemented using Integrate-and-Fire (I&F) models [9] and communicate using short impulses, called *spikes*, via synapses. Figure 1a illustrates an SNN with *two* pre-synaptic neurons connected to a post-synaptic neuron via synaptic elements with weights $w1$, $w2$ respectively. When a pre-synaptic neuron generates a spike, current is injected into the post-synaptic neuron, proportional to the product of the spike voltage and the conductance of the respective synapse. SNNs are trained by adjusting the

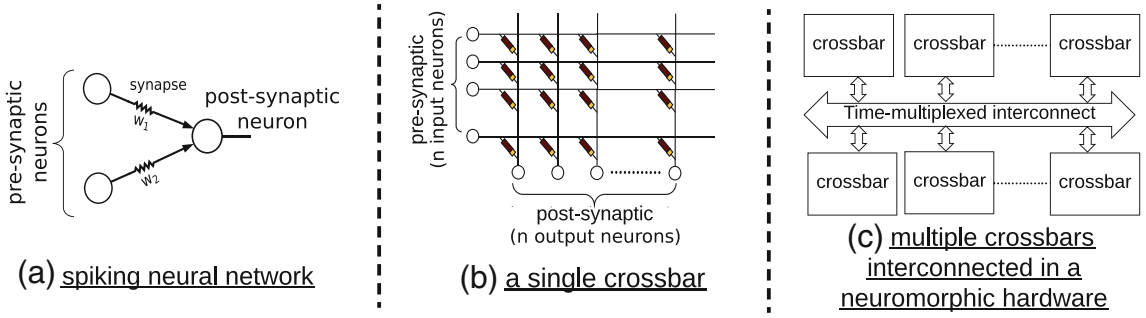

Figure 1 Overview of a SNN hardware: **a** connection of pre- and post-synaptic neurons via synapses in a spiking neural network, **b** a crossbar organization with fully connected pre- and post-synaptic neurons, and **c** a modern neuromorphic hardware with multiple crossbars and a time-multiplexed interconnect.

synaptic weights using a supervised, a semi-supervised, or an unsupervised approach [27, 28, 37].

Due to the ultra-low power footprint of neuromorphic hardware, several machine learning applications based on SNNs are implemented. In [18], the authors propose a multi-layer perceptron (MLP) based SNN to classify heartbeats using electrocardiagram (ECG) data. In [21], the authors propose the handwritten digit recognition using unsupervised SNNs. In [15], a spiking liquid state machine for heart-rate estimation is proposed. A SNN-based liquid state machine (LSM) for facial recognition is proposed in [24]. In [5], the authors propose a technique to convert a convolutional neural network (CNN) model for heartbeat classification into a SNN, with a minimal loss in accuracy.

Typically, SNNs are executed on special purpose neuromorphic hardware. These hardware can (1) reduce energy consumption, due to their low-power designs, and (2) improve application throughput, due to their distributed computing architecture. Several digital and mixed-signal neuromorphic hardware are recently developed to execute SNNs, such as Neurogrid [8], TrueNorth [1] and DYNAP-SE [35]. Although these hardware differ in their operation (analog vs. digital), they all support crossbar-based architectures. A crossbar is a two-dimensional arrangement of synapses (n^2 synapses for n neurons). Figure 1b illustrates a single crossbar with n pre-synaptic neurons and n post-synaptic neurons. The pre- and post-synaptic neurons are connected via synaptic elements. Crossbar size (n) is limited (<512) as scaling the size of the crossbar will lead to an exponential increase in dynamic and leakage energy. Therefore, to build large neuromorphic hardware, multiple crossbars are integrated using a shared interconnect, as illustrated in Figure 1c.

In order to execute an SNN on a neuromorphic hardware, the SNN is first partitioned into clusters of neurons and synapses. The clustered (local) synapses are then mapped to the crossbars and the inter-cluster synapses to the time-multiplexed interconnect. Several design time partitioning approach are presented in literature. In [44–46] the authors proposes techniques to efficiently map the neurons and synapses on a crossbar. The aim of these techniques is to maximize the utilization of the crossbar. NEUTRAMS partitions the SNN for crossbar-based neuromorphic hardware [26]. The NEUTRAMs approach also looks to minimize the energy consumption of the neuromorphic hardware executing the SNN. PyCARL [4] facilitates the hardware-software co-simulation of SNN-based applications. The framework allows users to analyze and optimize the partitioning and mapping of an SNN on cycle-accurate models of neuromorphic hardware. DFSynthesizer [42] uses a greedy technique to partition the neurons and synapses of an SNN. The SNN partitions are mapped to the neuromorphic hardware using an algorithm that adapts to the available resources of the hardware. SpiNeMap [6] uses a greedy partitioning technique to partition the SNN followed by a meta-heuristic-based technique to map the partitions on the hardware. PSOPART SNNs to a crossbar architecture [17]. The objective of SpiNeMap and PSOPART is to minimize the spike communication on the time-multiplexed interconnect in order to improve the overall latency and power consumption of the DYNAP-SE hardware. Table 1 compares our contributions to the state-of-the-art techniques.

As these partitioning approaches aim to find the optimal hardware performance, their exploration time is relatively large and therefore not suitable for partitioning and re-mapping of online learning SNNs. Run-time approaches are proposed for task mapping on multiprocessor systems. A heuristic-based run-time manager is proposed in [12]. The run-time manager controls the thread allocation and voltage/frequency scaling for energy efficient execution of applications on multi processor systems. In [30], the authors propose a genetic algorithm-based run-time manager to schedule real-time tasks on Dynamic Voltage Scaling (DVS) enabled processors, with an aim to minimize energy consumption. A workload aware thread scheduler is proposed in [20] for multi-processor systems. In [14], the authors propose a multinomial logistic regression model to partition the input workload in run-time. Each partition is then executed at pre-determined frequencies to ensure minimum energy consumption. In [13], the authors propose a technique to remap tasks run on faulty processors with a minimal migration overhead. A thermal-aware task scheduling approach is proposed in [11] to estimate and reduce the temperature of the multi processor system at

Table 1 Summary of related works.

Related works	Run-time mapping	Objective
[44–46]	×	Maximize single crossbar utilization
NEUTRAMS [25]	×	Minimize number of crossbars utilized
SpiNeMap [6]	×	Minimize spikes on time-multiplexed interconnect
PSOPART [16]	×	Minimize spikes on time-multiplexed interconnect
DFSynthesizer [42]	×	Optimize the hardware utilization in run-time
Proposed	√	Reduces energy consumption of online learning SNNs on hardware.

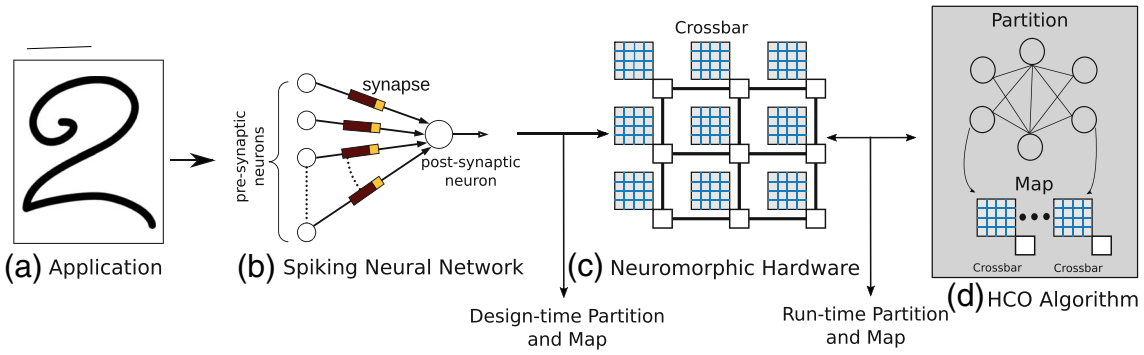

Figure 2 Mapping of online learning SNN on Neuromorphic Hardware.

run-time. The technique performs an extensive design-time analysis of fault scenarios and determines the optimal mapping of tasks in run-time. However, such run-time techniques to remap SNN on neuromorphic hardware are not proposed. To the best of our knowledge, this is the first work to propose a run-time mapping approach with a significantly lower execution time when compared to existing design-time approaches. Our technique reduces the spikes communicated on the time-multiplexed interconnect, therefore reducing the energy consumption.

3 Methodology

The proposed method to partition and map an SNN in run-time is illustrated in Figure 2 illustrates. The network model is built using a directed graph, wherein each edge represents a synapse whose weight is the total number of spikes communicated between the two SNN neurons. The input to the mapping algorithm is a list of all the neurons *(A)*, the total number of spikes communicated over each synapse and the size of a crossbar *(k)*. The mapping algorithm is split into two steps, as shown in Figure 3.

Figure 4 illustrates the partitioning of an SNN with 6 neurons into 3 sub-lists. The spikes communicated between the neurons is indicated on the synapse. First, we divide the input list of neurons into sub-lists (Section 3.1), such that each sub-list can be mapped to an available crossbar. Second, we reduce the number of spikes communicated between the sub-lists (Section 3.2), by moving the neurons between the sub-list (indicated in blue).

3.1 Building Sub-lists

Algorithm 1 describes the greedy partitioning approach. The objective is to greedily cut the input list of neurons *(A)* into s sub-lists, where s is the total number of crossbars in the given design. The size of a sub-list is determined by the size of the crossbars *(k)* on the target hardware. A variable *margin (line 3)* is defined to store the unused neuron slots available in each sub-list. The *mean (line 4)* number of spikes generated per crossbar is computed using the total number of spikes communicated in the SNN-based application. A *cost* function (Algorithm 2) is defined to compute the total number of spikes communicated (cost) between each of the sub-lists.

The algorithm iterates over the neurons (n_i) in the input list (A) and updates the slots in the current sub-list *(line 8)*. Neurons are added to the current sub-list until one of following two criteria are met - (1) the length of the sub-list equals k, or (2) the cost (number of spikes) is greater than the *mean* value and sufficient extra slots ($margin$) are still available. When the criteria is met, the current sublist is validated and its boundary stored. When the penultimate sub-list is validated, the execution ends because the boundary of the last sub-lists is already known (nth element in list). The list p contains the sub-lists boundaries.

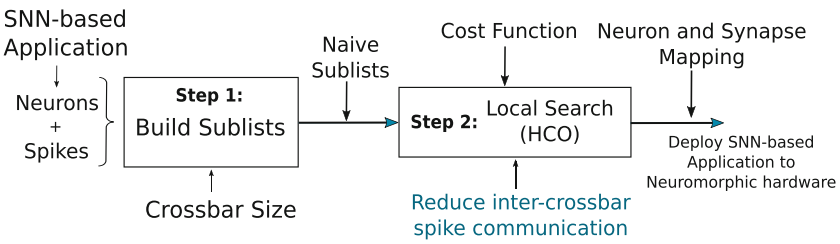

Figure 3 Overview of proposed partitioning algorithm.

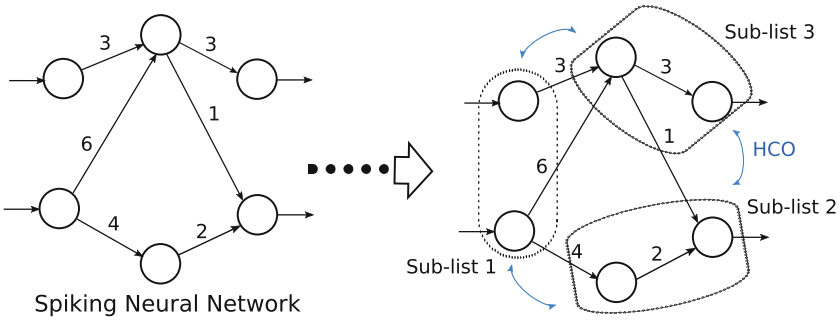

Figure 4 Partitioning of an SNN.

Algorithm 1 Building sublists.

```
1  procedure FUNCTION (A[1 → n])
2  foreach Crossbar s ∈ p do
       /* iterate over all crossbars in p   */
3      Input the variable margin;
       /* Mean spikes per crossbar          */
4      Compute Mean;
       /* iterate over all neurons in A     */
5      foreach n_i ∈ A do
           /* Cost is the number of spikes in
              current cluster                */
6          Compute Cost;
7          while Cost ≤ Mean do
8              Assign n_i to crossbar p;
9          end
10     end
11 end
```

Algorithm 2 Cost function.

```
1  procedure FUNCTION (A[1 → n], p[1 → s])
2  max ← 0;
3  foreach Cluster (p[i]) do
4      sum ← 0 ;
5      foreach n in p[i] do
           /* total spikes communicated      */
6          compute Sum;
7      end
8      if Sum > Max then
9          Max ← Sum;
10     end
11 end
```

Algorithm 3 Hill climbing algorithm.

```
1  procedure FUNCTION (A[1 → n], p[1 → s])
   /* compute the initial cost              */
2  compute Cost;
3  foreach n in A do
4      move n across cluster boundary;
5      compute new Cost C_n;
6      select min(C_n);
7  end
   /* end 2-part procedure                  */
```

3.2 Local Search

The solution obtained from Algorithm-1 is naive and not optimal. Although each sublist s obtained from Algorithm-1 meets the cost criteria, it is possible to have unevenly distributed costs across the sublists. We search for a better solution by performing multiple local searches to balance the cost. This is done by using the hill-climbing optimization technique to iterate through the sublist and *move* its boundary

Algorithm 3 describes the hill-climbing optimization technique. The technique relies on a *cost function (line 2)* to compute and evaluate a solution. The cost function used in the optimization process is shown in Algorithm 2. The cost function computes the maximum cost (number of spikes) for a chosen sub-list. The optimal solution should contain the lowest cost. The algorithm iterates through each subslist to search for the best solution (cost) of its neighbors. The algorithm begins by moving the boundary of a sub-list one position to the left or one position to the right. Each neuron (n_i) in the sublist is moved across the boundary to a neighboring sub-list and the *cost* of the neighbors are computed. The algorithm selects the solution with the local minimum cost. The process is repeated for every neuron in the list (A) until the sub-lists with the minimum cost is found.

4 Evaluation

4.1 Simulation Environment

We conduct all experiments on a system with 8 CPUs, 32GB RAM, and NVIDIA Tesla GPU, running Ubuntu 16.04.

- **CARLsim** [10] : A GPU accelerated simulator used to train and test SNN-based applications. CARLsim reports spike times for every synapse in the SNN.
- **DYNAP-SE** [36]: Our approach is evaluated using the DYNAP-SE model, with 256-neuron crossbars interconnected using a NoC. [47].

Table 2 Applications used for evaluating.

Category	Applications	Synapses	Topology	Spikes
synthetic	S_1000	240,000	FeedForward (400, 400, 100)	5,948,200
	S_2000	640,000	FeedForward (800, 400, 800)	45,807,200
realistic	EdgeDet [10]	272,628	FeedForward (4096, 1024, 1024, 1024)	22,780
	MLP-MNIST [21]	79,400	FeedForward (784, 100, 10)	2,395,300

4.2 Evaluated Applications

In order to evaluate the online mapping algorithm, we use 2 synthetic and 2 realistic SNN-based applications. Synthetic applications are indicated with an 'S_' followed by the number of neurons in the application. Edge detection (EdgeDet) and MLP-based digit recognition (MLP-MNIST) are the two realistic applications used. Table 2 also indicates the number of synapses (column 3), the topology (column 4) and the number of spikes for the application obtained through simulations using CARLsim [10].

4.3 Evaluated Design-time vs run-time Approach

In order to compare the performance of our proposed run-time approach, we choose a state-of-the-art design-time approach as the baseline. The crossbar size for both the algorithms is set to 256 (k=256).In this paper we compare the following approaches:

- *PSOPART* [16]: The PSOPART approach is a design-time partitioning technique that uses and instance of particle swarm optimization (PSO) to minimize the number of spikes communicated on the time-multiplexed interconnect.
- *HCO-Partitioning*: Our HCO-partitioning approach is a two-step layer-wise partitioning technique with a greedy partitioning followed by a HCO-based local search approach to reduce the number of spikes communicated between the crossbars.

5 Results

Table 3 reports the execution time (in seconds) of the design-time and run-time mapping algorithms for synthetic and realistic applications, respectively. We make the following two observations. *First*, on average, our HCO partitioning algorithm has an execution time 780x lower than that of the PSOPART algorithm. Second, the significantly lower run-time of the HCO partitioning algorithm (<50 seconds) allows for the online learning SNN to be re-mapped on the edge devices, before the start of the next training epoch.

Figure 5 shows the lifetime of an online learning application with respect to the execution times of each training epoch (t) and the HCO partitioning algorithm (h). The execution time of the partitioning algorithm needs to be significantly lower than the time interval between training epochs. This is achieved with the HCO-partitioning algorithm as its execution time is significantly (780x) lower than the state-of-the-art design-time approaches.

In Figure 6, we compare the number of spikes communicated between the crossbars while partitioning the SNN using the HCO partitioning algorithm when compared to the design-time PSOPART approach. We see that, on average, the PSOPART algorithm reduces the number of spikes by a further 6.25%, when compared to the HCO partitioning algorithm. The PSOPART will contribute to a further reduction in the overall energy consumed on the neuromorphic hardware. However, this outcome is expected as the design-time partitioning approach is afforded far more exploration time to minimize the number of spikes communicated between the

Table 3 Execution time of design-time and proposed run-time approach in seconds.

Category	Applications	PSOPART (sec)	HCO-Partition (sec)
synthetic	S_1000	20011.33	19.10
	S_2000	45265.00	24.68
realistic	EdgeDet	6771.02	45.62
	MLP-MNIST	5153.41	11.03

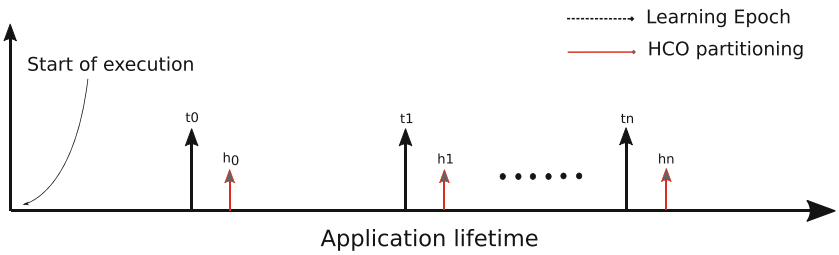

Figure 5 Life-time of online learning SNN.

crossbars. Also, the effects of *concept drift* will soon lead to the design-time solution becoming outmoded. Therefore, a run-time partitioning and re-mapping of the SNN will significantly improve the performance of the SNN on the neuromorhpic hardware and mitigate the effects of *concept drift*.

6 Conclusion

In this paper, we propose an algorithm to re-map online learning SNNs on neuromorphic hardware. Our approach performs the run-time mapping in two steps: (1) a layer-wise greedy partitioning of SNN neurons, and (2) a hill-climbing based optimization of the greedy partitions with an aim to reduce the number of spikes communicated between the crossbars. We demonstrate the in-feasibility of using a state-of-the-art design-time approach to re-map online learning SNNs in run-time. We evaluate the our approach using synthetic and realistic SNN applications. Our algorithm reduces SNN mapping time by an average 780x when compared to a state-of-the-art design-time approach with only 6.25% lower performance.

7 Discussion

In this section we discuss the scalability of our approach. Each iteration of Algorithm-1 performs basic math operations. The hill-climbing algorithm computes as many as 2x(s-2) solutions, and performs a comparison to find the minimum cost across all the solutions. In our case, the co-domain of the cost function are well-ordered positive integers. The cost function is also linear in n, however the hill-climb optimization algorithm only terminates when the local minimum cost function is computed. Therefore, it is in our interest to optimize the number of times the cost function is to be run.

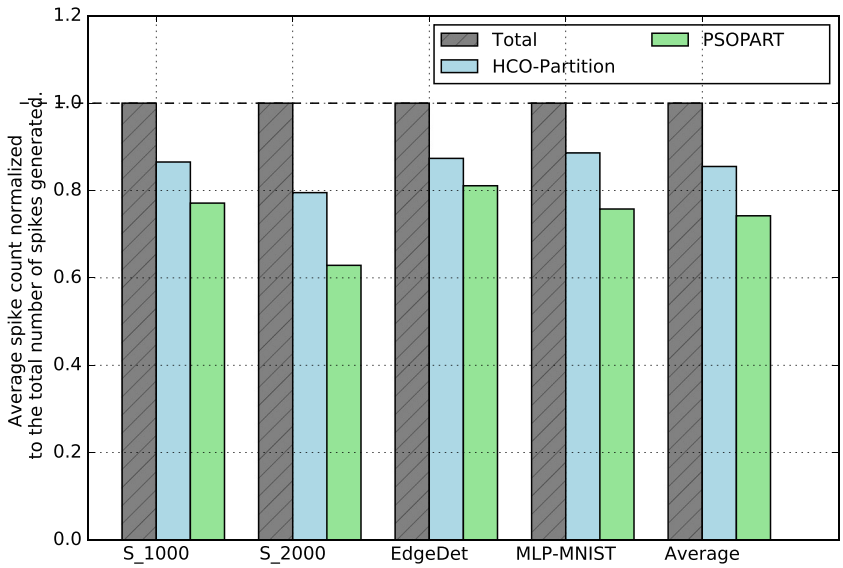

Figure 6 Number of spikes communicated on the time-multiplexed interconnect normalized to the total number of spikes generated.

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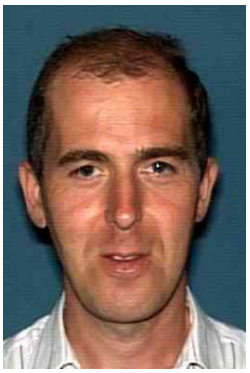

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