A Comprehensive Analysis of Charge-Pump-Based Multi-Stage Multi-Output DC-DC Converters

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***Abstract*—This paper presents an analytical model for calculating the output voltage and the power efficiency of multi-stage multi-output (MSMO) DC-DC converters (DDC) that use charge pump cells for boosting the voltage. Various cases such as multi-output current consumption and its effects on the output voltage and the power efficiency are studied. Based on the model, a tapered design approach is proposed that can bolster the power efficiency and lower the output voltage drop of MSMO DDCs. Moreover, a charge-pump-based DDC is introduced and designed to verify the proposed model. Simulation results using a standard high-voltage 180-nm CMOS technology affirms the accuracy of the presented model.**

***Index Terms*—DC-DC Converter, Multi-Output, Charge-Pump, Power Efficiency, Tapered Design**

I. Introduction

Handheld and portable devices such as wearable or implantable biomedical systems and wireless sensors or actuators for the internet-of-thing (IoT) applications - where a battery or a wireless power link is used to supply power to the system - mandate the use of low-voltage and power-efficient design methods [1], [2]. Even though lowering the supply voltage may seem to be a viable choice in reducing the power consumption and the overall form factor of the system (*e.g.,* shrinking the battery size), higher levels of supply voltage are sometimes required due to the existence of high-power blocks such as neural stimulators, RF power amplifiers, and on-chip flash memories [3], [4], [5]. In particular, brain stimulation circuits in a bidirectional brain-machine interface (BMI) system must use a high-voltage power supply so as to sink/source current from/to the brain tissue. A BMI should often accommodate the use of multiple supply voltages to be able to elicit stimulation in a large group of individuals with various brain-tissue impedances [6]. Therefore, power-efficient DC-DC converters (DDC) are required for all of the aforementioned applications.

A commonly used inductor-less DDC suitable for on-chip implementation is the Dickson charge pump [7]. Various architectures have been implemented based on the Dickson charge pump to improve the power efficiency (η) and mitigate the design challenges (such as voltage drop on diode-connected transistors) of early versions. Although several analytical models have been reported to characterise charge-pump-based DDCs, a generic model that can capture important behaviors, such as power-efficiency and output variations, of all different topologies especially multi-stage multi-output (MSMO) structures is still lacking. This work studies the static behavior of charge-pump-based MSMO DDCs. Based on the presented model, a tapered MSMO DDC is proposed to improve the power efficiency and lower the voltage drop caused by multi-stage output loading. Finally, a design example is shown and simulated using a standard high-voltage 180-nm CMOS technology to verify the model and the effectiveness of the tapered design approach.

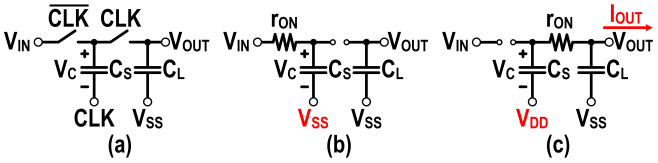

Fig. 1. Basic model of a charge-pump-based DDC. a) The circuit model, b) charging phase ($CLK = V_{SS}$), and c) pumping phase ($CLK = V_{DD}$)

II. Proposed Analytical Model

A. Multi-Stage Single-Output (MSSO) DC-DC Converter

To design a DDC for a specific application, several features including the output voltage under loading and the power efficiency (η) must be considered. Fig. 1(a) displays a basic model of a charge-pump-based DDC. When the circuit is in the charging mode (Fig. 1(b)), the storage capacitor C_S starts charging through the switch equivalent resistance r_{ON}, and creates a time constant for the charging phase. In the pumping mode (Fig. 1(c)), the capacitor is connected to the output node V_{OUT}, providing output current I_{OUT}. The output voltage of the circuit in the steady-state can be calculated, as follows:

$$V_{OUT} = V_{DD} + V_C - V_{DR,C} - V_{DR,R} \tag{1}$$

where V_{DD} is the supply voltage and $V_C = (1-\alpha)V_{IN}$ (where $\alpha = \exp(-1/(2f_{CLK}r_{ON}C_S)$ and $V_{IN} = V_{DD}$) is the voltage across the capacitor at the end of the charging phase. Furthermore, $V_{DR,C} = I_{OUT}/(2f_{CLK}C_S)$ and $V_{DR,R} = r_{ON}I_{OUT}$ hold (where f_{CLK} is the clock frequency of the charge pump circuit). The circuit η in the steady-state is derived, i.e.,

$$\begin{aligned}\eta &= \frac{P_{OUT}}{P_D + P_T + P_{Supply}} \\ &= \frac{V_{OUT}I_{OUT}}{C_{P,eq}f_{CLK}V_{DD}^2 + 2r_{ON}I_{OUT}^2 + 2V_{DD}I_{OUT}}\end{aligned} \tag{2}$$

where $C_{P,eq}$ is the equivalent parasitic capacitance of switches. P_D and P_T indicate dynamic and thermal power consumption, respectively, and P_{Supply} is the power provided by the supply.

Fig. 2 shows a generic multi-stage single-output (MSSO) DDC, where each block denotes a charge pump circuit. For a

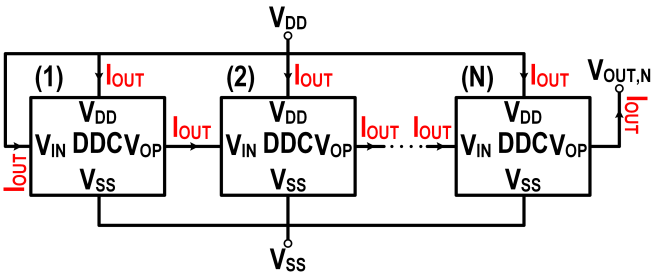

Fig. 2. Block diagram of an MSSO DDC (clock routing is not shown).

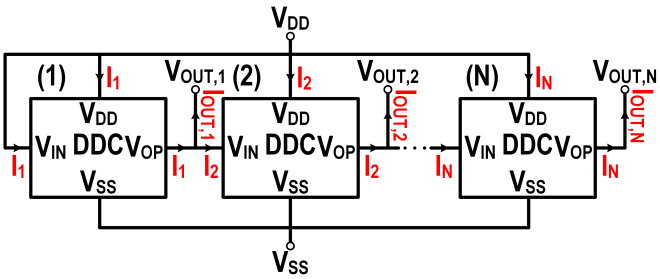

Fig. 3. Block diagram of an MSMO DDC (clock routing is not shown).

given output current I_{OUT} coming out of the N^{th} stage, an N-stage DDC sinks $(N+1)\times I_{OUT}$ from the supply voltage and produces an output voltage which is $(N+1)\times V_{DD}$.

Clearly, if the output voltage drop and the thermal and dynamic power dissipation of the circuit are all zero, the DDC achieves 100% efficiency. However, because of several nonidealities such as incomplete charging of storage capacitors due to inappropriate timing, non-zero insertion loss of metal-oxide-semiconductor (MOS) switches, and non-zero voltage drop of storage capacitors during the pumping phase, the output voltage in the steady-state will always be smaller than the ideal value, resulting in degradation of η. Based on (1) and (2), a generic model for output voltage and η of an MSSO DDC is developed.

For an MSSO DDC, since the load current evenly flows through all charge-pump stages, the overall voltage drop, $V_{DR} = V_{DR,R} + V_{DR,C}$, remains the same for all stages. Assuming that all storage capacitors in the circuit acquire their steady-state charge during the charging phase, α^2 will be very small. The output voltage for the n^{th} stage of an N-stage MSSO DDC $V_{OUT,n}$ is thus derived, as follows:

$$\begin{aligned} &V_{OUT,n} = V_{DD} + (1-\alpha)V_{OUT,n-1} - V_{DR} \approx \\ &(n+1)\Big(1-\frac{\alpha n}{2}\Big)V_{DD} - n\Big(1-\frac{\alpha(n-1)}{2}\Big)V_{DR} \end{aligned} \tag{3}$$

It should be noted that $V_{OUT,0}$ is equal to V_{DD}. The closed-form expression in (3) is utilized to analyze various charge-pump-based DDC architectures. Based on (3), the selection of a proper clock frequency ensures complete charging of the storage capacitors, which, in turn, leads to reduction of α. In this case, the only parameter contributing to the output voltage drop is V_{DR}. To reduce V_{DR}, one can increase the size of storage capacitors, while considering the area constraint.

As for the power efficiency of charge-pump-based DDCs, it is adversely affected by the output voltage drop (i.e., a reduction in output power) as well as the thermal power dissipation (caused by the equivalent resistance of MOS switches) and the dynamic power consumption (caused by the equivalent parasitic capacitance of circuit's components). Considering all of these factors, the η of an MSSO DDC is derived, as follows:

$$\eta = \frac{V_{OUT,N} I_{OUT,N}}{N(P_D + P_T) + (N+1)V_{DD} I_{OUT,N}} \tag{4}$$

where $I_{OUT,N}$ is the output load current of an N-stage MSSO DDC. According to (4), in order to improve η, the dynamic and thermal power dissipation must be reduced. Simultaneously, the output voltage drop should be kept constant or lowered to ensure a high η. For moderately low output load currents (i.e., sub-mA), the resistive voltage drop, $V_{DR,R}$, is small due to low on-resistance of MOS switches. Therefore, the main contributor to the output voltage drop, V_{DR}, is the non-zero voltage drop of the storage capacitors, $V_{DR,C}$, during the pumping phase. Clearly, a larger storage capacitance or a higher clock frequency will reduce the capacitive voltage drop. Among these two options, increasing the storage capacitance seems to be a more viable choice, as boosting the frequency leads to a higher dynamic power dissipation, and thus, a lower η. This implies that a larger storage capacitance allows us to choose a lower clock frequency for a given value of capacitive voltage drop, which leads to a notable decrease in dynamic power consumption.

B. Multi-Stage Multi-Output (MSMO) DC-DC Converter

Fig. 3 illustrates an MSMO DDC, where all the stages are connected to N output loads. Evidently, the output current of each stage not only passes through that particular stage but also flows through all preceding stages. As a result, the output voltage drop of the first few stages is larger than that of the last stages. The current provided by the n^{th} stage in an N-stage MSMO DDC is expressed as

$$I_n = \sum_{m=n}^{N} I_{OUT,m} \tag{5}$$

Moreover, the output voltage for the n^{th} stage of an MSMO DDC is calculated and is indicated in (6).

$$\begin{aligned} V_{OUT,n} \approx\ & (n+1)V_{DD} \\ & - \alpha\Big[\frac{n(n+1)}{2}V_{DD} - \sum_{m=0}^{n-1}(n-m)V_{DR,m}\Big] \\ & - \sum_{m=1}^{n} V_{DR,m} \end{aligned} \tag{6}$$

where $V_{DR,n}$ is the output voltage drop associated with the n^{th} stage. It is worth mentioning that $V_{DR,0}$ in (6) is equal to zero. Similarly, the overall η of an MSMO DDC is calculated, as follows:

$$\eta = \frac{\sum_{n=1}^{N} V_{OUT,n} I_{OUT,n}}{N P_D + \sum_{n=1}^{N} P_{T,n} + V_{DD}\sum_{n=1}^{N}(n+1)I_{OUT,n}} \tag{7}$$

where $P_{T,n} \propto I_n^2$ is the thermal power dissipation of the n^{th} stage. As indicated in (7), all stages have the same dynamic

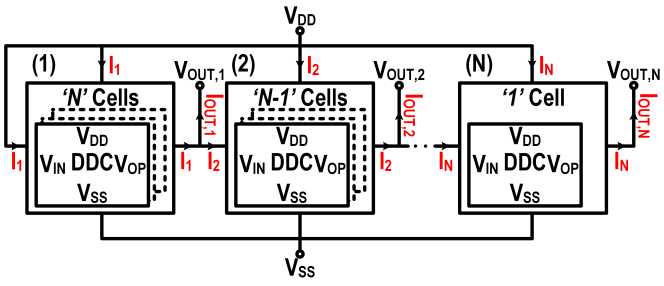

Fig. 4. Block diagram of a tapered MSMO DDC (clock routing is not shown).

power dissipation since the storage capacitors and the clock frequency of all of the charge-pump stages are identical. In a special case when $I_{OUT} = I_{OUT,1} = I_{OUT,2} = ... = I_{OUT,N}$, $V_{DR,n} = (N-n+1)V_{DR,N}$, where $V_{DR,N}$ is the voltage drop associated with the last stage. Under this condition, (6) and (7) for an MSMO DDC are simplified to (8) and (9), respectively.

$$V_{OUT,n} \approx (n+1)\left(1-\frac{n\alpha}{2}\right)V_{DD} - \left[\frac{n(2N-n+1)}{2} - \frac{n(1-n)(n-3N-2)\alpha}{6}\right]V_{DR,N} \quad (8)$$

$$\eta = \frac{6\sum_{n=1}^{N} V_{OUT,n} I_{OUT}}{6NP_D + N(N+1)(2N+1)P_T + 3N(N+3)V_{DD}I_{OUT}} \quad (9)$$

where $P_T = P_{T,N}$ is the thermal power loss of the last stage. Equation (8) shows that the output voltage decreases when all outputs of an MSMO DDC are loaded. As a consequence, η will be degraded. To mitigate this issue, the first stages with larger output currents are designed to incorporate multiple parallel charge pump cells. For the special case presented above where the output load current of all stages are equal, the proposed tapered structure demonstrated in Fig. 4 can be used. Since the output current of the first stage, I_1, is N times larger than that of the last stage, we use N parallel charge pump cells to reduce its voltage drop. The same trend applies to subsequent stages. This method makes the output voltage drop of an MSMO DDC similar to that of an MSSO DDC; therefore, the output voltage of a tapered MSMO DDC is also calculated using (3). The use of the tapered structure improves η by reducing the output voltage drop and lowering the thermal power consumption. It should be noted that the dynamic power dissipation of each tapered DDC stage will increase. However, the rate of increase in the dynamic power dissipation is less than the rate of drop in thermal power consumption. The power efficiency of the tapered structure of Fig. 4 is derived to be:

$$\eta = \frac{2\sum_{n=1}^{N} V_{OUT,n} I_{OUT}}{N(N+1)(P_D+P_T) + N(N+3)V_{DD}I_{OUT}} \quad (10)$$

III. Model Verification and Simulation Results

In order to verify the proposed analytical model, a new charge-pump-based DDC is designed and simulated for MSSO and MSMO configurations. Design methodology: Based on the available area and topology, the storage capacitance and clock frequency are chosen. Then, considering the required output voltage and load current, the most optimum number of stages for a given value of the supply voltage can be found using the proposed model. The schematic of the designed charge pump cell is depicted in Fig. 5(a). In this circuit, M_3 and M_4 provide a charging path for storage capacitors, C_{S1} and C_{S2}, respectively. In the pumping phase, M_5 and M_6 connect C_{S1} and C_{S2} to the output node, respectively. Moreover, C_L is used to reduce the ripple on the output voltage. In order to ensure that M_3 and M_5 or M_4 and M_6 do not turn on simultaneously, their gate terminals are isolated using two cross-coupled circuits realized by M_1-M_2 and M_7-M_8. In addition, C_{21} and C_{22} are chosen to be larger than C_{11} and C_{12}, respectively, to introduce a phase (time) difference between the voltages seen at the gates of M_3 and M_5 or M_4 and M_6. Since C_{11}, C_{12}, C_{21}, and C_{22} do not pump charge to the output node, they are designed to be much smaller than storage capacitors, and thus, are ignored in the steady-state model. Figs. 5(b) and (c) exhibit the equivalent circuits for charging and pumping cycles. In each cycle, active switches are replaced with their equivalent resistance, and inactive ones are opened. Assuming that the pair of M_3-M_4 and M_5-M_6 and the pair of C_{S1} and C_{S2} are sized equally, $r_{ON,C} = r_{ON,3} = r_{ON,4}$, $r_{ON,P} = r_{ON,5} = r_{ON,6}$, and $C_S = C_{S1} = C_{S2}$. Accordingly, the time-dependent output-voltage-drop coefficient becomes $\alpha = \exp(-1/(2f_{CLK}r_{ON,C}C_S))$ and the overall voltage drop is $V_{DR} = I_{OUT}(1/(2f_{CLK}C_S) + r_{ON,P})$.

To verify the proposed analytical model, the charge pump circuit, shown in Fig. 5(a), has been designed and simulated in a standard high-voltage 180-nm CMOS technology. The supply voltage for the designed circuit was set to $5\ V$, and thus, $5\ V$ thick-oxide transistors were used. In the design setup, following values were used: $C_L = C_{S1} = C_{S2} = 20\ pF$, $C_{11} = C_{12} = 100\ fF$, and $C_{21} = C_{22} = 900\ fF$. Also, based on the selected sizes for transistors and the process information, each charge pump cell exhibits an equivalent parasitic capacitance of $1.5\ pF$. Furthermore, the size of MOS switches were chosen such that $r_{ON,P} = 4r_{ON,C} = 400\ \Omega$. The simulation results for the output voltage and η versus the number of stages are shown in Fig. 6. For a given amount of output load current, increasing the number of cascaded stages results in an increase in difference between the actual output voltage and the ideal value, $(N+1)V_{DD}$, and hence, degradation of η. The simulated output voltage and η of a 3-stage MSSO DDC versus the storage capacitance are shown in Fig. 7. Based on these results, increasing the storage capacitance lowers the output voltage drop and ameliorates the power efficiency. Fig. 8 shows simulated output voltage and η versus the output load current. The dynamic power dissipation of the circuit depends on the clock frequency of the DDC, and thus, does not change based on the output load current. Therefore, for low output load currents, η remains low. On the other hand, for large output currents, the drop in the output voltage and the increase in the thermal power dissipation result in lowering the power efficiency. Fig. 9 compares the output voltage and η of a conventional and a tapered MSMO DDCs for different values of the output load current. Results indicate that the tapered structure exhibits a lower voltage drop and a higher η, particularly for large output currents. Indeed, for $1\ mA$ of output load current for each

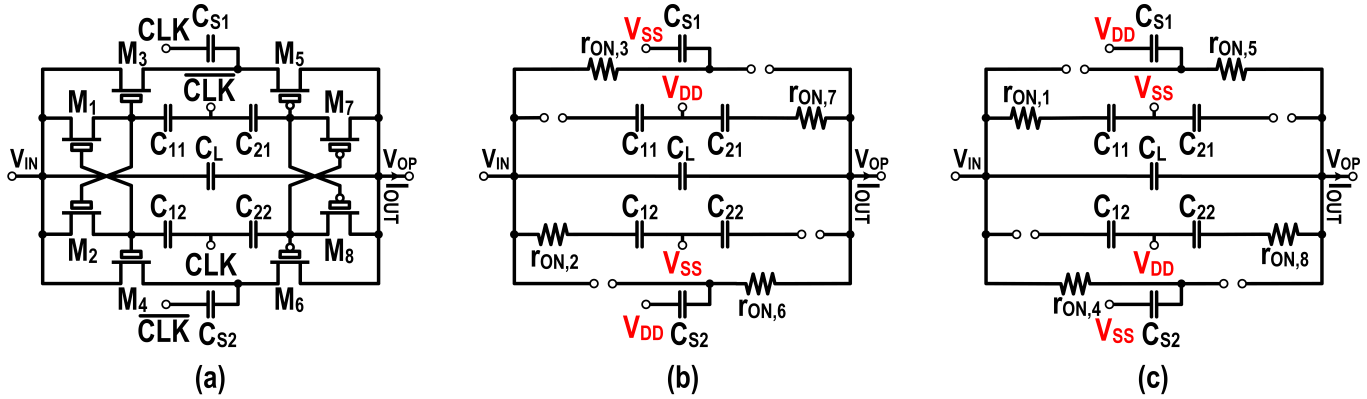

Fig. 5. a) Schematic of the charge-pump cell, b) and c) The equivalent circuit for charging-pumping cycles at $CLK = V_{SS}$ and $CLK = V_{DD}$ respectively.

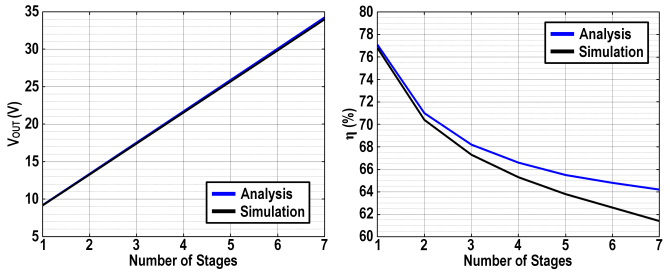

Fig. 6. V_{OUT} and η versus the number of stages for an MSSO DDC. ($CLK = 20MHz$, $C_S = 20pF$, $I_{OUT} = 500\mu A$)

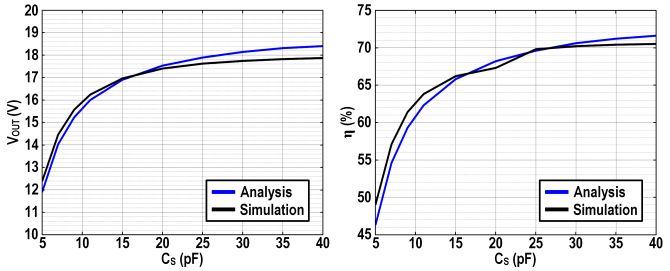

Fig. 7. V_{OUT} and η versus the storage capacitance for a 3-stage MSSO DDC. ($CLK = 20MHz$, $I_{OUT} = 500\mu A$)

stage, the output voltage drop of the simulated tapered 3-stage MSMO DDC for the last output, $V_{OUT,3}$, is 5 V less than that of a normal 3-stage MSMO DDC. Furthermore, for the same amount of output load current, the simulated tapered 3-stage MSMO DDC shows 23 % higher power efficiency compared to the normal architecture emphasizing the performance and superiority of the proposed tapered structure. The simulation results for each figure are also compared against the proposed model, verifying accuracy of the model. Due to the nonlinear behavior of MOS switches for large voltage swings, the value of parasitic capacitance and most importantly, the equivalent channel resistance vary resulting in a negligible error between the simulation results and the proposed model.

Conclusion

An analytical approach for modeling the output voltage and the power efficiency of various configurations, including MSSO and MSMO, of charge-pump-based DDCs was presented. To reduce the output voltage drop and improve the power efficiency of MSMO structures, the tapered design approach was introduced with great performance both in terms of the output voltage and the power efficacy compared to

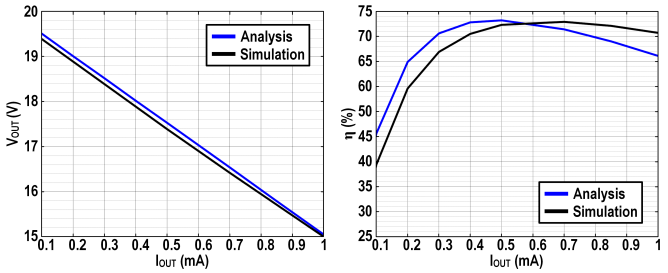

Fig. 8. V_{OUT} and η versus the output load current for a 3-stage MSSO DDC. ($CLK = 20MHz$, $C_S = 20pF$)

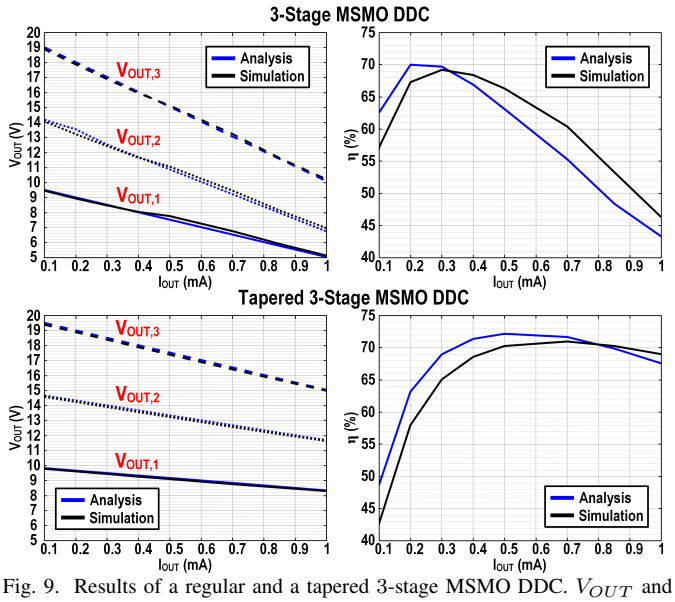

Fig. 9. Results of a regular and a tapered 3-stage MSMO DDC. V_{OUT} and η versus the output load current. ($CLK = 20MHz$, $C_S = 20pF$)

conventional topologies. Finally, the accuracy of the model was investigated using multiple simulations done on several architectures incorporating the newly introduced charge pump cell in a high-voltage 180-nm CMOS technology. Results verified accuracy of the analytical model.

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