A Novel Low Loss 3D System-in-Package Approach for 60GHz Antenna on Chip Applications

Stephen Adamshick
ECE Department
Western New England University
Springfield, USA
sa276908@wne.edu

Sandhiya Reddy Govindarajulu
ECE Department
Florida International University
Miami, USA
sredd015@fiu.edu

Elias A. Alwan
ECE Department
Florida International University
Miami, USA
ealwan@fiu.edu

***Abstract*—This paper presents a novel low loss 3D system in package (SiP) approach for achieving antenna-on-chip integration. Specifically, this design uses 3D through silicon via (TSV) technology to achieve a vertical SiP phased array radio. The fully integrated package consists of a digital baseband chip, a radio frequency integrated circuit (RFIC), and lastly a microstrip patch phased array. The 3D TSVs achieve an insertion loss of less than 0.4 dB/pair at millimeter-wave frequencies. The differential fed microstrip patch array achieves a return loss of 40 dB at a 60 GHz center frequency with 4 GHz instantaneous bandwidth. The antenna array achieves an E and H plane realized gain of 17.1 dBi for a 4×4 element design. In addition, this design approach enables individual fabrication of each element to maximize yield with low cost assembly using ball grid array (BGA) technology. Lastly, this design does not require special design rules that comprise either transistor or antenna performance as compared to other methods outlined in antenna on chip design.**

***Index Terms*—Antenna arrays, Electronics packaging, Microstrip patch antennas, Millimeter-wave communication, System integration**

I. Introduction

Trends continue to show that data processing, storage, and transmission rates are growing exponentially [1]–[3]. However, the demand to concurrently access this information is exceeding the current technologies available. The growth in data traffic and mobile connectivity has resulted in a highly congested microwave spectrum (<6GHz) with limited resources and deterioration in quality of service. To overcome spectrum congestion, an obvious approach is to make use of the available millimeter-wave (mm-wave) spectrum by exploiting the higher frequency bands from 20 to 80 GHz. Notably, mm-wave frequencies provide opportunities for wide bandwidth and enable data transmission rates of 50-100Gbps [4]. Particularly, mm-wave systems are attractive for short and long range terrestrial and satellite links as well as future autonomous and vehicle-to-vehicle communications. As such, millions of users can simultaneously communicate, even in presence of potential signal interference. Further, the small form factor of mm-wave radio frequency (RF) front-ends (antennas and electronics) implies inconspicuous integration on small mobile and vehicular platforms.

An obvious drawback of mm-wave communication is the large pathloss and attenuation due to obstructions and rain. Other challenges in designing mm-wave radios are mechanical fabrication inaccuracies due to their smaller footprint [5]–[8].The high pathloss in mm-wave communication can be overcome by employing antenna arrays with large gain and spatial beamforming. Notably, most commonly designed mm-wave antenna arrays employ either a dipole, a patch, a loop, or a monopole. Such elements are easy to design and their small size makes them excellent candidates for on-chip/vertical integration with RF front-end integrated circuits (ICs). However, creating large antenna arrays on an IC is a challenge due to the special design rules required for on-chip integration [9]–[11]. Namely, on-chip antennas require large ground planes to prevent radiation into the silicon (Si) substrates due to its high relative permittivity ϵ_r. The low resistivity of Si substrates ($10\ \Omega - \text{cm}$) suppresses electromagnetic (EM) radiation from antennas and concurrently degrade gain and radiation efficiency. To overcome the efficiency issue, large area Si is required, increasing the IC cost and making a system-on-chip (SoC) approach cost prohibitive. Therefore, designers have considered a system-in-package (SiP) approach that combines different IC components with the antenna arrays, both in the same integrated chip package. As compared to SoC implementations, SiP also allows for 2D integration of different ICs on the same chip. However, due the limited

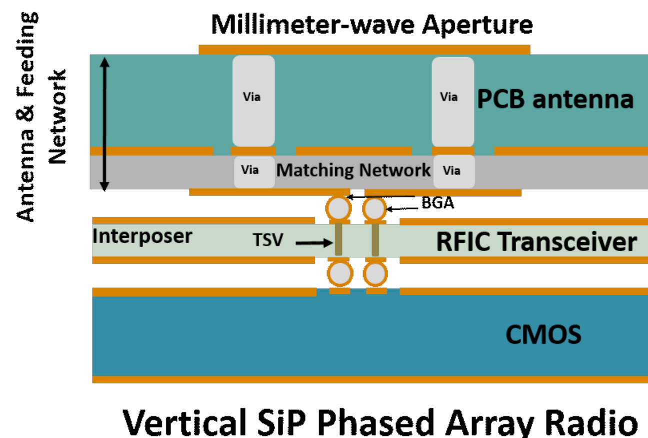

Fig. 1. Low loss 3D SiP phased array radio. Our novel “More than Moore (MtM)” packaging approach employs a 3D integration with TSV structures to interconnect the heterogeneously stacked ICs.

978-1-7281-8058-8/20/$31.00 ©2020 IEEE

Authorized licensed use limited to: FLORIDA INTERNATIONAL UNIVERSITY. Downloaded on September 22,2021 at 00:10:26 UTC from IEEE Xplore. Restrictions apply.

electrical connectivity of ICs, current SiP implementations still require long horizontal traces to interconnect the different IC components on a multi-chip module. These long interconnect transitions (e.g. bond wires) are lossy and result in pathloss between the individual components, namely the IC and antenna array.

In this letter, we present a novel low-profile 3D integration method to interconnect heterogeneously integrated stacked circuits in a SiP, as depicted in Fig 1. The SiP is a complete radio architecture that consists of a low cost, high gain antenna array with feeding network, operating at 60GHz. Notably, the array is implemented on printed circuit board (PCB). To reduce losses associated with bond wires in typical SiP, the array is vertically integrated to the RF transceiver chip using Through Silicon Via (TSV) structures to enable 3D vertically stacked ICs. As such, significant reduction in the overall package size is realized as compared to traditional 2D SiP implementations. In addition, our mm-wave array stack-up exhibits near theoretical gain at 60GHz using our 3D integration approach. The SiP packaging approach is described in Section II. In Section III, we present the design and simulation results of the mm-wave antenna array stack-up. Overall conclusions are presented in Section IV.

II. SIP PACKAGING APPROACH

Traditionally, electronic components are packaged in single chip carriers, which are then assembled onto a PCB that provides interconnects between the chips of different functionality. However, in the 30-70 GHz regime, the PCB interconnects sustain high frequency losses due to the physical distance between devices. To overcome this, 3D integration with TSVs is employed to maximize mm-wave performance while maintaining reduced costs as shown in Fig. 2 [12].

Our SiP packaging approach takes advantage of 3D TSV technology in the RFIC transceiver chip to interconnect the baseband CMOS to the RFIC and our novel antenna array, as shown in Fig. 1. In doing so, the tunable mm-wave transceiver can be implemented in 65-90nm CMOS at a significantly lower cost as compared to the scaled CMOS design in digital implementations. Notably, the additional processing steps required to fabricate the 3D interconnect occur in a lower cost technology. Further, the RFIC chip with the 3D interconnects will feature copper interconnects on both sides of the IC with BGA solder bumps as the I/O between each of the chips.

In our design, we utilize the plug based TSVs as these achieve a minimal insertion loss (see Fig. 3) and are configurable to the required impedance for optimum matching to the antenna array and transceiver components [12]. Furthermore, no balun is required as the TSVs can be excited in the differential mode consistent with the antenna array. Notably, the 5×50 m TSVs exhibit minimal loss at mm-wave frequencies despite a substrate resistivity of 10 Ω - cm, as depicted in Fig. 3. The measured data from this characterization was extrapolated to accommodate vias of 10×100 m. The larger dimensions will support better mechanical stability and increased yield while maintaining superior mm-wave performance as the next section will describe with the fully integrated antenna array.

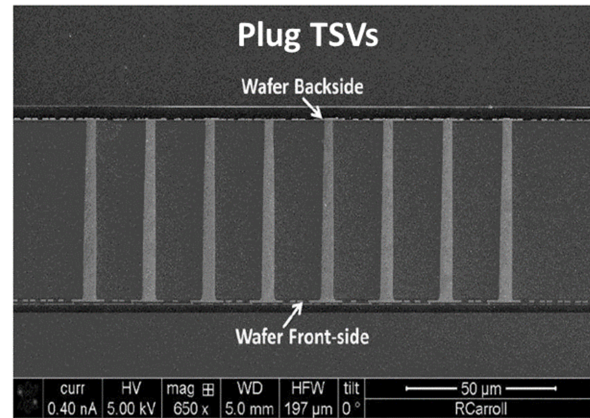

Fig. 2. Focused Ion Beam (FIB) prepared Scanning Electron Microscope (SEM) image of the 3D TSV interconnect structures illustrating metallization on both the front and backside of the IC package.

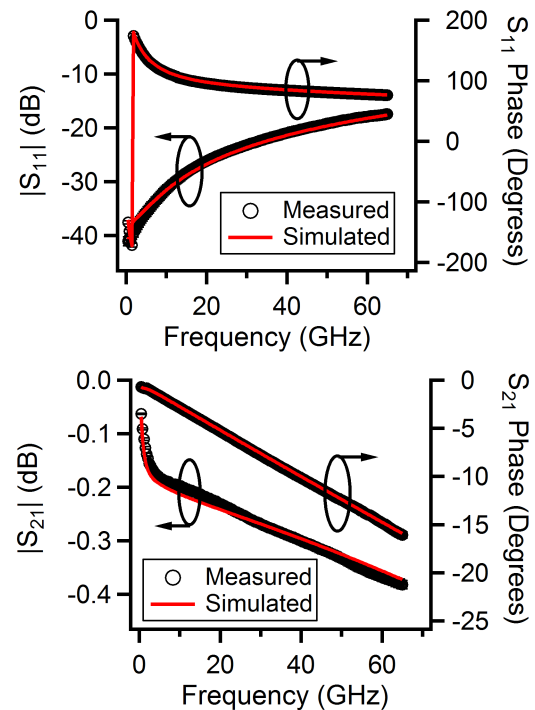

Fig. 3. The return and insertion loss of the differential TSV pair characterized to 65 GHz normalized to 50 Ω [12].

III. MILLIMETER-WAVE PHASED ARRAY

A. Array Stack-up Geometry

In this section, we present the design of a mm-wave finite array of patch elements, operating at 60GHz. The design of the mm-wave array is depicted in Fig. 4. The array consists of 4 × 4 patch elements designed on RT/Duroid 5880 (ϵ_r = 2.2) substrate with thickness 0.13 mm. The total unit cell

Authorized licensed use limited to: FLORIDA INTERNATIONAL UNIVERSITY. Downloaded on September 22,2021 at 00:10:26 UTC from IEEE Xplore. Restrictions apply.

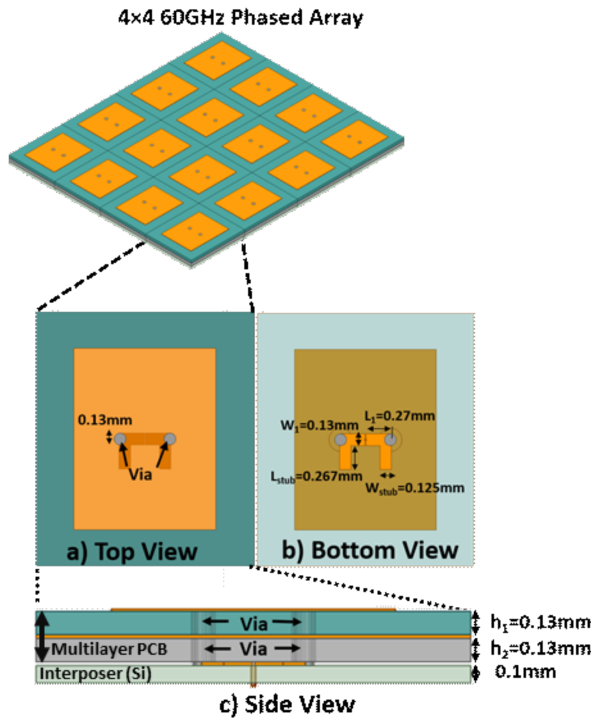

Fig. 4. 60GHz mm-wave phased array with 4×4 patch elements: a) Top view b) Bottom view c) Side view

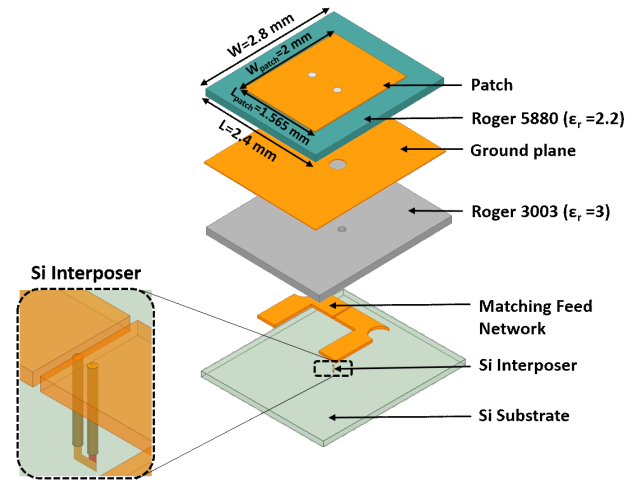

Fig. 5. 3D view of simulated stacked phased array

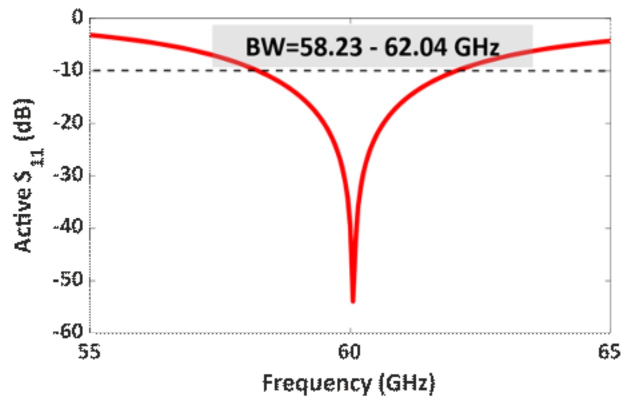

Fig. 6. S-parameter of the simulated phased array

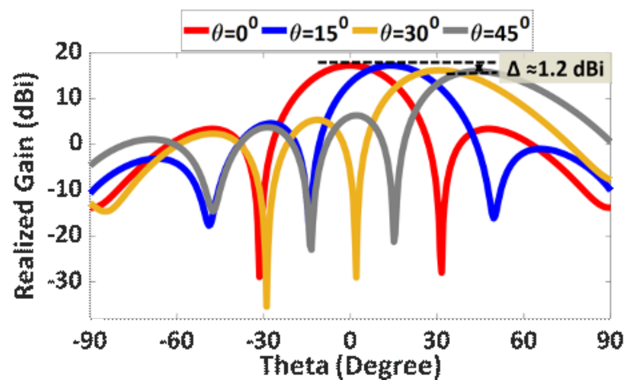

Fig. 7. Simulated E-plane scanning performance of a 4×4 patch array at 60GHz for angles: 0°,15°,30°,45°

dimensions are 2.4mm × 2.8 mm × 0.45 mm (L × W × h). The patches are fed differentially using two vias that connect the aperture to a matching network, feeding the interposer. The latter houses the TSV interconnects, as depicted in Fig. 1. The matching network consists of an open stub and is designed as a transition between the TSVs and the vias feeding the antenna aperture. Details of the different layers of the array stack-up are illustrated in Fig. 5. In this analysis, the BGAs were replaced by direct connections. As seen, the antenna and the matching network are each implemented on a different PCB. Specifically, the matching network is implemented on the lower Roger 3003 substrate (ϵ_r = 3) with thickness 0.13 mm. Notably, PCB implementation avoids the losses associated with Si substrate.

B. Simulated Results

A finite array simulation with 4×4 patch elements was conducted using ANSYS HFSS v.19. The array is optimized to operate at 60 GHz. Fig. 6 shows that the array achieves active S11¡-10dB from 58.23 to 62.04 GHz by exciting the center element. Further, at boresight, the array achieves a realized gain of 17.1 dBi at both E and H plane, as depicted in Fig. 7-8. This result is compared to a similar patch array's unit cell without the Silicon interposer. Clearly, the silicon interposer does not incur any significant losses, as illustrated in Fig. 9. Further, scanning performance for angles 0°,15°,30°,45° in both E and H planes is depicted in Fig. 7 and 8 , respectively. Results show that the array can scan down to 450 from boresight. As expected, the realized gain reduces by a $\cos(\theta)$ factor, where θ is the scan angle. The simulated array provides -40dB low cross-polarization in E plane and less than -60dB in H plane as shown in Fig. 10.

Authorized licensed use limited to: FLORIDA INTERNATIONAL UNIVERSITY. Downloaded on September 22,2021 at 00:10:26 UTC from IEEE Xplore. Restrictions apply.

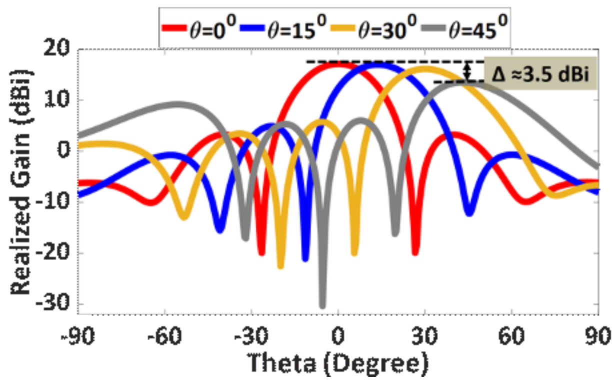

Fig. 8. Simulated H-plane scanning performance of a 4×4 patch array at 60GHz for angles: 0°,15°,30°,45°

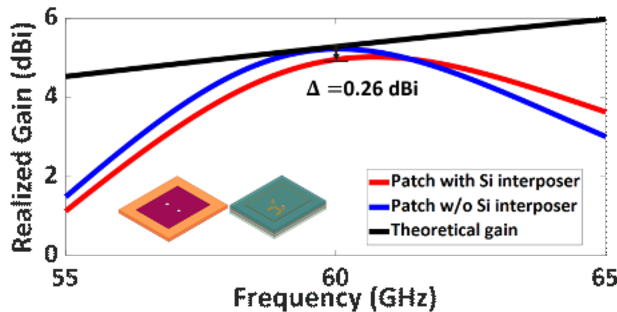

Fig. 9. Realized gain of a patch array's unit cell with and without Si interposer.

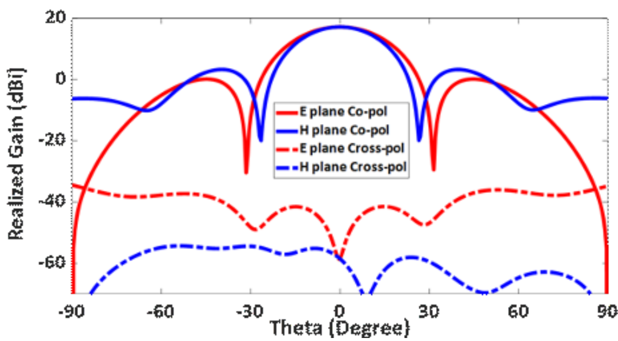

Fig. 10. Simulated radiation pattern at 60GHz

IV. Conclusions

This paper presented a fully integrated 3D SiP solution that utilizes 3D TSV technology to minimize millimeter wave losses. The 3D SiP approach enables the design of a high gain antenna array network that would not be traditionally feasible with other SoC or SiP architectures. The TSVs are integrated within the RFIC chip to minimize costs while not sacrificing performance. The antenna array consists of a differential fed 4x4 microstrip patch with an open stub matching feed network. The 4x4 microstrip patch array achieves a 4 GHz bandwidth centered about 60 GHz with a realized antenna gain of 17.1 dBi with the silicon interposer IC only accounting for a 0.26 dBi of loss. Further, all components of this design strategy can be fabricated independently and combined using traditional BGA packaging technology. Lastly, this approach requires no special design rules for the transistor devices or antenna structures, thus making it an ideal candidate for antenna on chip integration.

References

[1] G. Fettweis and E. Zimmermann, "Ict energy consumption-trends and challenges," in *Proceedings of the 11th international symposium on wireless personal multimedia communications*, vol. 2, no. 4. Citeseer, 2008, p. 6.

[2] R. A. Gupta and M.-Y. Chow, "Networked control system: Overview and research trends," *IEEE transactions on industrial electronics*, vol. 57, no. 7, pp. 2527–2535, 2009.

[3] J. Chapin and W. Lehr, "Mobile broadband growth, spectrum scarcity, and sustainable competition." TPRC, 2011.

[4] Z. Pi and F. Khan, "An introduction to millimeter-wave mobile broadband systems," *IEEE communications magazine*, vol. 49, no. 6, pp. 101–107, 2011.

[5] H. M. Cheema and A. Shamim, "The last barrier: on-chip antennas," *IEEE Microwave Magazine*, vol. 14, no. 1, pp. 79–91, 2013.

[6] M. Marcus and B. Pattan, "Millimeter wave propagation: spectrum management implications," *IEEE Microwave Magazine*, vol. 6, no. 2, pp. 54–62, 2005.

[7] S. R. Govindarajulu, S. B. Venkatakrishnan, and E. A. Alwan, "Millimeter-wave wideband array for vehicle to vehicle communication," in *2018 IEEE International Symposium on Antennas and Propagation & USNC/URSI National Radio Science Meeting*. IEEE, 2018, pp. 1203–1204.

[8] B. J. DeLong, S. R. Govindarajulu, M. H. Novak, E. A. Alwan, and J. L. Volakis, "A 60ághz phased array with measurement and de-embedding techniques," *Analog Integrated Circuits and Signal Processing*, vol. 97, no. 3, pp. 557–563, 2018.

[9] Y. P. Zhang and D. Liu, "Antenna-on-chip and antenna-in-package solutions to highly integrated millimeter-wave devices for wireless communications," *IEEE Transactions on Antennas and Propagation*, vol. 57, no. 10, pp. 2830–2841, 2009.

[10] M. Sun, Y. P. Zhang, Y. Guo, K. Chua, and L. Wai, "Integration of grid array antenna in chip package for highly integrated 60-ghz radios," *IEEE Antennas and Wireless Propagation Letters*, vol. 8, pp. 1364–1366, 2009.

[11] F. Gutierrez, S. Agarwal, K. Parrish, and T. S. Rappaport, "On-chip integrated antenna structures in cmos for 60 ghz wpan systems," *IEEE Journal on Selected Areas in Communications*, vol. 27, no. 8, pp. 1367–1378, 2009.

[12] S. Adamshick, R. Carroll, M. Rao, D. La Tuplie, S. Kruger, J. Burke, and M. Liehr, "High frequency electrical characterization of 3d signal/ground through silicon vias," *Progress In Electromagnetics Research*, vol. 47, pp. 71–75, 2014.

Authorized licensed use limited to: FLORIDA INTERNATIONAL UNIVERSITY. Downloaded on September 22,2021 at 00:10:26 UTC from IEEE Xplore. Restrictions apply.