

Comprehensive Low Power Adiabatic Circuit Design with Resonant Power Clocking

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Abstract—In this paper, the first comprehensive methodology is presented for design of low power adiabatic circuits inclusive of the adiabatic core design and the power-clock generation. Prior works have focused on either designing adiabatic cores or the power clock generation circuit, only. These non-comprehensive views can misrepresent the performance savings and fail to address the opportunities at integration. In this work, a comprehensive solution is presented that also features a unique innovation for the power clock generation circuit in step-charged circuits designed with rotary traveling wave oscillators (RTWO) and adiabatic frequency dividers. In experimentation, SPICE based simulations are performed at 416 MHz and 330 MHz in the 90 nm technology node and compared to CMOS based implementations, as well as other known power-clock generation techniques. A 32-bit CMOS adder consumes $3.5\times$ more power when compared to the proposed 32-bit ECRL adder operating at a frequency of 416 MHz. Furthermore, 1000 32-bit CMOS adders in parallel consumes $3.4\times$ more power when compared to 1000 32-bit ECRL adders in parallel designed with the proposed architecture at a frequency of 416 MHz.

I. INTRODUCTION

Adiabatic logic achieves low power consumption by recycling the energy dissipated back to the power source [1]. In adiabatic logic, the transition from one voltage level to another is not abrupt like standard CMOS logic. A voltage ramp (power-clock) is utilized to charge and recover the energy from the output. A sinusoidal signal, called the power-clock, is used as the voltage ramp which serves both as an energy and timing source to adiabatic gates. The power-clock enables charge to flow back and forth from the load, recycling part of the energy back to the power-clock resulting in low power consumption. Depending on the adiabatic logic family, there can be two or more power-clock signals, referred to as phases of the power-clock.

Prior works have only provided partial solutions for an adiabatic system i.e., focus has primarily been on either generating the power clock or an energy efficiency adiabatic logic family [2–6]. Furthermore, these solutions lack detailed analysis of the overhead by either side on the order (e.g. incurred by the control logic for the power-clock generation circuits). This work proposes a comprehensive methodology that includes the novelty of utilizing a resonant clock solution in the power clock generation circuitry. The proposed novel power-clock circuit is designed to provide the desired number of phases and load driving capability of the adiabatic logic

core. In particular, rotary traveling wave oscillators (RTWO) are utilized to generate the control signals for the step-charged circuit. RTWOs are a low-power, high frequency, multiphase, and constant magnitude resonant clock source [7]. RTWOs are robust in terms of frequency and phase while providing constant magnitude [8, 9]. High frequency RTWOs are designed which is then frequency divided to generate the required control signal for the step-charged circuit. The frequency divider is an adiabatic circuit that is operated with the multiphase clock signals of the RTWO [10]. The proposed methodology utilizes this proposed implementation of the power-clock signal, designed at the desired number of phases, frequency, and load profile, to implement the adiabatic logic circuit component. For demonstration and experimentation, the proposed architecture is first implemented on a 32-bit efficient charge recovery logic (ECRL) adder [11], and scaled to 1000 adders in parallel with equivalent load to account for routing. In SPICE based simulations, the power consumption of the ECRL adder is reported, and compared to a FSM based power-clock generation technique [12] for the ECRL adder and a standard CMOS adder.

This rest of this paper is organized into the following sections. Technical background is discussed in Section II. The proposed architecture is presented in Section III. Experimental analysis and the results are discussed in Section IV. Conclusions are provided in Section V.

II. TECHNICAL BACKGROUND

A. Power-Clock and Two-Step Charged Circuit

The power-clock serves as the timing source that synchronizes the adiabatic logic, requiring a reliable and robust power-clock. The power-clock eliminates the need for registers in adiabatic logic, as it has inherent pipelining [1]. Multiphase power-clocks are required to synchronize the multiple stages in adiabatic logic. The power-clocks for adiabatic logic need to satisfy two conditions to achieve high energy efficiency 1) rail-to-rail voltage swing and 2) trapezoidal or sine like power-clock source. Prior works for adiabatic logic have employed passive components to generate the power-clock that incur significant area overhead and challenges in terms of integration and feasibility [2–6]. A finite state machine (FSM) implementation is presented in [12] to control the switches in step-charged circuits to generate the power-clock. Step-charging for driving a capacitive load was first proposed in [13]. A two-step charged circuit designed with tank capacitors is illustrated

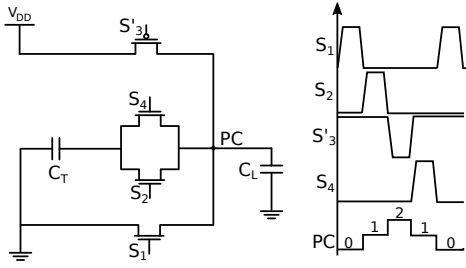


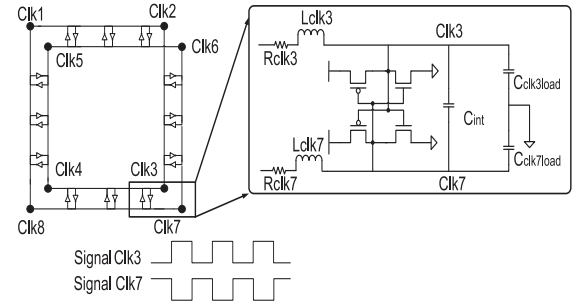
Fig. 1. Two-step charged power clock source.

in Fig. 1. The switches in step-charged circuits are turned On in periodic fashion to generate a step-like signal at the node PC . The control signals for the step-charged circuits require energy efficient and robust control signals to minimize the over all power consumption.

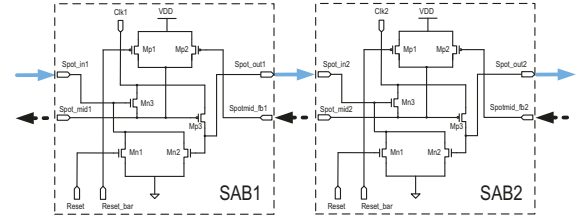
In step-charging circuits, the capacitance at the output node is charged from the power source and the tank capacitors to generate a step-charged signal. The step-charged circuit was first introduced in [13]. A two-step charged circuit designed with tank capacitors and switches along with the operational waveform is illustrated in Fig. 1. Charging the load capacitor (C_L) in steps results in energy reduction when compared to a single step [13]. The total energy dissipated by the step-charged circuit is estimated as: $E_{diss} = (V_{DD}^2 C_L)/N$, where N is the number of steps [13]. The switches in a two-step charged circuit are turned On/Off in periodic fashion to generate the desired voltage level at the node PC , illustrated in Fig. 1. The size of the control switches and the frequency at which it is operated contribute to the overall energy dissipation of the circuit. As the number of steps increase, the energy dissipation increases. Prior works have focused on either determining the optimal number of steps, switch size, load capacitance to tank capacitance ratio, or techniques to generate the control signals [12, 14]. Designing an energy efficient control circuit for the step-charged circuit is largely unexplored.

B. Rotary Traveling Wave Oscillators

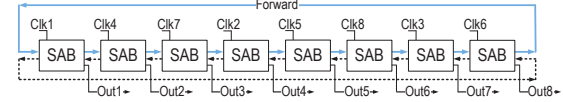
A rotary traveling wave oscillator is a low-power, resonating signal along the mobius shape, where frequency depends on the geometric shape of the distribution network and the clock load, due to resonance [7]. Rotary traveling wave oscillators (RTWOs) are modeled as an LC oscillator [7]. The frequency of oscillations of the RTWO is expressed as: $f_{osc} = 1/2\sqrt{L_T C_T}$. The total inductance L_T depends on the geometry of the rotary ring and C_T is the total capacitance of the ring, interconnects and devices connected to the rotary ring. The traveling wave along the mobius shaped transmission line of the RTWO provides multiple phases inherently [7]. The phase delay of the RTWO is evenly distributed in the direction of wave propagation. The relationship between the time delay, t and phase delay, θ is expressed as, $\theta/2\pi = t/T$; where T is the clock period. The clock signal travels along the rotary ring and reaches back the reference point with the phase of $\theta = 2\pi$. RTWOs do not require bulky inductors and



(a) Rotary traveling wave oscillator (RTWO).



(b) Spot advancing block (SAB) [10].



(c) Resonant frequency divider [10].

Fig. 2. Resonant clock source and frequency divider topology.

capacitors, and eliminate the need for high-quality inductors or custom inductor libraries to implement resonant clocking. In [15], an ASIC compliant solution to design RTWOs with clock dividers at frequencies below 1 GHz is presented.

1) *Resonant Frequency Division*: Resonant frequency division for RTWOs was proposed in [10]. The dividers makes use of the multiple phases of a rotary clock that act as the power-clock for the spot-advancing blocks (SABs). The circuit for the SABs is shown in Fig. 2(b). The SABs are connected in the form of a loop with each SAB having a phase of the clock signal associated with it as shown in Fig. 2(c). The phase of each clock signal determines when the output of a SAB is passed on to the next SAB. The principle of frequency division depends on the phase difference between the adjacent SABs incurred by the clock. The SABs provide the multiphase adiabatic signals to control the switches of the step-charged circuits.

In Fig. 2(c), the number of clock signals is set to 8, with a phase delay of $1/8 * 2\pi$ between adjacent clock signals. The *Spot_in* signal propagates the signal to the next stage and the *Spotmid_fb* cleans up the spot signal of the current SAB. The SAB frequency divider shown in Fig. 2(c) performs a frequency division ratio of 3. The phase delay and the number of SAB connections determines the division ratio. The multiphase clock signals are assigned with respect to the rotary clock ring shown in Fig. 2(a). Depending on the frequency division ratio, the number of SABs vary but are determined and known at design time.

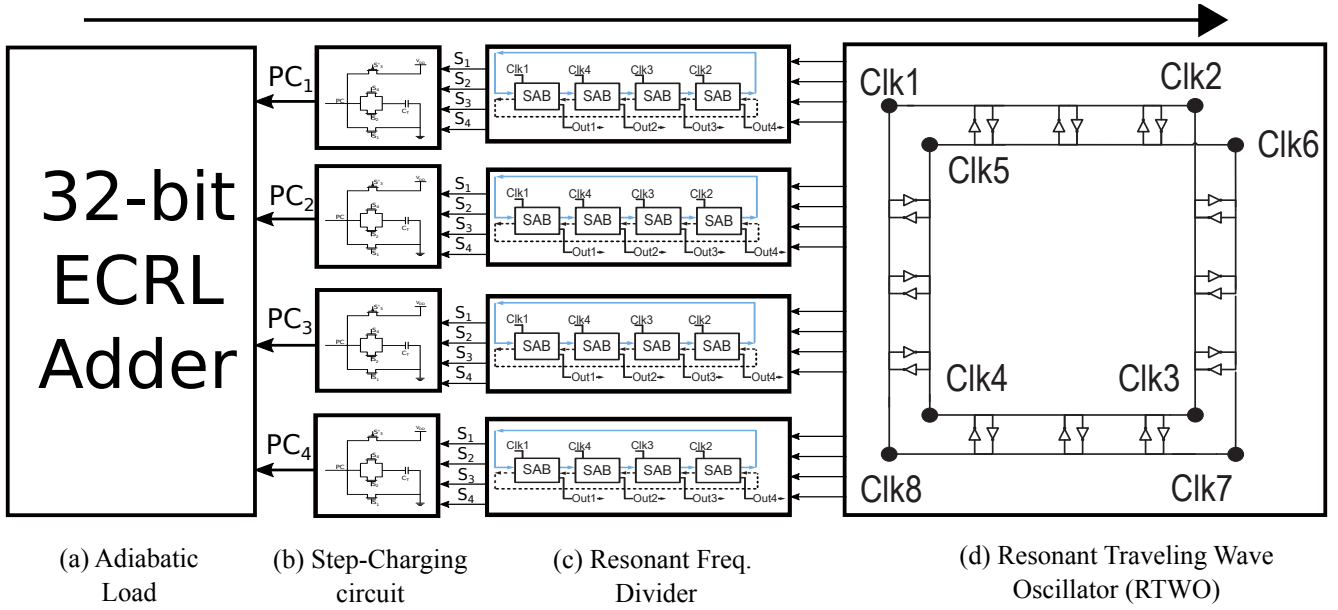


Fig. 3. Proposed multiphase clock generation and delivery architecture for adiabatic logic.

III. PROPOSED ARCHITECTURE

In current art, multiphase power-clock signals need to be designed with one dedicated step-charged circuits for each power-clock phase. The required phase difference between each power-clock is 90° . The proposed multiphase power-clock generation architecture eliminates the need for such dedicated circuits, illustrated in Fig. 3. In order to illustrate the general concept on a specific case, four power-clocks are generated that are 90° out of phase with each other to drive a 32-bit ECRL adder. The ECRL logic family requires a four phase power-clock. For simplicity, in this work a two-step charged circuit is designed to generate four different phases of the power-clock. The following sections discuss the methodology and circuit design for this work.

A. Methodology

A top down approach is used to design the power-clock architecture in this work. First, an adiabatic core is designed and the total capacitance of the core (C_{Total}) is estimated (Fig. 3(a)). Second, the number of power-clock phases required and capacitance driven by each phase is determined. Third, a two-step charged circuit is designed with tank capacitors maintaining the C_L/C_T ratio at 10:1 [12] (Fig. 3(b)). Fourth, based on the number of switches required for the step-charged circuit the resonant frequency divider topology is designed (Fig. 3(c)). Finally, the rotary traveling wave oscillator is designed with the frequency divider topology information and target frequency (Fig. 3(d)).

B. Circuit Design

A 32-bit ECRL adder is considered for this work, illustrated in Fig. 3(a). The ECRL adder requires four power-clocks with each power-clock 90° out of phase. The proposed power-clock design consists of a rotary traveling wave oscillator (RTWO),

resonant frequency divider, and two-step charged circuit. The two-step charged circuit is designed as illustrated in Fig. 3(b) (detailed in Fig. 1). MOS type capacitors are used for the tank capacitors along with three NMOS switches and one PMOS switch. At steady state when the switch S_1 is closed, the voltage at the node PC is discharged to 0. The switch S_2 is then closed, during which the charge stored across the tank capacitor is transferred to the node PC , at this point the voltage is approximately at $V_{DD}/2$. Next, the switch S_3 is closed, the voltage at the node PC is at full-swing V_{DD} . Finally, the switch S_4 is closed, the voltage at the node PC goes back to $V_{DD}/2$.

The two-step charged circuit requires four control signals, illustrated in Fig. 1. In order to generate the control signals, a divide by three resonant frequency divider is designed, illustrated in Fig. 3(b). The divider topology requires four clocks with a constant phase delay of $1/4 \times \pi$ between them. The adjacent phase delays between the clocks are set to be $3/4 \times 2\pi$, resulting in a phase delay of $3/4 \times 2\pi$ between each SAB. As the clock signal loops through the frequency divider, the total phase delay is $4 \times 3/4 \times 2\pi$, generating a divide by three signal. The OUT signal of each SAB block has a phase delay of $3/4 \times 2\pi$, that is utilized to control each switch of the step-charged circuit. In Fig. 4, the output signal from each SAB is illustrated along with the associated clock phases and frequency division phase. Note that the SAB circuit illustrated in Fig. 2(b), generates the inverted signal of OUT at the node $Spot_out$, which is used to control the switch S_3 for the PMOS. This eliminate the need for an inverter.

To generate the 90° phase delay between the power clocks, the routing order between $OUT1$ to $OUT4$ to the step-charged circuit is modified. To generate PC_1 the switch connections from the divider to the two-step charged circuit are as follows: $OUT1 \rightarrow S_1$, $OUT2 \rightarrow S_2$, $OUT3'(Spot_out) \rightarrow S_3$,

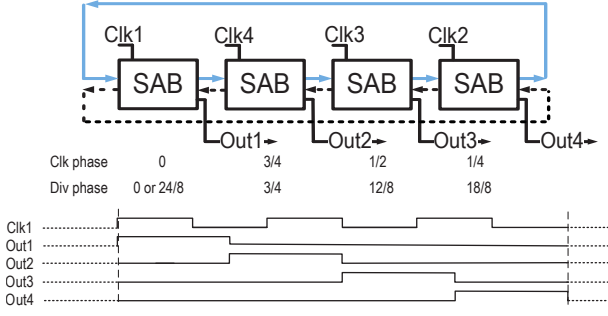


Fig. 4. Output of divide_by3 resonant frequency divider.

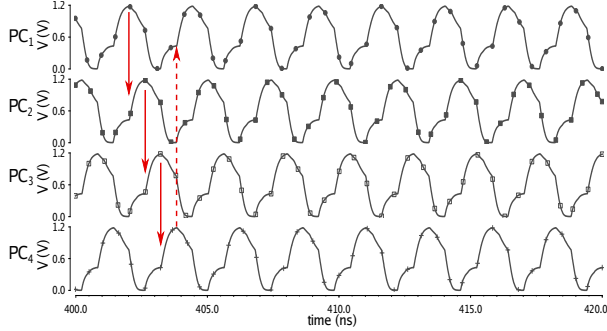


Fig. 5. Four-phase step charged power clock, frequency = 416 MHz.

and $OUT4 \rightarrow S_4$. In similar fashion, to generate PC_2 the switch connections are: $OUT4 \rightarrow S_1$, $OUT1 \rightarrow S_2$, $OUT2'(Spot_out) \rightarrow S_3'$, and $OUT3 \rightarrow S_4$. In similar fashion PC_3 and PC_4 are designed. The four phase power-clocks plotted in Fig. 5 is designed with a 1.25 GHz RTWO. The RTWO is then frequency divided by 3 to generate the control signals for the step-charged circuit to generate the power-clock operating at a frequency of 416 MHz.

IV. EXPERIMENTAL ANALYSIS

A 90 nm CMOS technology node along with HFSS models for the RTWOs [15] are employed to implement the proposed architecture. The proposed architecture is evaluated with SPICE simulations at two different frequencies, 416 MHz and 330 MHz chosen arbitrarily. The overall power consumption reported includes the control circuit, clock source, and adiabatic load. In Table I, the overall power consumption at the two operating frequencies is presented. The power consumption for the designs in Table I is calculated over 100 clock cycles at each frequency. The proposed architecture is compared to an FSM based technique for the power-clock generation [12] and to a standard cell based 32-bit CMOS adder. A voltage controlled ring oscillator [16] is designed to generate the clock for the FSM and CMOS based designs. Additionally, 1000 parallel adders are designed along with load capacitors accounting for routing to evaluate the proposed power-clock architecture for large designs.

The 32-bit CMOS adder consumes $3.5\times$ more power when compared to the proposed 32-bit ECRL design operating at a frequency of 416 MHz. The savings in power are attributed to the ECRL based design along with the power-clock generation

TABLE I
32-BIT ECRL ADDER POWER CONSUMPTION. $V_{DD} = 1.2$ V.

Design Name	Frequency = 416 MHz Power Cons.(%Eff)	Norm. to This Work	Frequency = 330 MHz Power Cons.(%Eff)	Norm. to This Work
32-bit ECRL adder This work	1.10 mW (41%)	1 $\times$	1.18 mW (38%)	1 $\times$
32-bit ECRL adder with PC from [12]	1.59 mW (12%)	1.5 $\times$	1.51 mW (12%)	1.3 $\times$
32-bit CMOS adder with clock	3.83 mW	3.5 $\times$	3.09 mW	2.6 $\times$
1000 parallel 32-bit ECRL adders This work	158.30 mW (47%)	1 $\times$	139.40 mW (48%)	1 $\times$
1000 parallel 32-bit ECRL adders with PC from [12]	283.50 mW (8%)	1.8 $\times$	241.30 mW (9%)	1.7 $\times$
1000 parallel 32-bit CMOS adders with clock	538.10 mW	3.4 $\times$	464.30 mW	3.3 $\times$

technique. The RTWOs along with the frequency divider utilized are adiabatic circuits that provide substantial savings in power. The switches in the step-charged circuits are controlled by the resonant signals from the adiabatic frequency divider. The savings in power are observed at an operating frequency of 330 MHz as well. The 32-bit CMOS adder consumes $2.6\times$ more power when compared to the 32-bit ECRL designed with the proposed architecture.

To further investigate the savings provided by the proposed architecture, the FSM based technique is implemented [12]. The 32-bit ECRL adder designed with the power-clock from [12] consumes $1.5\times$ more power when compared to the 32-bit ECRL adder designed with the proposed architecture at a frequency of 416 MHz. The two techniques are designed with the same two-step charged circuit topology driving the same 32-bit ECRL adder. It is observed from Table I that the proposed architecture provides significant savings in power due to the control signals designed in this work. The conversion efficiency is reported in Table I. The proposed architecture has an average conversion efficiency of 40% across the two frequencies. The proposed architecture provides a resonant solution to achieve significant savings in power while driving the switches in the step-charged circuit. In Table I, power consumptions results are presented for 1000 parallel adders along with load capacitors accounting for routing. The ECRL adders designed with the power-clock from [12] consumes $1.8\times$ more power when compared to the proposed power-clock architecture at a frequency of 416 MHz. The proposed power-clock architecture has an average conversion efficiency of 48% across the two frequencies. The proposed architecture provides significant savings with large designs thanks to the RTWOs and frequency dividers.

V. CONCLUSIONS

Low power adiabatic circuits with a novel power-clock design methodology is presented in this paper. A two-step charged circuit topology with rotary traveling wave oscillator architecture is proposed to provide an energy efficient solution for the power-clock design. A 32-bit CMOS adder consumes $3.5\times$ more power when compared to the proposed 32-bit ECRL adder operating at a frequency of 416 MHz. Furthermore, the proposed architecture on comparison to FSM based power-clock design technique consumes $0.7\times$ less power.

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