Voltage Balancing Control with Capacitor Charging Method for Series Connected SiC MOSFET Submodules

Inhwan Lee, Xiu Yao
Electrical Engineering
State University of New York at Buffalo
Buffalo, USA
Email: inhwanle@buffalo.edu

***Abstract*—Device series connection is a method to achieve higher blocking voltage with multiple devices. However, a voltage unbalance among the series connected devices is a critical issue that may lead to a failure of the devices. The unbalance can be caused by difference of device characteristics and mismatch of gate signals due to delay of external gate drive circuit. In this work, a voltage balancing control (VBC) for series connected SiC MOSFET submodules is studied to solve the unbalance issue. One submodule consists of two switches and one shunt capacitor. By charging or discharging the shunt capacitor, voltage balancing can be achieved. The VBC is experimentally verified with four series connected SiC MOSFET submodules up to 3 kV DC voltage. Voltage balancing is achieved within 5 % of an expected balanced voltage.**

Keywords— Wide bandgap (WBG) device; Silicon carbide (SiC) MOSFET; Series connection; Voltage balancing control.

I. INTRODUCTION

Silicon (Si) power device is the most commonly used device in power electronics applications. However, the physical property of the Si limits the performance of power device regarding switching frequency and blocking voltage. Therefore, SiC devices are increasingly being considered as a potential substitute to Si devices due to their capability of higher switching frequencies and higher voltages [1]. Despite of the potential high voltage capability of SiC device, the highest blocking voltage of a commercial discrete SiC MOSFET is limited and not able to meet high voltage demand in power converter applications. To fulfill the high voltage demand, multiple devices can be connected in series which makes higher voltage capability achievable. Another advantage of series connection is lower on-resistance than using a single higher voltage rating device [2]. However, a main problem of series connection is a voltage unbalance issue caused by difference of device characteristics and mismatch in gate signals due to delay of external gate drive circuit. The unbalance voltages can harm the devices. In order to solve the unbalance issue, voltage balancing control (VBC) is required in device series connection.

In general, the VBC for series connection consists of two parts, drain-side control and gate-side control [3]. For the drain-side control, a passive snubber circuits are commonly used. A snubber circuit is studied and experimentally verified with different devices [4]–[6]. It is easy to implement. However, using passive snubber circuit causes a additional switching losses with slow switching speed. Since a fast switching speed is one of main advantage of using SiC device, a passive snubber circuit ruined a merit of using SiC device.

The other method is the gate-side control. A digital signal processor (DSP) or a field-programmable gate array (FPGA) based control techniques and external balancing circuits to the gate side have been studied [7]–[15]. Even though this method allows faster switching speed than using snubber circuit, it is

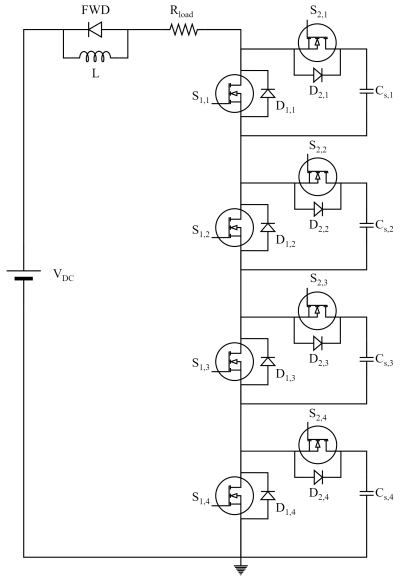


Figure 1. Circuit configuration of series connection

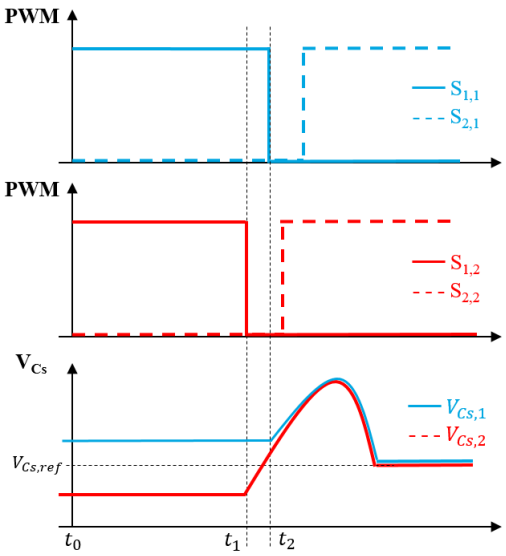


Figure 2. Voltage balancing operation principle

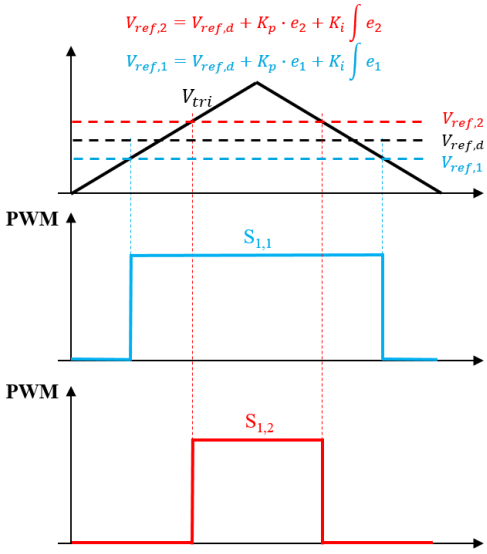


Figure 3. PWM siganal generation with adjusted duty ratio

complicated and difficult to implement.

In this paper, a VBC with capacitor charging method is studied for series connected SiC MOSFET submodules. The VBC allows fast switching speed and accurate voltage balancing with simple PI-based control algorithm. The main idea is to control PWM signals to charge or discharge capacitors for voltage balancing. A fundamental control technique is first proposed in [16] for stacked Si IGBT modules with analog control circuits. Due to the fast switching speed of SiC device, it requires high precision of controller which is more challenging than control of Si device. In order to achieve a precise control, a DSP is used instead of analog control circuits in this work due to its flexibility. A PI controller is proposed in this work, which provides faster voltage balancing compared to the P controller as presented in [16]. Since the PWM signals are directly controlled by DSP and capacitors are charged and discharged by the controllable PWM signals, there is no need of extra control circuits. Besides, the proposed VBC can achieve a highly accurate voltage balancing, within 5 % tolerance.

The rest of this paper is organized as follows: In Section II, the voltage balancing control with capacitor charging method is described; in Section III, the hardware circuit board and experimental results are presented; finally, Conclusion is presented in Section IV.

II. Voltage Balancing Control with Capacitor Charging Method

A. Circuit Configuration and Operation Principle

A test circuit with four series connected submodules is shown in Figure. 1. One submodule consists of two switches ($S_{1,n}$, $S_{2,n}$) and one shunt capacitor ($C_{s,n}$) ($n = 1, ..., N, N = 4$). The two switches are turned on and off complementary. When the main switch ($S_{1,n}$) is turned on, the submodule is conducted. On the other hand, when $S_{1,n}$ is turned off and auxiliary switch ($S_{2,n}$) is turned on, the module becomes open circuit with a voltage determined by capacitor voltage ($V_{Cs,n}$). During turn-off transient of $S_{1,n}$, the drain current will commute to the auxiliary branch and charge $C_{s,n}$ through $D_{2,n}$ due to stray inductance. This charging current results in a spike in the capacitor voltage. Once the $S_{2,n}$ is fully turned on, the capacitor will release this charge back to the source.

Figure. 2 shows the operation principle with waveforms. In the waveforms, the $V_{Cs,2}$ is lower than $V_{Cs,ref}$ during $t_0 - t_1$, where $V_{Cs,ref}$ is a reference of balanced capacitor voltage. Therefore, the $C_{s,2}$ should be connected to the circuit earlier than $C_{s,1}$ and charged more. This results from decreased duty ratio of $S_{1,2}$. On the other hand, the $V_{Cs,1}$ is higher than $V_{Cs,ref}$ during $t_0 - t_1$ which requires increased duty ratio of $S_{1,1}$ to lower $V_{Cs,1}$. Eventually, $S_{1,2}$ and $S_{1,1}$ will be turned off at t_1 and t_2 respectively. The capacitor $C_{s,1}$ will be connected to the circuit later than $C_{s,2}$ and thus the $C_{s,2}$ is charged for a longer time than $C_{s,1}$. This results in balanced voltages between the two capacitors.

Figure. 3 shows how the PWM signals in Figure. 2 are generated. Triangular carrier (V_{tri}) is shared by all the modules; $V_{ref,d}$ is a initially defined reference signal to achieve a desired duty ratio; K_p is proportional gain and K_i is integral gain. As shown in Figure. 3, the $V_{ref,d}$ is shifted with an offset determined by the corresponding e_n feedback, where $e_n = V_{Cs,ref} - V_{Cs,n}$. Given that $V_{Cs,1}$ is higher than $V_{Cs,ref}$, the reference signal of 1^{st} module ($V_{ref,1}$) becomes negatively shifted. On the contrary, $V_{ref,2}$ is positively shifted since $V_{Cs,2}$ is lower than $V_{Cs,ref}$. During turn-off, it can be seen in Figure. 2 that $C_{s,2}$ is connected earlier and thus charged more. In other words, if $V_{Cs,n}$ needs to be increased, the duty ratio of $S_{1,n}$ is decreased so that $C_{s,n}$ is charged more. If $V_{Cs,n}$ should be decreased for voltage balancing, the duty ratio of $S_{1,n}$ is

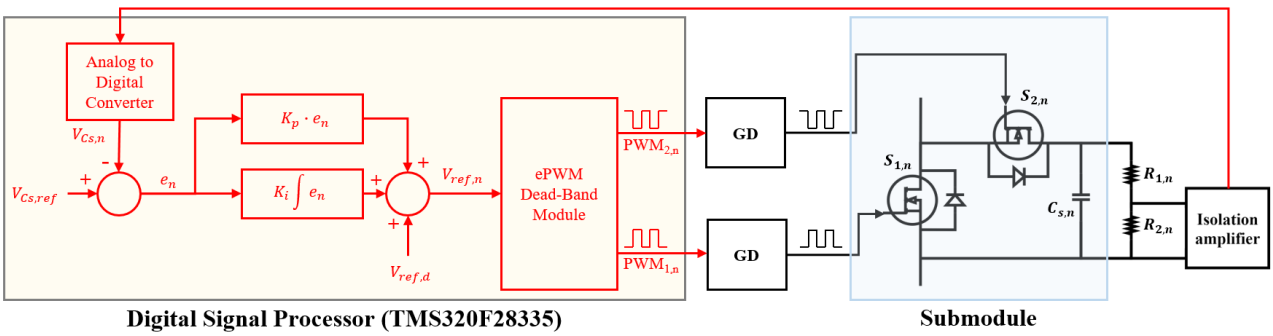


Figure 4. Schematic diagram of the proposed VBC for one SiC MOSFET submodule

increased.

B. Voltage Balancing Controller Design

A controller diagram of one submodule is shown in Figure. 4. It is closed loop control with $V_{Cs,n}$ feedback signal. The feedback signal is isolated by an isolation amplifier (AMC1311) and converted to digital signal in DSP. The $V_{Cs,n}$ is compared with the $V_{Cs,ref}$ to calculate how much the capacitor voltage is unbalanced from reference voltage. The $V_{Cs,ref}$ is predefined reference of balanced capacitor voltage which is V_{DC}/N. The e_n is used in the proposed PI controller to determine the amount of the $V_{ref,d}$ shift. As a result, $V_{ref,n}$ is calculated in the following equation; $V_{ref,n} = V_{ref,d} + K_p \cdot e_n + K_i \int e_n$. The calculated $V_{ref,n}$ is used in ePWM Dead-Band Module to generate two complimentary PWM signals ($PWM_{1,n}$, $PWM_{2,n}$) with a dead time to avoid short circuit.

III. Experimental Verification

A. Test Setup

The circuit configuration of Figure. 1 is implemented in hardware as shown in Figure. 5. A DC link and load resistors are connected to a mother board. A TI TMS320F28335 DSP is used in this work which operates at 150 MHz with 32 bit CPU and provides a 12 bit resolution of analog to digital converter. A Rohm semiconductor 650 V SiC MOSFET (SCT3120AL) is first adopted for the test [17] and its system parameters are listed in Table I. The proposed VBC is tested at different DC voltages (1.6 kV, 2 kV) with 400 Ω at 20 kHz switching frequency with maximum 10 kW power. A shunt capacitance is chosen as 1 μF based on parameter selection studies in [16], [18].

B. Experimental Results

Experimental results of SCT3120AL SiC MOSFETs are shown in Figure. 6-10. Device voltages of four main switches ($V_{S1,n}$, $n = 1, ..., 4$) are measured. When the main switch is turned off, the $V_{S1,n}$ is the voltage across the $C_{S,n}$ which indicates that the voltage balancing of $C_{s,n}$ results in the balancing of device voltages ($V_{S1,n}$). In this work, a voltage balancing is defined as when the all voltages are within 5 % tolerance of balanced voltage (V_{DC}/N). Figure. 6 shows unbalanced voltages at 1.6 kV DC voltage without the VBC. In order to study how the PI controller improves balancing control, P controller is first tested and voltage balancing time is measured. With the P controller, voltage balancing is achieved in 3.01 ms as shown in Figure. 7. For the proposed VBC with PI controller, voltage balancing is achieved in 2.24 ms which is 25 % faster balancing time than P controller as shown in Figure. 8 (a).

The balancing process of device voltages are shown in Figure. 8 (b). It is observed that different devices have different duty ratio for voltage balancing. Since $V_{S1,2}$ and $V_{S1,3}$ have to be increased, the duty ratios of the $S_{1,2}$ and $S_{1,3}$ are decreased. Therefore, positive pulse widths of $V_{S1,2}$ and $V_{S1,3}$ are increased which results in more charged capacitor voltages. In reversely, the duty ratios of $S_{1,1}$ and $S_{1,4}$ are increased to

Table I. Test circuit parameters for SCT3120AL SiC MOSFET

Parameters	Value
DC voltage (V_{DC})	1.6 kV, 2 kV
Load resistor (R_{load})	400 Ω
Inductance (L)	390 μH
Shunt capacitance (C_s)	1 μF
Switching frequency (f_{sw})	20 kHz

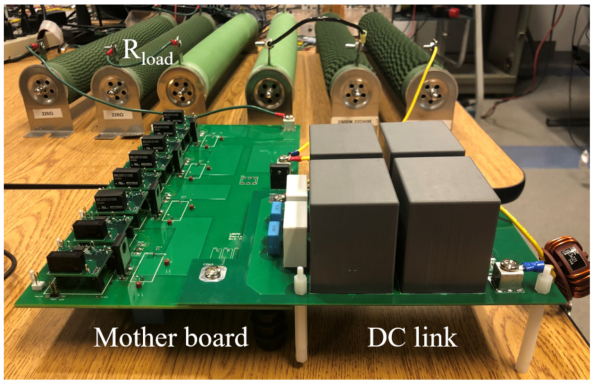


Figure 5. Hardware test setup

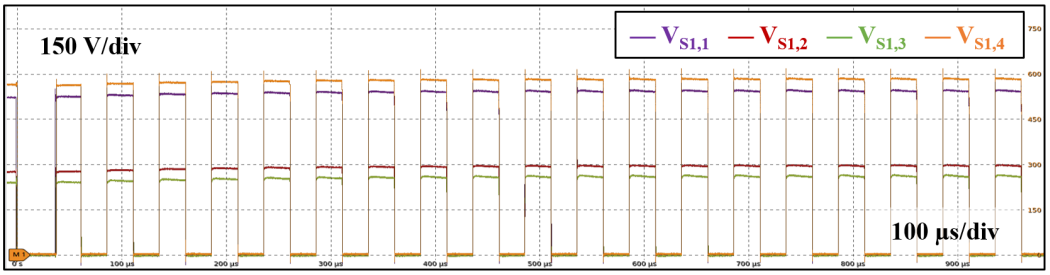


Figure 6. Unbalanced voltages of SCT3120AL SiC MOSFETs without VBC at 1.6 kV

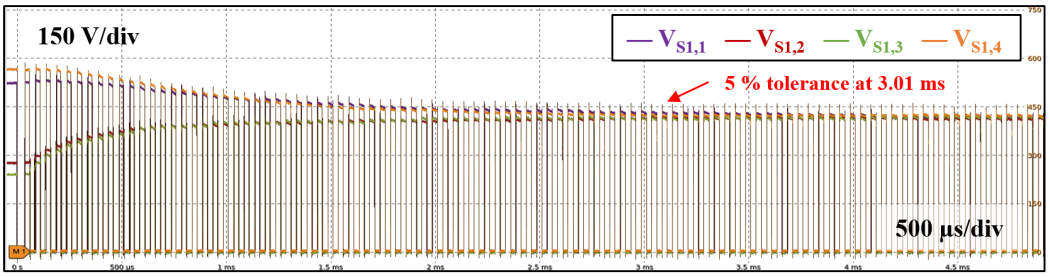
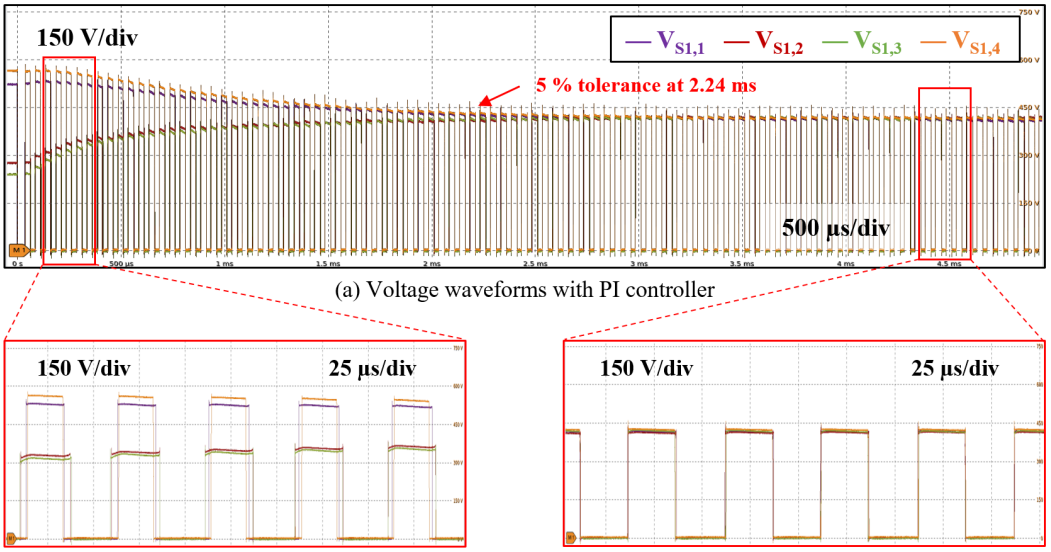


Figure 7. Balanced voltages of SCT3120AL SiC MOSFETs with P controller at 1.6 kV



(a) Voltage waveforms with PI controller

(b) Voltage balancing process waveforms

(c) Balanced voltage waveforms

Figure 8. Balanced voltages of SCT3120AL SiC MOSFETs with the proposed VBC using PI controller at 1.6 kV

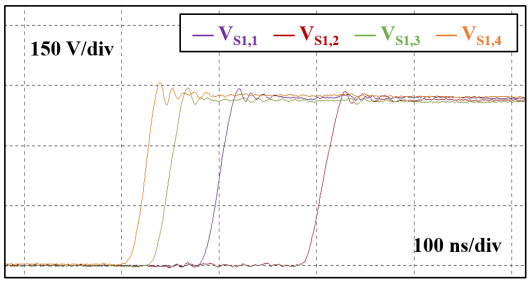


Figure 9. Dynamic voltage sharing of devices at 1.6 kV

reduce $V_{S1,1}$ and $V_{S1,4}$. When the voltages are unbalanced, duty ratio of each device is controlled to charge or discharge capacitors. Once the voltage balancing is achieved, duty ratio of each device will be same as predefined value depending on $V_{ref,d}$.

Figure. 8 (c) shows that the four main switches have same duty ratio which is 50 % when the voltages are balanced. Dynamic voltage sharing of devices are shown in Figure. 9. A 20.5 ns is measured as an average voltage rising time (t_{rise}) of four devices. It shows that the proposed VBC does not ruin the fast switching speed of SiC device since a typical t_{rise} of SiC device is tens of nanoseconds. Voltage balancing at 2 kV is tested as shown in Figure. 10. Since the highest voltage capability of four series connection is 2.6 kV with SCT3120AL (650 V), 2 kV is selected as highest DC voltage for voltage balancing test of SCT3120AL device.

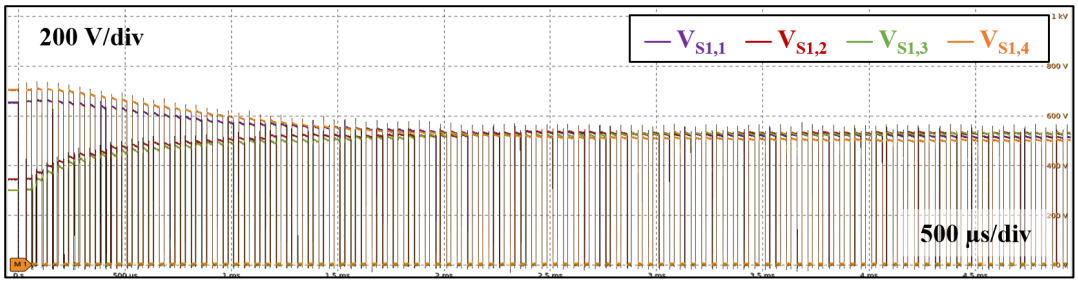


Figure 10. Balanced voltages of SCT3120AL SiC MOSFETs with the proposed VBC using PI controller at 2.0 kV

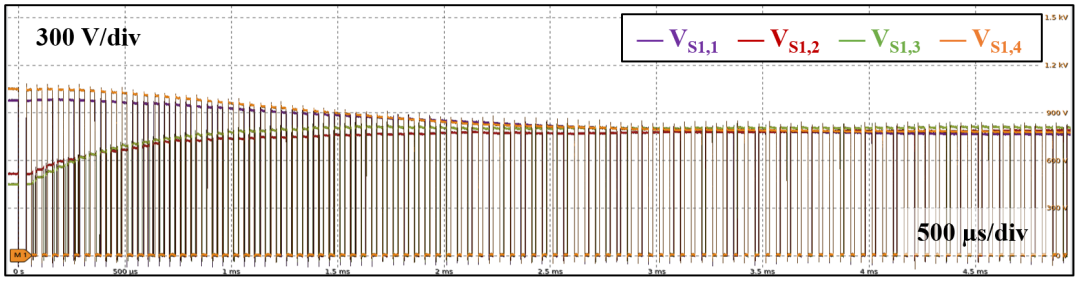


Figure 11. Balanced voltages of C2M0280120D SiC MOSFETs with the proposed VBC using PI controller at 3.0 kV

In order to study the VBC at higher DC voltage, a CREE 1.2 kV SiC MOSFET (C2M0280120D) is adopted [19]. System parameters of the test circuit with C2M0280120D SiC MOSFETs are listed in Table II. DC voltage is 3 kV and 3.25 A load current with 9.75 kW power. As shown in Figure. 11, voltage balancing is achieved at 3 kV with C2M0280120D SiC MOSFETs as well.

Table II. Test circuit parameters for C2M0280120D SiC MOSFET

Parameters	Value
DC voltage (V_{DC})	3 kV
Load current (I_{load})	3.25 A
Inductance (L)	390 µH
Shunt capacitance (C_s)	1 µF
Switching frequency (f_{sw})	20 kHz

IV. Conclusion

A VBC with PI controller using capacitor charging method is studied for four series connected SiC MOSFET submodules. The VBC is experimentally verified with two different SiC MOSFETs at 20 kHz. The 650 V SiC MOSFET is tested at 2 kV with 10 kW and the 1.2 kV SiC MOSFET is tested at 3 kV with 9.75 kW. In both devices, the proposed VBC achieves a highly accurate voltage balancing, within 5 % tolerance.

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References

[1] Z. Chen, "Characterization and modeling of high-switching-speed behavior of SiC active devices," Master's thesis, Virginia Tech, 2009.

[2] A. Bolotnikov, P. Losee, A. Permuy, G. Dunne, S. Kennerly, B. Rowden, J. Nasadoski, M. Harfman-Todorovic, R. Raju, F. Tao, P. Cioffi, F. J. Mueller, and L. Stevanovic, "Overview of 1.2kV 2.2kV SiC MOSFETs targeted for industrial power conversion applications," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2015, pp. 2445–2452.

[3] N. Y. A. Shammas, R. Withanage, and D. Chamund, "Review of series and parallel connection of IGBTs," *IEE Proceedings - Circuits, Devices and Systems*, vol. 153, no. 1, pp. 34–39, Feb 2006.

[4] K. Vechalapu, S. Bhattacharya, and E. Aleoiza, "Performance evaluation of series connected 1700V SiC MOSFET devices," in *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Nov 2015, pp. 184–191.

[5] K. Vechalapu and S. Bhattacharya, "Performance comparison of 10 kV-15 kV high voltage SiC modules and high voltage switch using series connected 1.7 kV LV SiC MOSFET devices," pp. 1–8, Sept 2016.

[6] K. Vechalapu, S. Hazra, U. Raheja, A. Negi, and S. Bhattacharya, "High-speed medium voltage (MV) drive applications enabled by series connection of 1.7 kV SiC MOSFET devices," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Oct 2017, pp. 808–815.

[7] K. Wada and K. Shingu, "Voltage Balancing Control for Series Connected MOSFETs Based on Time Delay Adjustment Under Start-Up and Steady-State Operations," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2018, pp. 5495–5499.

[8] P. Wang, F. Gao, Y. Jing, Q. Hao, K. Li, and H. Zhao, "An Integrated Gate Driver with Active Delay Control Method for Series Connected SiC MOSFETs," in *2018 IEEE 19th*

Workshop on Control and Modeling for Power Electronics (COMPEL), June 2018, pp. 1–6.

[9] S. Ji, F. Wang, L. M. Tolbert, T. Lu, Z. Zhao, and H. Yu, "An FPGA-Based Voltage Balancing Control for Multi-HV-IGBTs in Series Connection," *IEEE Transactions on Industry Applications*, vol. 54, no. 5, pp. 4640–4649, Sep. 2018.

[10] Z. Zhang, H. Gui, J. Niu, R. Chen, F. Wang, L. M. Tolbert, D. J. Costinett, and B. J. Blalock, "High Precision Gate Signal Timing Control Based Active Voltage Balancing Scheme for Series-Connected Fast Switching Field-Effect Transistors," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2018, pp. 925–930.

[11] A. Marzoughi, R. Burgos, and D. Boroyevich, "Active Gate-Driver With dv/dt Controller for Dynamic Voltage Balancing in Series-Connected SiC MOSFETs," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 4, pp. 2488–2498, 2019.

[12] C. Abbate, G. Busatto, and F. Iannuzzo, "High-Voltage, High-Performance Switch Using Series-Connected IGBTs," *IEEE Transactions on Power Electronics*, vol. 25, no. 9, pp. 2450–2459, Sept 2010.

[13] E. Raszmann, K. Sun, R. Burgos, I. Cvetkovic, J. Wang, and D. Boroyevich, "Voltage Balancing of Four Series-Connected SiC MOSFETs under 2 kV Bus Voltage using Active dv/dt Control," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019, pp. 6666–6672.

[14] S. Parashar and S. Bhattacharya, "Active Voltage Balancing Methodology for Series connection of 1700V SiC MOSFETs," in *2019 IEEE 7th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2019, pp. 430–437.

[15] S. Parashar and S. Bhattacharya, "A Novel Gate Driver for Active Voltage Balancing in 1.7kV Series Connected SiC MOSFETs," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2019, pp. 2773–2779.

[16] L. Yang, P. Fu, X. Yao, and J. Wang, "A module based self-balanced series connection for IGBT," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2014, pp. 1953–1958.

[17] SCT3120AL N-Channel Silicon Carbide Power MOSFET. [Online]. Available: `https://www.rohm.com/`

[18] L. Yue and X. Yao, "Implementation of a Self-Balancing Control for Series IGBTs," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2018, pp. 3700–3704.

[19] C2M0280120D Silicon Carbide Power MOSFET C2M^{TM} MOSFET Technology N-Channel Enhancement Mode. [Online]. Available: `http://http://www.cree.com/`