

Over-current Protection for Series-connected IGBTs based on Desaturation Detection

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Abstract—One major challenge regarding series-connected IGBTs is the protection against over-current faults, besides voltage balancing among the devices. In this paper, an over-current protection method based on desaturation detection is proposed for series-connected IGBTs which are controlled by a digital signal processor (DSP) to realize voltage sharing. A hardware test platform was built, which is capable of generating current spikes of various magnitudes and durations. Different aspects of system behavior under fault are characterized to provide design guidance to ensure safety. Finally, experimental results show that the proposed series IGBT control can achieve voltage balance without slowing down the switching transients. Additionally, the desaturation circuit can detect an over-current in less than $1\ \mu\text{s}$. Furthermore, with the proposed protection method, the fault can be fully cleared depending solely on voltage balancing circuits, while maintaining voltage balance during the entire process.

I. INTRODUCTION

The recent development in high-voltage dc (HVDC) transmission and flexible ac transmission (FACT) requires ever-increasing voltage blocking capabilities from semi-conductor switches. However, current commercial silicon IGBTs can only reach up to 6.5 kV. [1]. Consequently, series-connected IGBTs have been used to replace single devices as switching elements for the voltage-source converters in high-voltage applications.

The major challenge for implementing series IGBTs is the voltage balancing, because the different parameters and parasitic elements in the circuit may cause imbalanced voltage sharing, which can be dangerous for the devices. Extensive research has been done regarding the series IGBT voltage balancing, ranging from passive methods that rely mostly on snubber circuits [2], [3] to active techniques that utilize feedback, such as collector-emitter voltage, gate-emitter voltage, or collector-gate voltage, etc [4], [5]. For this paper, the voltage balancing of the series IGBTs is achieved using the method proposed in [6]. Compared to other active control techniques, it does not require high-speed, high-precision sampling and computing units since the feedback signals

are slow-changing capacitor voltages. What's more, with the method from [6], the IGBTs do not suffer from a slower switching as is sometimes the case with more complicated digital control methods.

Besides voltage balancing, series IGBT protection during faults is another important aspect which requires further investigation. There are two types of faults: open-circuit and over-current faults. This paper focuses on the over-current fault which is the more dangerous type since a high current spike threatens every IGBT in the series string and thus needs to be detected timely. The response time for over-current protection should be within $1\ \mu\text{s}$ [7], [8]. Multiple protection techniques have been proposed for single IGBTs in research papers [8]–[10], [13]. di/dt feedback control methods offer fast detection and can be integrated with soft turn-off after a fault detection. However, the circuit is complicated and the detections depend on stray inductance which can be hard to characterize and is sensitive to noises [7], [11]. In this paper, the desaturation detection method is chosen, since it can be realized with a simple and reliable circuit, and the detection is based on the actual fault current which may not be fast-rising [13].

One challenge for series IGBT protection is that if a fault is detected, the entire series branch should turn off in an organized manner. Therefore, passive voltage balancing for series IGBTs [12] is unfit due to the lack of coordination. Contrarily, a central controller can be used to coordinate the IGBT actions during a fault. Another challenge concerns the fault clearing capability. If the series IGBTs are used to form a more complicated topology, such as a voltage source converter (VSC), simply turning off the series IGBTs may not stop the high fault current from flowing through their snubber circuits. Therefore, it is desirable if the series branch can clear the fault under the protection control. In this paper, a DSP is used for both voltage balancing for protection during a fault. Furthermore, an over-current fault generation platform is built, featuring a short-circuit IGBT and an air-core inductor, to inject a controlled current with a ramping rate of a few mega-amps per

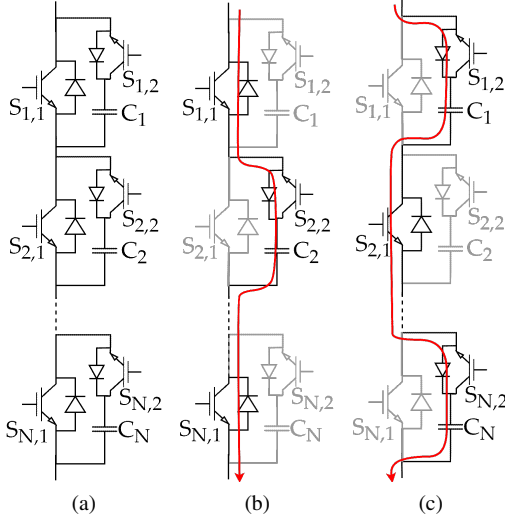


Figure 1: Series IGBT topology and operation principle. (a) main IGBTs and their auxiliary branches, (b) delayed turn-on for $S_{2,1}$, (c) delayed turn-off for $S_{2,1}$.

second. The short-circuit IGBT is only responsible for injecting the fault current, but not clearing it, to emulate a permanent fault. The fault current is withstood and cleared solely with the series IGBTs and their auxiliary circuits. Additionally, an over-current control scheme for series IGBTs is proposed, which manages to achieve the following goals:

- Fast over-current detection, able to actuate protection and fault clearance mechanisms within $1 \mu s$ after the fault current exceeds the trip level;
- Safe fault clearance that solely depends on the existing series IGBTs and their auxiliary circuits;
- Voltage balance during and after the fault to keep the IGBTs safe.

Furthermore, balancing controller resolution and related delay length, fault current clearance trajectory, and the resulted shunt capacitor voltage gains are characterized in the paper, which aims to provide guidance during the system design phase and offer explorations into series IGBT protection.

II. SERIES IGBT CONTROL

A. System Topology and Operation Modes

Fig. 1a shows the series IGBT circuit topology which consists of two parts. The first part is the main IGBTs connected in series with the annotation $S_{i,1}$. The second part is the auxiliary branches, including the auxiliary IGBTs $S_{i,2}$ and the shunt capacitors C_{Si} . $S_{i,1}$ and $S_{i,2}$ operate in a complementary manner and thus, balancing the main IGBTs' off-state voltages becomes balancing the shunt capacitor voltages [6], [14].

If one IGBT turns on with a delay, such as $S_{2,1}$ in Fig. 1b, its shunt capacitor stays inserted for a longer

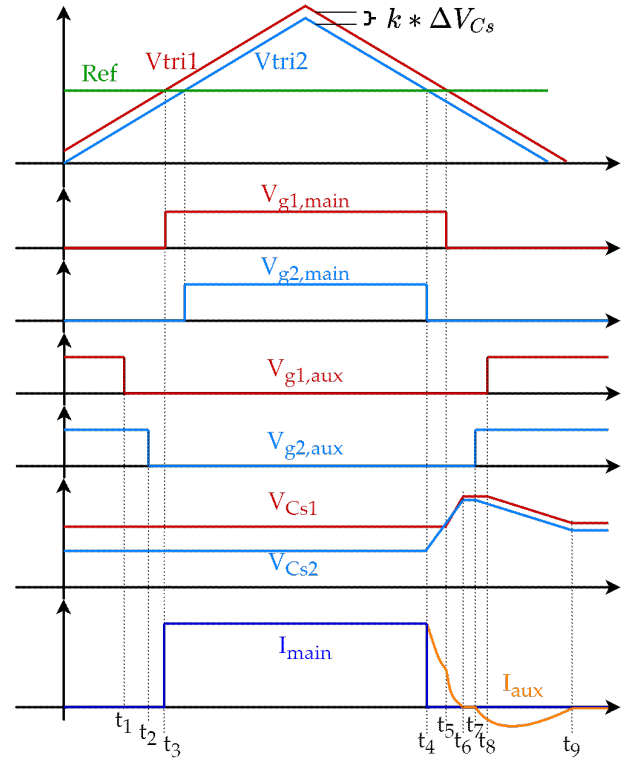


Figure 2: Illustrative waveforms for the voltage balancing control.

time and gets charged more. Therefore, when all the IGBTs are turned on eventually, V_{Cs2} rises compared to the others. Contrarily, if one module has a delayed turn-off, as shown in Fig. 1c, the corresponding capacitor gets charged less, and its voltage drops. Therefore, by applying gate delays, one can regulate the voltage sharing of the series string.

One way to generate such delays to actively regulate the capacitor voltages is illustrated in Fig. 2. Initially at $t = 0$, V_{Cs1} is higher than V_{Cs2} . Each capacitor voltage is then used to create a dc offset to add to the triangular carrier of the corresponding series module. When the carriers are used to compare with a common reference signal, delays are introduced to the PWM signals. From t_1 to t_3 , the voltage balancing are not affected, since no current charges or discharges the shunt capacitors, as a result of the previous steady-state. At t_4 , the first main IGBT, the one with a lower V_C , turns off. The falling string current starts to charge the capacitor and raise V_{Cs2} . V_{Cs1} also starts to rise after some delay and both capacitor voltages reach their peak when the current falls to 0 at t_6 . The extra charges stored in the capacitors from the falling current will be released when their auxiliary IGBTs turn on at t_7 and t_8 , respectively. This discharge will be over at t_9 and a new steady-state is established.

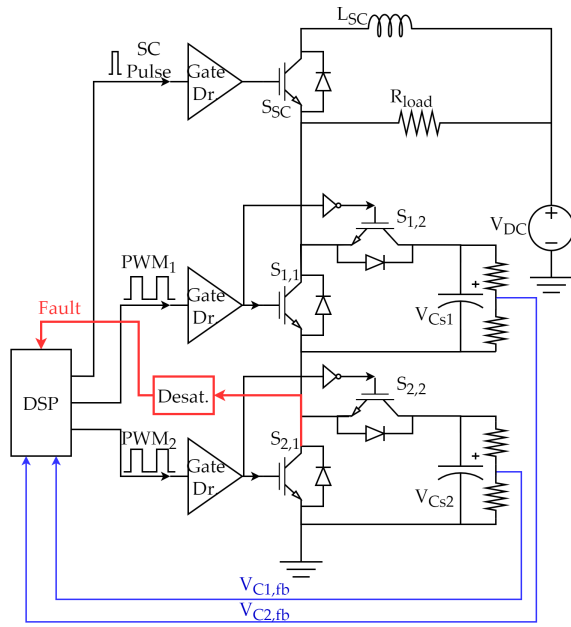


Figure 5: Schematic of the hardware test platform.

1) *State I: Normal Operation:* This is the default operation where all the over-current tests start. In State I, the DSP keeps the voltage sharing balanced. When the main IGBTs $S_{1,1}$ and $S_{2,1}$ are on, the branch current is I_{load} , determined by the source voltage and R_{load} . When the main IGBTs switch off, the tailing branch current commutes to the auxiliary branches.

2) *State II: Fault Current Ramp-up:* Once the DSP triggers S_{SC} , the over-current generation branch is connected to the system and the source voltage is imposed across the short-circuit inductor L_{SC} . The over-current I_{SC} then starts to ramp up following Eq. 3.

$$I_{SC} = \Sigma L * V_{dc} * t_{fault} \quad (3)$$

where ΣL is the sum of L_{SC} and stray inductance in the main branch, and t_{fault} is the duration of the fault until the main IGBTs turn off. Fig. 7 shows Simulink simulation results for I_{fault} and its ramp-up rate is 6.25 MA/s, determined by $V_{dc}/\Sigma L$. The rest of the simulation model parameters can be found in Table I. In the meantime, since all the auxiliary IGBT anti-parallel diodes are reverse biased, the shunt capacitors remain disconnected, maintaining voltages from the previous steady-state. At the end of State II, a fault detection will be made. However, before the main IGBTs start to turn off, the fault current will continue rising.

3) *State III: Fault Clearing:* This state starts when all the IGBTs have turned off and the fault current starts to commute to the auxiliary branches. A small portion of I_{SC} will flow through R_{load} , due to the voltage drop induced by L_{SC} . However, since it is much smaller

compared to the fault current that charges the shunt capacitors and it does not go through any switches, the resistor current I_R is ignored.

On the other hand, L_{SC} and the series shunt capacitors form an LC circuit with an initial current close to the peak I_{SC} . Therefore, I_{SC} is subject to the LC resonance and starts to oscillate following the resonance trajectory, as shown in Fig. 7. The resonance frequency can be calculated as follows.

$$f_0 = \frac{1}{T_0} = \frac{1}{2\pi\sqrt{\Sigma L \frac{C_s}{N}}} \quad (4)$$

where N is the number of series modules.

After one-fourth of the resonance cycle, the fault current reaches zero and the fault is cleared because with the proposed method, all the IGBTs are turned off and the auxiliary anti-parallel diodes are reverse biased. Both shunt capacitor voltages increase equally since the dominating factors to $\Delta V_{Cs1/2}$ are the common fault current and the shunt capacitance rather than stray elements or device parameter differences. The shunt capacitor voltage increase can be calculated using Eq. 5, ignoring the slow damping effect of the load resistor.

$$\begin{aligned} \Delta V_{Cs} &= \frac{1}{C_s} \int_0^{\frac{\pi\sqrt{\Sigma L C_s/N}}{2}} I_0 \cos \frac{t}{\sqrt{\Sigma L C_s/N}} dt \\ &= I_0 \sqrt{\frac{\Sigma L}{N C_s}} \end{aligned} \quad (5)$$

where I_0 is the peak fault current through the main IGBTs as well as the auxiliary anti-parallel diodes. In the system design phase, after the device voltage and current margins have been finalized and the parasitic inductance has been evaluated, Eq. 5 can be used to select the number of series IGBTs as well as the shunt capacitance.

4) *State IV: Post-fault Protection:* After the fault current falls to zero and all the switches are in blocking-state, the voltage sharing of the main IGBTs will be determined by the parasitic capacitances parallel to each IGBT C_{CE} , as shown in Fig. 6d. Therefore, the voltages may become imbalanced. However, if V_{CE} of one

Table I: Simulation and Experiment Parameters

Parameter	Value
V_{dc}	1 kV
L_{SC}	160 μH
L_{stray}	2 μH
R_{load}	320 Ohm
C_s	6 μF
f_{sw}	1 kHz
N	2

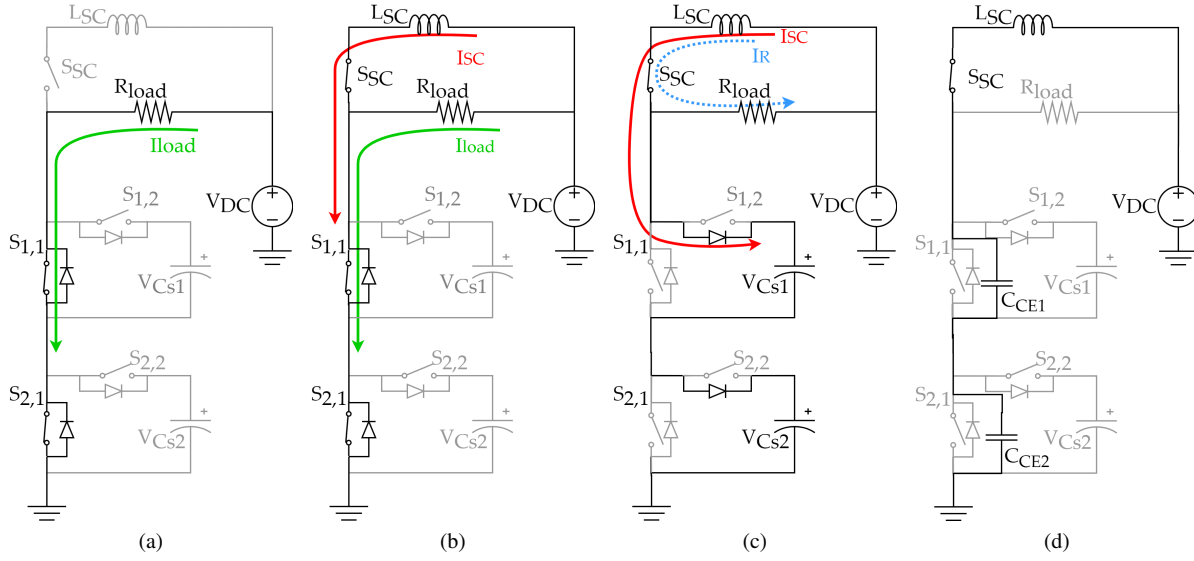


Figure 6: Current paths and inserted components during four operation states. (a) State I: normal operation, (b) State II: fault current ramp-up, (c) State III: fault clearing, (d) State IV: post-fault protection.

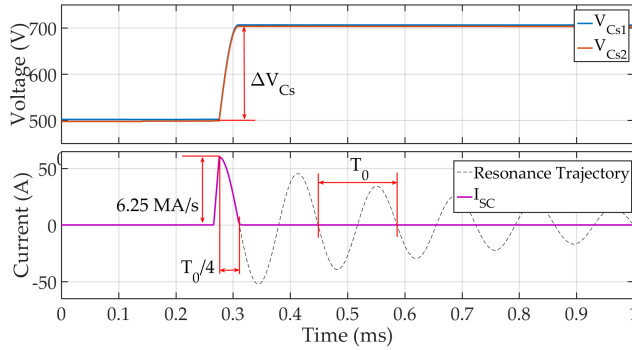


Figure 7: Simulation results for V_{Cs} and short-circuit current during fault.

main IGBT keeps rising, it will eventually become high enough to forward bias the auxiliary free-wheeling diode and become clamped at the corresponding V_{Cs} . Due to this voltage limiting effect, the series IGBTs will continue to be protected until further measures are taken, such as a system shut down.

IV. EXPERIMENTAL VALIDATION

The test platform circuit schematic is shown in Fig. 5 and the parameters are listed in Table I. The main and auxiliary IGBTs are IXBH42N170, while the short-circuit control switch is IXGN100N170. In this section, the test results will be presented and discussed first to demonstrate the voltage balancing control, and then series IGBT protection results will be used to illustrate the protection mechanism and its effectiveness.

A. Series IGBT Voltage Balancing Tests

Before demonstrating the voltage balancing control, series IGBT voltage sharing without it is first investigated. To do so, synchronous gate pulses were sent to the series modules from the DSP and the duty ratio is fixed at 50% without any delay added. The imbalanced voltage sharing waveforms are shown in Fig. 8.

It can be seen that when the dc bus voltage is 1 kV, the V_{CE} difference between the two series IGBTs is around 100 V or 10% of the bus voltage. The reason for the imbalance is because dV_{CE1}/dt is higher than dV_{CE2}/dt , as shown in the zoomed-in transient waveforms. This can be further explained by considering the two series modules and their parasitic capacitances to the ground. The higher ranking series module, or the $S_{1,1}$ module, has a larger voltage ramp during turn-off transients. Therefore, the parasitic capacitance to the ground in the higher ranking module will draw more current from the gate, which makes V_{CE1} rise faster than V_{CE2} [15]. In the turn-on transient, there exists a 20 ns delay between the two collector-emitter voltages. However, the determining factor for the voltage imbalance is still the difference in dV_{CE}/dt .

The series modules were tested again with voltage balancing control and the results are shown in Fig. 9. From the overall waveforms in Fig. 9a, it can be seen that the ΔV_{CE} has reduced greatly from 100 V to 2 V and both series IGBTs share the 1 kV equally. Fig. 9b and 9c show that the delays between V_{CE1} and V_{CE2} are 102 ns during turn-off and 38 ns during turn-on. Considering Eq. 1 and 2, the amount of delay is expected for the minor voltage imbalance when $k=1$. It can also be seen

that the voltage rise and fall times are short, even with a $6 \mu F$ shunt capacitor, because V_{CS} does not connect until V_{CE} has already reached 500 V. In summary, the voltage balancing control can effectively compensate the voltage imbalance caused by the parasitics in the circuit while not sacrificing the transient performance of the series string.

B. Over-current Protection

To display the series IGBT over-current protection mechanism, the critical waveforms of the desaturation detection circuit, as well as system behavior, are shown in Fig. 10. The maximum fault current generated in the experiments was 46 A and the IGBTs under test were still considered to be in the saturation region. Considering that a typical IGBT's dV_{CE}/dI_C is smaller in the saturation region than in the desaturation region, an over-current detector capable of detection in the saturation region will be sensitive enough in the desaturation region.

Fig. 10a presents the signal waveforms inside the desaturation detection circuit. At t_0 , the fault occurs and the IGBT collector current I_C starts to ramp up. In the meantime, the desaturation detection capacitor starts to get charged, since V_{CE} of the corresponding IGBT is rising, which is reflected in V_{CDE} . At t_1 , the fault current exceeds the trip value I_{trip} , and V_{CDE} reaches the trip voltage. The comparator then pulls the output Detect_out to low and the falling edge is used to alarm the DSP of an over-current fault. Upon receiving the falling edge, the DSP sends turn-off signals to all the IGBT gate drives. The time between t_1 and t_2 , which is approximately $0.8 \mu s$, is the gate driver processing delay. At t_2 , the gate drivers start turning off all the IGBTs, as shown by the downward bends in $V_{G1,M}$ and $V_{G2,M}$ in Fig. 10a. $0.6 \mu s$ later at t_3 , the main IGBTs have

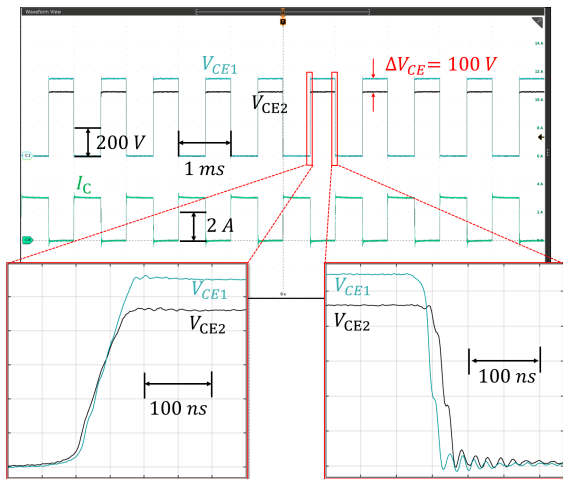
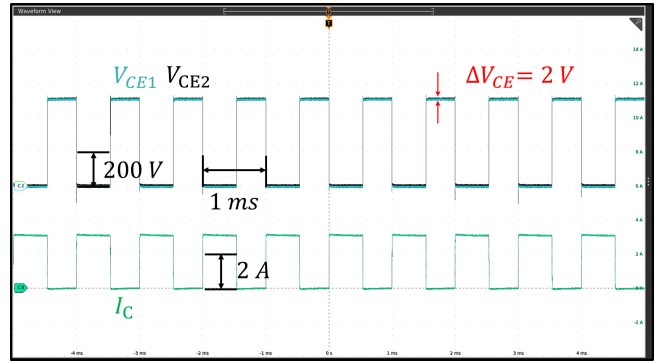
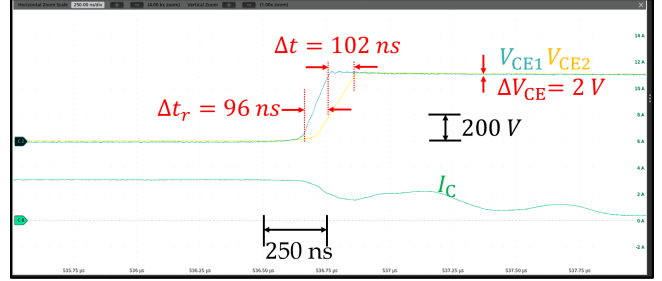


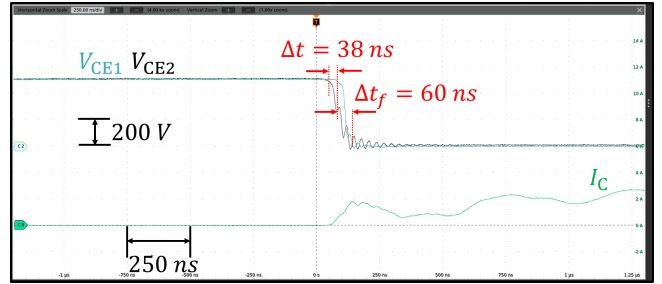
Figure 8: Voltage sharing without balancing control at 1 kV dc bus voltage.



(a) Overall voltage and current waveforms.



(b) Zoomed-in turn-off transient waveforms.



(c) Zoomed-in turn-on transient waveforms.

Figure 9: Voltage and current waveforms of balanced operation at 1 kV dc bus voltage.

finished discharging the miller capacitors and start to cut off the collector current. The fault current then commutes to the auxiliary branches and starts to charge the shunt capacitors now connected in series. The commutation of the fault current from main IGBTs to shunt capacitors causes it to oscillate, as illustrated in Fig. 6c. However, after one-fourth of the oscillation cycle, the fault current becomes below zero at t_4 , as shown in Fig. 10b. Since at this point, all the IGBTs are in blocking-state, no reverse current can flow from the shunt capacitors back to the dc bus, the fault is cleared.

Fig. 10b displays the system behavior under a typical fault which resulted in a 46 A peak fault current. The time between t_3 and t_4 is the fault clearance time. Given that L_{SC} is $160 \mu H$ and ΣC_S is $3 \mu F$, the clearing time can be calculated by the following equation.

$$t = \frac{\pi}{2} \sqrt{L_{SC} * \Sigma C_S} = 34.4 \mu s \quad (6)$$

As shown in Fig. 10b, the measured fault clearance time is around $32 \mu s$. Fig. 10b also shows that V_{CE1} and V_{CE2} can maintain balance from t_3 to t_4 , during which they are determined by the corresponding shunt capacitor voltages. V_{CS1} and V_{CS2} , on the other hand, both increase, since they are charged by the falling fault current. Each shunt capacitor voltage gain can be calculated using the equation below which is derived from Eq. 5.

$$\Delta V_{CE} = \frac{1}{C_s} \int_{t_3}^{t_4} i_{fault} dt = 139.2V \quad (7)$$

The measured maximum ΔV_{CE} in Fig. 10b is 138 V. The shunt capacitors ensure that during a fault, series voltage balance is maintained, because it is determined by the shunt capacitor voltages and the fault current, rather than parasitic capacitance voltages. Furthermore, because of the relatively high capacitance, the shunt capacitors limit the series module voltage gain during a fault.

To further demonstrate the versatility of the proposed over-current detection circuit, a series of tests were done with varying V_{Trip} and their corresponding trip currents were recorded. The test results are listed in Table II and plotted in Fig. 11. As shown in Table II, changing V_{Trip} directly affects the trip current over a wide range. It can also be seen that, even with low fault currents, the proposed detector circuit can still distinguish a fault from normal operation using V_{Trip} . The graph in Fig. 11 indicates that V_{Trip} changes with I_{Trip} following the device I-V curve. Therefore, to select

Table II: V_{Trip} and corresponding I_{Trip} .

V_{Trip} (V)	3.5	3.7	3.8	3.9	4
I_{Trip} (A)	3	4	5.4	8.4	12
V_{Trip} (V)	4.05	4.1	4.15	4.2	
I_{Trip} (A)	14.6	17.2	27.6	37	

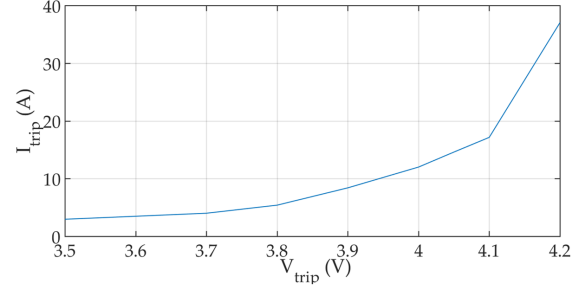


Figure 11: Trip current values based on different trip voltages.

a trip current for the proposed protection circuit, one can refer to the device datasheet and use the corresponding $V_{CE} + V_{DDE,f}$ as V_{Trip} .

V. CONCLUSIONS

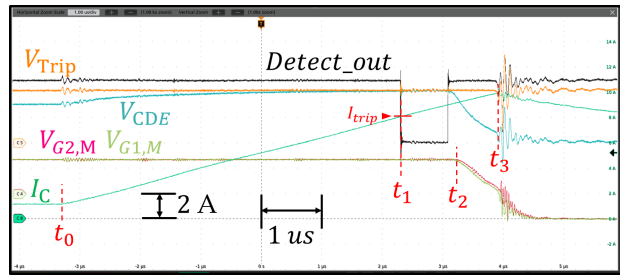
This paper proposed an over-current protection method for series-connected IGBTs. The protection method utilizes the outputs of a desaturation detection circuit to alert the DSP which then triggers an organized shutdown of all the IGBTs under fault. The DSP also serves as a central controller responsible for series IGBT voltage balancing which is realized by generating gate delays based on shunt capacitor voltage feedback. Additionally, a test platform capable of generating high current spikes in a controlled way was designed and built. The operation of the test platform was presented and system behaviors, namely fault current and shunt capacitor voltage gain under fault, are characterized. Experimental results show that during normal operation, series IGBTs can achieve balanced voltage sharing without sacrificing transient performance. During a fault, the protection circuit can detect the fault in less than $1 \mu s$ and react to it in $1.5 \mu s$. Furthermore, the fault clearance depends solely on the series IGBTs and their auxiliary circuits, which can simultaneously maintain voltage balance under fault.

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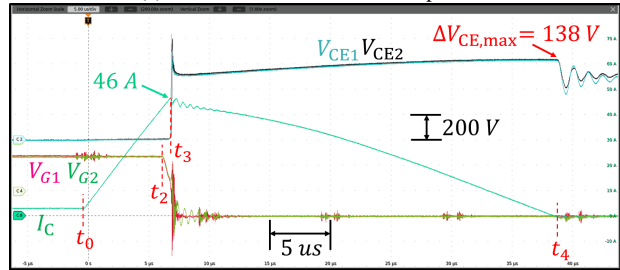
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REFERENCES

- [1] B. J. Baliga, *The igbt device: design and applications of the insulated gate bipolar transistor*. Binghamton: Elsevier Science & Technology Books, 2015, ch. 20, p. 668.



(a) Over-current fault detection process.



(b) Fault current and series IGBT voltage sharing during the fault.

Figure 10: Experimental results demonstrating a complete fault detection to clearance process.

- [2] J. Chen, J. Lin, and T. Ai, "The techniques of the serial and paralleled igbts," in *Proc. IEEE 22nd International Conference on Industrial Electronics, Control, and Instrumentation*, Taipei, Taiwan, 1996, pp. 999 – 1004.
- [3] X. Chen, L. Yu, T. Jiang, H. Tian, K. Huang, and J. Wang, "A fast and series-stacked igbt switch with balanced voltage sharing for pulsed power applications," *IEEE Transactions on Plasma Science*, vol. 45.
- [4] T. Lu, Z. Zhao, J. Shiqi, H. Yu, and L. Yuan, "Active clamping circuit with status feedback for series-connected hv-igbts," *IEEE Transactions on Industry Applications*, vol. 50, no. 5, pp. 3579 – 3590, 2014.
- [5] W. He, P. Palmer, and X. Zhang, "Igbt series connection under active voltage control," in *2011-14th European Conference on Power Electronics and Applications (EPE 2011)*, Birmingham, UK, Aug. 2011.
- [6] L. Yang, P. Fu, X. Yao, and J. Wang, "A module based self-balanced series connection for igbt," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2014.
- [7] F. F. F. Huang, "Igbt fault protection based on di/dt feedback control," in *Proc. IEEE Power Electron. Spec. Conf.*, FL, USA, 2007.
- [8] X. Zhang, H. Li, J. Brothers, L. Fu, M. Perales, J. Wu, and J. Wang, "A gate drive with power over fiber-based isolated power supply and comprehensive protection functions for 15-kv sic mosfet," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 946 – 955, Jun. 2016.
- [9] B. Lu and S. K. Sharma, "A literature review of igbt fault diagnostic and protection methods for power inverters," *IEEE Transactions on Industry Applications*, vol. 45, no. 5, pp. 1770–1777, Sept. 2009.
- [10] U. Choi, F. Blaabjerg, and K. Lee, "Study and handling methods of power igbt module failures in power electronics converter systems," *IEEE Transactions on Power Electronics*, vol. 30, no. 5, pp. 2517–2533, May 2015.
- [11] Z. Wang, X. Shi, L. M. Tolbert, F. Wang, and B. J. Blalock, "A di/dt feedback-based active gate driver for smart switching and fast overcurrent protection of igbt modules," *IEEE Transactions on Power Electronics*, vol. 29, no. 7, pp. 3720 – 3732, Jul. 2014.
- [12] R. Chokhawala and S. Sobhani, "Switching voltage transient protection schemes for high current igbt modules," in *Proc. IEEE Applied Power Electronics Conference and Exposition*, 1994, FL, USA, 1994.
- [13] R. Chokhawala, J. Catt, and L. Kiraly, "A discussion on igbt short-circuit behavior and fault protection schemes," *IEEE Transactions on Industry Applications*, vol. 31, no. 2, pp. 256 – 263, Apr. 1995.
- [14] L. Yue and X. Yao, "Implementation of a self-balancing control for series igbts," in *2018 IEEE Energy Conversion Congress and Expo (ECCE)*, Portland, OR, USA, 2018.
- [15] T. V. Nguyen, P. Jeannin, E. Vagnon, D. Frey, and J. Crebier, "Series connection of igbts with self-powering technique and 3-d topology," *IEEE Transactions on Industry Applications*, vol. 47, no. 4, pp. 1844 – 1852, May 2011.