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Active Voltage Balancing of Series Connected SiC MOSFET Submodules Using Pulsewidth Modulation

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ABSTRACT Series connection of multiple transistors is an attractive solution to achieve higher voltage capability. However, the voltage imbalance among the series-connected devices is a critical issue caused by mismatches of device characteristics and gate signals. To prevent the failure of devices from the voltage imbalance, voltage balancing control (VBC) is required. In this work, an active VBC for series-connected silicon carbide (SiC) MOSFET submodules is proposed with a pulsewidth modulation (PWM) method. A submodule consists of two switches and one shunt capacitor, and the PWM method actively controls the capacitor voltages for balancing. The proposed VBC is simulated in MATLAB/Simulink and experimentally verified with six series-connected SiC MOSFET submodules at up to 150 kHz. The voltage balancing is achieved within 3.9% of the targeted balanced voltage.

INDEX TERMS Pulsewidth modulation (PWM), series connection, silicon carbide (SiC) MOSFET, voltage balancing control (VBC), wide bandgap device.

I. INTRODUCTION

Silicon (Si)-based power devices, such as insulated gate bipolar transistors (IGBTs) and metal oxide semiconductor field effect transistors (MOSFETs), have been widely adopted in power electronics applications over several decades. However, switching frequency and blocking voltage of Si power devices are limited due to the physical property of Si [1]–[3]. Consequently, SiC devices are increasingly considered as a potential substitute for Si devices given their capability of higher switching frequencies and higher voltages [4], [5].

Different studies have been reported on SiC MOSFETs with a high blocking voltage over 10 kV [6]–[8]. However, due to limitations of the manufacturing technology and cost, the maximum voltage rating of commercially available discrete SiC MOSFET is 1.7 kV [9], which is inadequate to meet the high voltage demand in power converter applications. Series connection of multiple devices is an effective way to achieve high voltage capability. Another advantage of series connection compared to a single higher rating device is lower on-resistance [10]. A critical issue of series connection is voltage imbalance caused by differences in device characteristics and mismatches in gate signals. The unbalanced voltages may lead to device failure. Hence, extensive studies have been proposed for voltage balancing of series-connected devices, such as passive snubber circuit, active gate control, and capacitive coupling method.

Passive snubber circuits are widely used for series-connected devices considering their simplicity and reliability. A passive RC snubber circuit was studied to find the optimal RC values for series-connected SiC MOSFETs [11], [12]. However, the use of snubber circuits sacrifices the fast switching speed of SiC MOSFET and causes a considerable amount of losses due to energy dissipation of the capacitor. To reduce the losses, a controlled RC passive snubber system was proposed [13]. However, an extra on-board high voltage power supply is required per each stack of devices.

Active gate control method allows faster switching speed compared to passive snubber circuits. Different active gate drivers were proposed to control dv/dt actively with gate resistance modulation techniques [14], [15]. To compensate for dv/dt differences between series-connected devices, gate signal delay control schemes were proposed with delay line

ICs [16], [17] and a high-resolution pulsewidth modulator from micro-controllers [18]. An auxiliary gate current method was proposed to modify dv/dt by using an external Miller capacitor [19], and it was expanded for a higher number of series-connected devices [20], [21]. However, these active gate control methods require high-precision control and high-bandwidth analog components which result in increased complexity of the system and makes it difficult to implement for a higher number of devices.

In contrast, capacitive coupling drive method is utilized to reduce the complexity of the system [22]–[24]. All the series-connected devices can be controlled by a single gate driver with multiple driving capacitors. However, voltage imbalance still exists, and its performance of voltage balancing needs to be optimized.

Most of the control methods are designed and validated at limited test condition. First, the number of series connected device is only two in most cases [11], [14]–[19], [23]. Multiple series connection of SiC MOSFETs are more attractive for medium and high voltage power converters because the rated voltage of two series-connected device may still not be high enough in many cases. An active voltage balancing scheme is implemented up to eight series connection [21]. However, the voltage mismatch among devices is 30%, and therefore the voltage balancing performance should be improved. Snubber capacitor technique was studied for eight series connected SiC MOSFETs in a dc/dc converter and achieved accurate voltage balancing [25]. However, the voltage rise time is above 700 ns which is much longer than typical rise time of SiC MOSFETs (tens of ns). Second, the switching frequency is less than 50 kHz in most cases, much lower than the switching frequency capability of SiC MOSFETs.

In this paper, a VBC for series-connected SiC MOSFET submodules is proposed with PWM method to efficiently balance the device voltages. The major advantages of the proposed VBC are listed as follows:

1) The proposed VBC can realize the full fast switching speed potential of SiC MOSFET and is validated at high switching frequency of 150 kHz.
2) The PWM signals are controlled by a central controller. Therefore, extra control circuits are not required, which makes it straightforward to implement for a higher number of series-connected devices. Up to six series-connected submodules are verified in this paper.
3) Accurate voltage balancing can be achieved within 3.9% of the targeted balanced voltage.

A fundamental idea was first proposed in [26] and tested [27] for stacked Si IGBT submodules with proportional (P)-control based analog circuit controllers. It controls pulsewidths of the gate signals for capacitor voltage balancing by delaying the rising and falling edges of gate signals separately with analog delay circuits.

For SiC devices, the dynamic characteristic is more sensitive than Si-based devices to the parasitic inductances of circuit components due to the fast switching speed. This induces overshoot or high frequency oscillation in current and voltage waveforms and makes the circuit design more challenging. In order to minimize power loop and submodule loop inductance, magnetic cancellation schemes [28], [29] are applied to printed circuit board design. Decoupling capacitors are designed to decouple the parasitic inductance of dc link [30], [31].

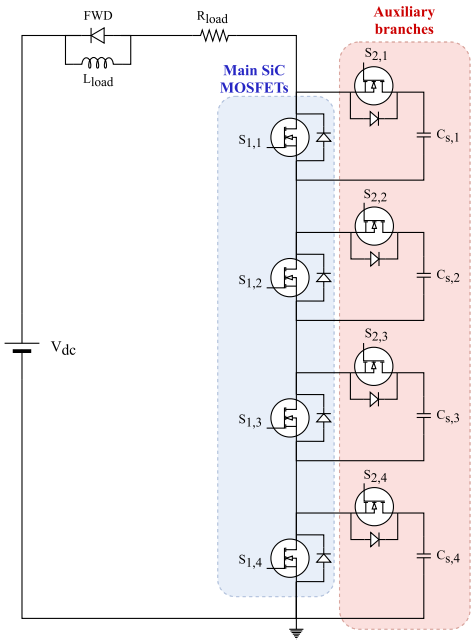


FIGURE 1. Circuit configuration of series connection.

High bandwidth controller is required as well for SiC devices due to the faster switching speed. In this work, a digital signal processor (DSP) is used as a central controller to control the pulsewidth of PWM signals without the analog delay generation circuits. This allows more accurate and faster voltage balancing control with a proposed proportional integral (PI)-control based algorithm. The VBC is validated with up to six series-connected SiC MOSFETs submodules at 150 kHz switching frequency which is much higher than the 1 kHz implementation in [27].

This paper is organized as follows. In Section II, the circuit configuration and principle of the proposed VBC are introduced. Section III presents system and controller design. Simulation studies in MATLAB/Simulink is discussed in Section IV. The hardware circuit implementation and experimental test results are described in Section V. Finally, Conclusion is presented in Section VI.

II. PROPOSED VOLTAGE BALANCING CONTROL

A. CIRCUIT CONFIGURATION

An example test circuit with four series-connected submodules is shown in Fig. 1 to illustrate the operation principle. Each submodule consists of two switches ($S_{1,n}$, $S_{2,n}$) and one shunt capacitor ($C_{s,n}$), where $n = 1, \ldots, N$ and N is the number of series-connected submodules. $S_{2,n}$ and $C_{s,n}$ compose

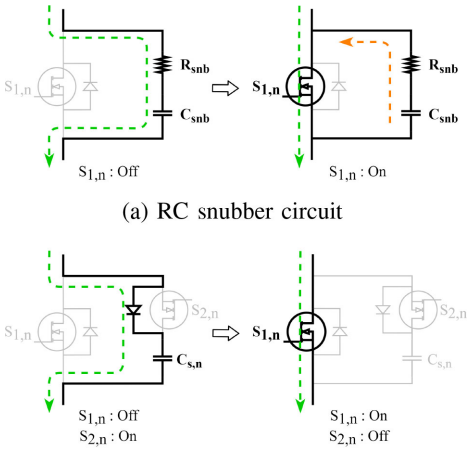


FIGURE 2. Comparison of circuit operation. (a) RC snubber circuit, (b) Submodule.

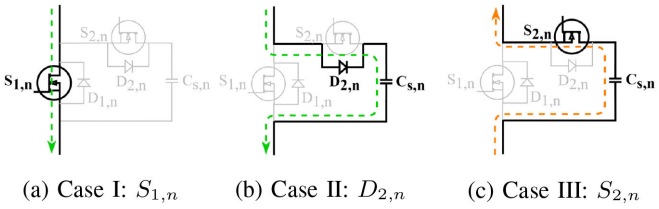


FIGURE 3. Conduction of one submodule in three different cases with current paths. (a) Case I: $S_{1,n}$, (b) Case II: $D_{2,n}$, (c) Case III: $S_{2,n}$.

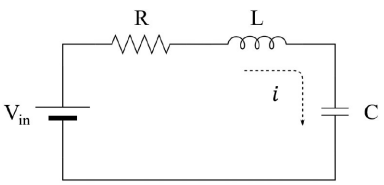


FIGURE 4. Equivalent RLC circuit of the system in the Case II.

an auxiliary branch in the submodule as a low loss snubber circuit.

Fig. 2 shows a comparison of circuit operation in an RC passive snubber circuit and the submodule. In the RC snubber circuit, the snubber capacitor voltage (V_{Csnb}) is charged up to the input voltage (V_{in}) during the turn-off transient of $S_{1,n}$, and the device voltage is $V_{S1,n} = V_{Csnb}$. The charged energy in the snubber capacitor (C_{snb}) is dissipated through the snubber resistor (R_{snb}) during turn-on transient of $S_{1,n}$, and V_{Csnb} becomes zero. This energy dissipation induces considerable loss in the RC snubber circuit. The charging and dissipating processes are repeated every switching cycle. The voltage charging speed during turn-off transient can be described as $dV_{Csnb}/dt = i/C_{snb}$ which means the voltage rising speed of device is $dV_{S1,n}/dt = i/C_{snb}$ as well. Consequently, larger C_{snb} takes longer time to absorb the energy causing slow switching speed of the device with additional switching losses. Typically, a few nano farad (nF) is used as C_{snb}.

Different from the passive RC snubber circuit, the charged energy in $C_{s,n}$ of the proposed submodule is not dissipated. Even though $S_{1,n}$ is turned on, the capacitor energy is saved and not dissipated due to the off state of $S_{2,n}$. Therefore, during the turn-off transient of $S_{1,n}$, the energy stored in $C_{s,n}$ is used again as the initial capacitor voltage ($V_{Cs,n,0}$) of turn-off transient. The shunt capacitor voltage can be expressed as $V_{Cs,n} = V_{Cs,n,0} + \Delta V_{Cs,n}$, where $\Delta V_{Cs,n}$ is the charged voltage by absorbing the additional energy. In the RC snubber circuit, the device voltage rising speed is determined by the capacitor charging speed as $dV_{S1,n}/dt = i/C_{snb}$ since the initial voltage of C_{snb} is zero during turn-off transient of $S_{1,n}$. However, in the proposed method, $V_{Cs,n,0}$ is not zero, and $dV_{S1,n}/dt$ is determined by the intrinsic dynamic characteristic of $S_{1,n}$ device itself until $V_{S1,n}$ reaches $V_{Cs,n,0}$. This allows fast switching speed of device. In this work, $C_{s,n}$ is a few micro farad (μF) which is much larger than typical C_{snb}. Therefore, $\Delta V_{Cs,n}$ is not dramatically changed during transient. The proposed VBC controls $\Delta V_{Cs,n}$ by adjusting pulsewidth of PWM signals, and eventually $V_{Cs,n}$ is balanced which results in voltage balancing of devices.

The conduction of one submodule can be divided into three cases as shown in Fig. 3.

- Case I: This is when $S_{1,n}$ conducts. In this case, the submodule conducts, and the current flows through $S_{1,n}$.
- Case II: This is when the $S_{1,n}$ is off-state, and the body diode ($D_{2,n}$) of $S_{2,n}$ conducts. The submodule becomes an open circuit with a voltage determined by the shunt capacitor ($V_{Cs,n}$). The current flows through $D_{2,n}$ and charges $C_{s,n}$. In this case, the system can be simplified as a series RLC model as shown in Fig. 4, where V_{in} is the system dc voltage, i is the load current, R is the load resistance, L is the load inductance, and C is the shunt capacitance. Capacitor voltage is described by the following equation:

$$V_C(t) = \frac{1}{C}\int i(t)dt, \tag{1}$$

where $i(t)$ can be obtained by solving the following RLC model:

$$\frac{d^2i}{dt^2} + \frac{R}{L}\frac{di}{dt} + \frac{i}{LC} = 0 \tag{2}$$

The solution of eq. (2) can be described as the following equation:

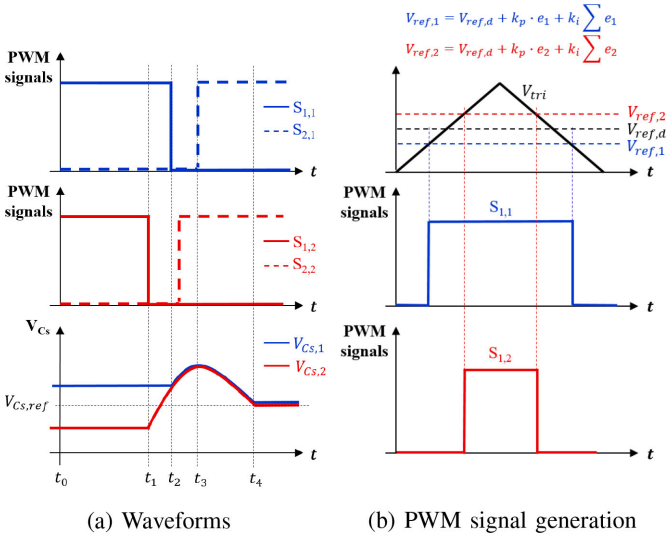
$$i(t) = Ae^{s_1 t} + Be^{s_2 t}, \tag{3}$$

where

$$s_{1,2} = -\frac{R}{2L} \pm \sqrt{\left(\frac{R}{2L}\right)^2 - \frac{1}{LC}} \tag{4}$$

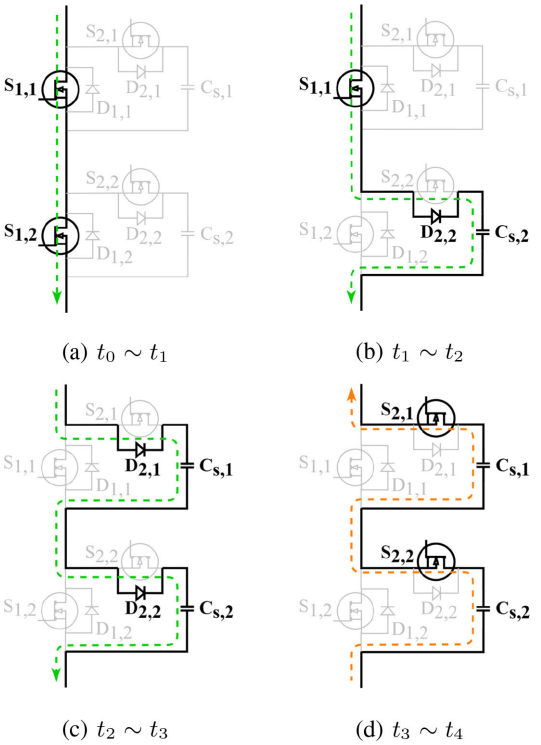
and

$$A = \frac{1}{s_1 - s_2}\left(1 - \frac{s_2}{R}\right)V_{in}, B = \frac{V_{in}}{R} - A. \tag{5}$$



(a) Waveforms (b) PWM signal generation

FIGURE 5. Operation principle of the proposed VBC. (a) Waveforms, (b) PWM signal generation.



(a) $t_0 \sim t_1$ (b) $t_1 \sim t_2$

(c) $t_2 \sim t_3$ (d) $t_3 \sim t_4$

FIGURE 6. Circuit operation of two series-connected submodules. (a) $t_0 \sim t_1$, (b) $t_1 \sim t_2$, (c) $t_2 \sim t_3$, (d) $t_3 \sim t_4$.

With eqs. (2)∼(5), $V_C(t)$ in eq. (1) can be obtained.

- Case III: The energy stored in the capacitor is released back to the source through the $S_{2,n}$. This discharges the capacitor until V_C reaches V_{in}.

B. OPERATION PRINCIPLE

Fig. 5 shows the operation principle of two series-connected submodules which can be expanded to a larger number of series connection. The operation can be divided into four periods, and the corresponding circuit operation of each period is shown in Fig. 6.

- Period $t_0 \sim t_1$: Both submodules represent Case I since the two main switches ($S_{1,1}$, $S_{1,2}$) are on-state. $V_{Cs,2}$ is lower than $V_{Cs,ref}$, where $V_{Cs,ref} = V_{dc}/N$ is the reference of balanced capacitor voltage. To achieve voltage balancing, $V_{Cs,2}$ needs to be increased by charging $C_{s,2}$.
- Period $t_1 \sim t_2$: In order to charge $C_{s,2}$, $S_{1,2}$ is turned off at t_1 while $S_{1,1}$ remains on-state until t_2. The second submodule turns into Case II, and $C_{s,2}$ gets charged by a positive current through $D_{2,2}$.
- Period $t_2 \sim t_3$: This period is a dead-band of the two switches in the first submodule. Since both $S_{1,1}$ and $S_{2,1}$ are off-state, $D_{2,1}$ conducts, and the first submodule is converted to Case II. Regardless of the status of $S_{2,2}$, the second submodule remains in Case II with $D_{2,2}$ conducting due to the turn-off state of $S_{1,2}$. The two shunt capacitors are charged until the $S_{2,1}$ is turned on. However, this period is a dead-band which is typically a very short period. Therefore, the amount of voltage variation is negligible in this period.
- Period $t_3 \sim t_4$: The $S_{2,1}$ is turned on at t_3. The two submodules represent Case III since both auxiliary switches ($S_{2,1}$, $S_{2,2}$) are on-state. The stored energy in the capacitors is released back to the voltage source through the auxiliary switches. This energy is discharged until the sum of the capacitor voltages is equal to the source voltage. Consequently, the distribution of voltages among the switches is balanced.

As discussed above, $S_{1,2}$ is turned off keeping $S_{1,1}$ on-state to charge $C_{s,2}$ for voltage balancing. This can be done by controlling the voltage references of the PWM signals ($V_{ref,n}$). According to Fig. 5(b), a triangular carrier (V_{tri}) is shared by all the submodules, and $V_{ref,n}$ is adjusted using PI-controller as shown in the following equation:

$$V_{ref,n} = V_{ref,d} + k_p \cdot e_n + k_i \sum e_n, \tag{6}$$

where $V_{ref,d}$ is an initially defined reference signal for a desired duty ratio, k_p is the proportional gain, k_i is the integral gain, and e_n is the error ($e_n = V_{Cs,ref} - V_{Cs,n}$). Given that $V_{Cs,1}$ is higher than $V_{Cs,ref}$ in Fig. 5, the reference signal of the first module ($V_{ref,1}$) becomes negatively shifted. Alternatively, $V_{ref,2}$ is positively shifted since $V_{Cs,2}$ is lower than $V_{Cs,ref}$. This procedure results in adjusted pulsewidths and increases $V_{Cs,2}$ for voltage balancing.

III. CONTROLLER AND SYSTEM DESIGN

A. CONTROLLER DESIGN

Fig. 7 illustrates the closed-loop controller diagram of one submodule with $V_{Cs,n}$ feedback signal. The feedback signal is isolated by an isolation amplifier (AMC1311) and converted

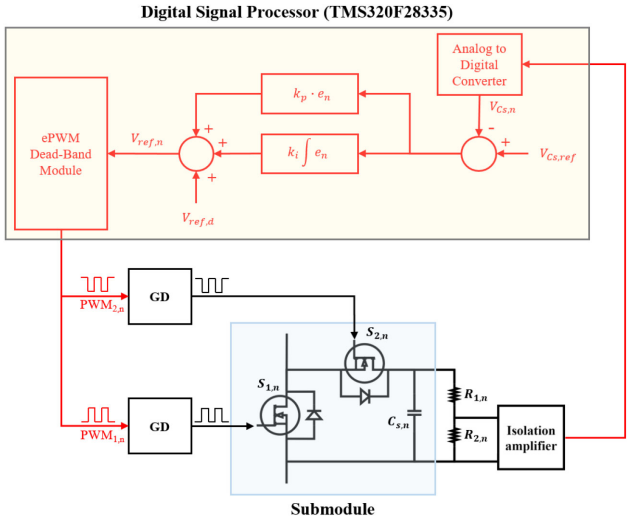


FIGURE 7. Schematic diagram of the proposed VBC for one SiC MOSFET submodule.

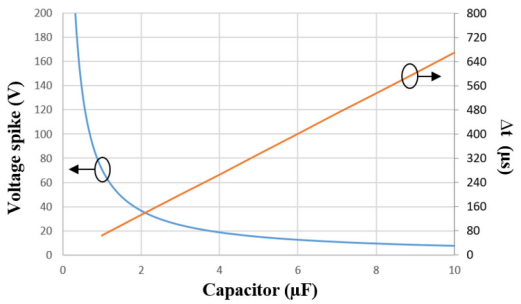


FIGURE 8. Shunt capacitor selection considering voltage spike and Δt.

to a digital signal in DSP. $V_{Cs,n}$ is compared with $V_{Cs,ref}$ to calculate e_n which is used in the proposed PI-controller to determine the amount of shift from $V_{ref,d}$. As a result, the adjusted $V_{ref,n}$ is calculated using eq. (6). The calculated $V_{ref,n}$ is used in ePWM Dead-Band Module to generate two complementary PWM signals ($PWM_{1,n}$, $PWM_{2,n}$) with a dead time to avoid a short circuit.

B. SIZING OF SHUNT CAPACITOR AND AUXILIARY SWITCH CONSIDERATION

Sizing of the shunt capacitor is a tradeoff between voltage overshoot and voltage balancing time. The voltage overshoot during transient can be obtained from the equivalent RLC circuit shown in Fig. 4. The RLC model can be described as the following equation:

$$\frac{V_{in}}{LC} = \frac{d^2V_C}{dt^2} + \frac{R}{L}\frac{dV_C}{dt} + \frac{1}{LC}V_C. \tag{7}$$

The transient solution of eq. (7) can be expressed with the given initial conditions, $i(0) = V_{in}/R$ and $V_C(0) = V_{in}$, as the following equation:

$$V_{C,t}(t) = Ce^{s_3 t} + De^{s_4 t}, \tag{8}$$

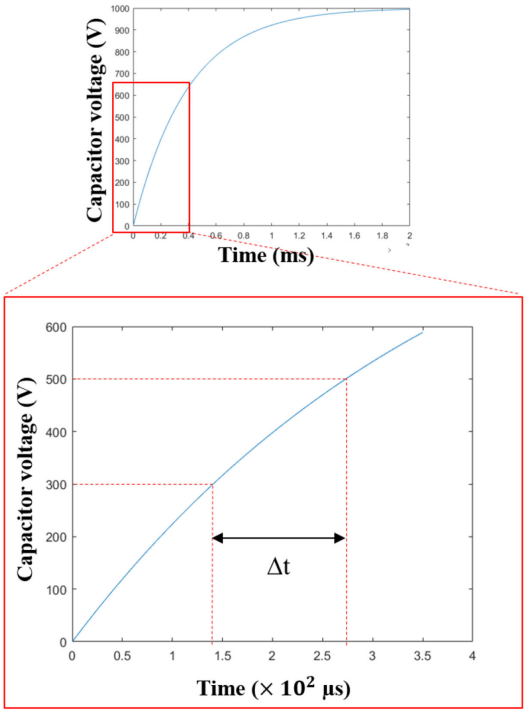


FIGURE 9. Shunt capacitor charging voltage.

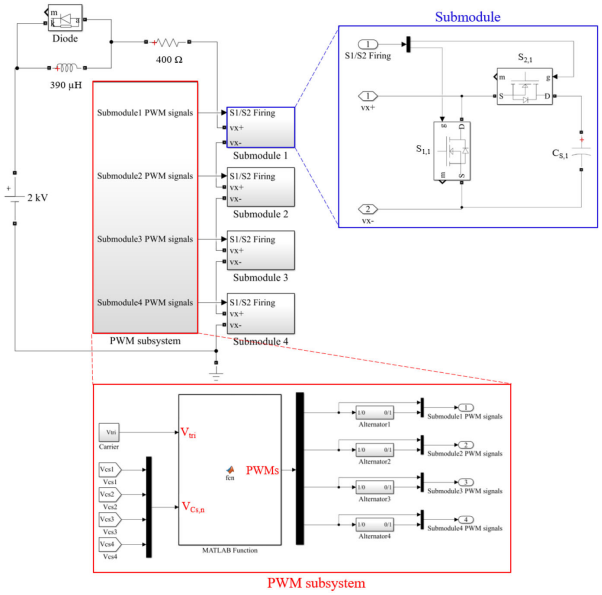


FIGURE 10. MATLAB/Simulink model for four series-connected submodules.

where

$$s_{3,4} = -\frac{R}{2L} \pm \sqrt{\left(\frac{R}{2L}\right)^2 - \frac{1}{LC}} \tag{9}$$

and

$$C = \frac{V_{in}}{RC}\left(\frac{1}{s_3 - s_4}\right), D = \frac{V_{in}}{RC}\left(\frac{1}{s_4 - s_3}\right). \tag{10}$$

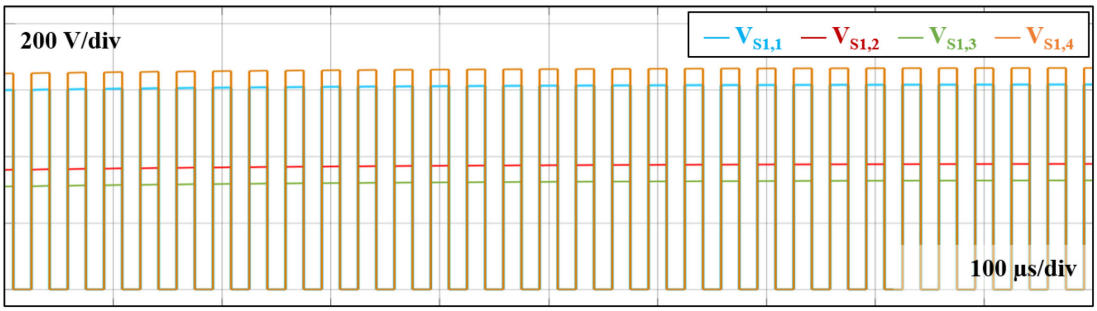


FIGURE 11. Simulated unbalanced voltages of four series-connected submodules without the VBC at 2 kV.

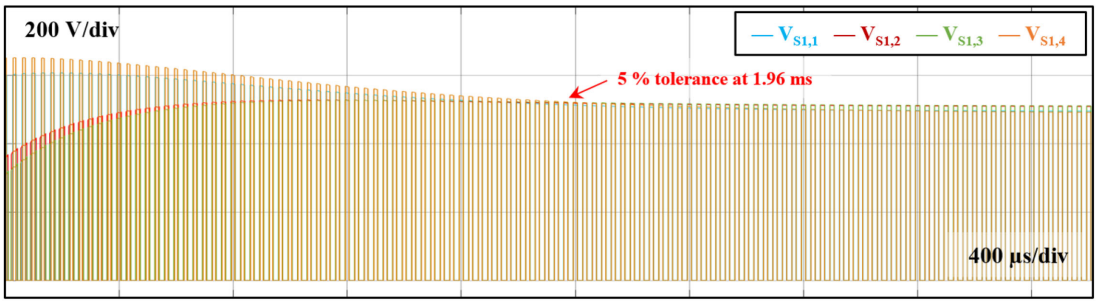


FIGURE 12. Simulated balanced voltages of four series-connected submodules with the proposed VBC at 2 kV.

The maximum value of eq. (8) is the maximum voltage spike of the capacitor. The relationship between the voltage spike and shunt capacitor is plotted as the blue curve in Fig. 8.

To investigate the relationship between voltage balancing time and shunt capacitance, eq. (1) is used. Fig. 9 shows the plot of eq. (1), where the capacitor is 2 μF, the targeted balanced voltage (V_{bal}) is set as 500 V, and the initial unbalance (V_{unbal}) is designed as 300 V. By using eq. (1), the required charging time (Δt) to reach V_{bal} can be calculated and is closely related to the voltage balancing time. By plotting the voltage overshoot and Δt as a function of shunt capacitance in Fig. 8, 2 μF was selected in this study. Capacitance value can be adjusted based on voltage overshoot and balancing time requirements for specific applications.

The auxiliary switch needs to withstand the same dc voltage as the main switch. For continuous drain current, load current mainly goes through the main switch while shunt capacitor charging current and discharging current go through the auxiliary snubber switch with much smaller amplitude. Detailed waveforms will be discussed in Section V. During turn-off transient of the main switch, a part of load current flows to the auxiliary branch through the body diode of the auxiliary switch. Therefore, there is a short pulse current through the auxiliary switch with a peak amplitude close to the load current during the turn-on transient of auxiliary switch. Although in this study the same device rating was used for main and auxiliary switches, the auxiliary switch current rating has a potential to be reduced by half considering that pulse current rating can be 2-3 times continuous current rating [32].

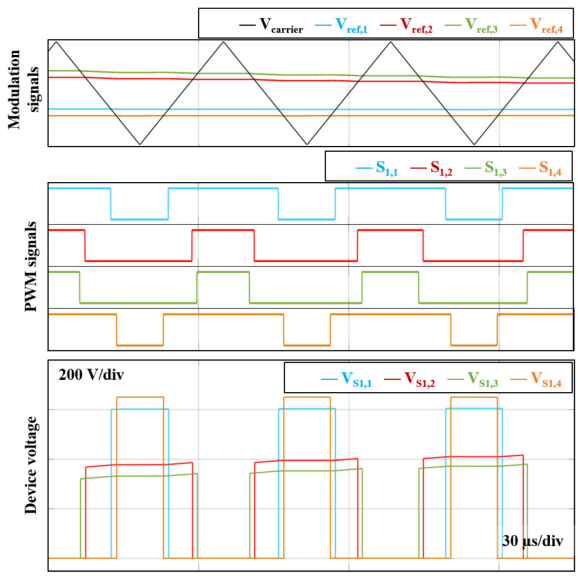


FIGURE 13. Simulated results of PWM signals and device voltages for the first three switching cycles at 2 kV.

IV. SIMULATION STUDY

A. FOUR SERIES-CONNECTED SUBMODULES

The proposed VBC is designed and simulated in MATLAB/Simulink as shown in Fig. 10. The system parameters are $V_{dc} = 2\ kV$, $L_{load} = 390\ \mu H$, $R_{load} = 400\ \Omega$, $C_{s,n} = 2\ \mu F$, and $f_{sw} = 30\ kHz$, where V_{dc} is the system dc voltage, L_{load} is the load inductance, R_{load} is the load resistance, and

- a: a_{th} switching cycle
- $V_{c,n,a}$: capacitor voltage of n_{th}submodule at a_{th}switching cycle
- $V_{ref,n,a}$: adjusted reference voltage of PWM signals at a_{th}switching cycle
- $\Delta t_{n,a}$: the pulse width difference between submodule
- $\Delta V_{c,n,a}$: charged voltage during $\Delta t_{n,a}$
- $t_{balancing}$: time to achieve voltage balancing

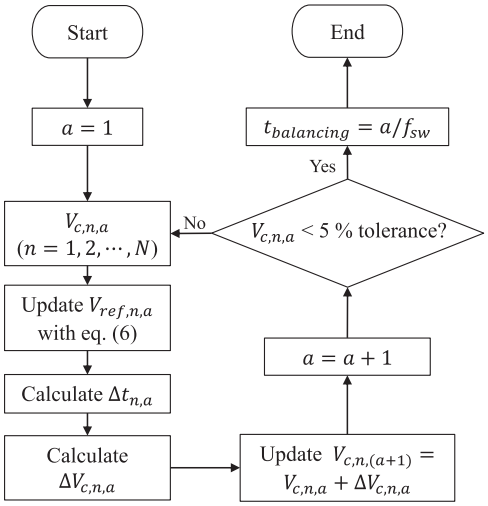


FIGURE 14. Flowchart for theoretical voltage balancing time analysis.

f_{sw} is the switching frequency. The PWM subsystem is designed to generate PWM signals for each submodule. $V_{Cs,n}$ is used as input to generate the adjusted PWM references $V_{ref,n}$ using eq. (6). The PWM signals distributed to each submodule are generated by using the adjusted $V_{ref,n}$ and carrier V_{tri}.

The model is initially simulated without the VBC to study the influence of the controller on voltage balancing. The unbalanced voltages are preset shunt capacitor initial voltages ($V_{Cs,1} = 610\ V$, $V_{Cs,2} = 385\ V$, $V_{Cs,3} = 330\ V$, and $V_{Cs,4} = 675\ V$), which are the same values in experiments.

$V_{S1,n}$, which represents $V_{Cs,n}$ during off-state of $S_{1,n}$, is measured, and the unbalanced voltages are observed in Fig. 11. The proposed VBC with PI-controller is simulated, and voltage balancing is achieved as shown in Fig. 12. The voltage waveforms of the first three switching cycles are presented in Fig. 13 to illustrate the effect of the proposed VBC on voltage balancing. The VBC adjusts the pulsewidths of the PWM signals for $V_{S1,n}$ balancing. $V_{S1,2}$ and $V_{S1,3}$ are lower than the desired balanced voltage and need to be increased. $V_{ref,2}$ and $V_{ref,3}$ are then increased for voltage balancing based on eq. (6). This results in smaller pulsewidths of the gate pulses and longer turn-off duration of $S_{1,2}$ and $S_{1,3}$ to increase $V_{S1,2}$ and $V_{S1,3}$. In the meantime, $V_{ref,1}$ and $V_{ref,4}$ are decreased, and shorter turn-off duration are observed in $V_{S1,1}$ and $V_{S1,4}$ waveforms.

B. VOLTAGE BALANCING TIME COMPARISON

For theoretical analysis of balancing time, the Δt calculation process mentioned in Section III is used. With the adjusted

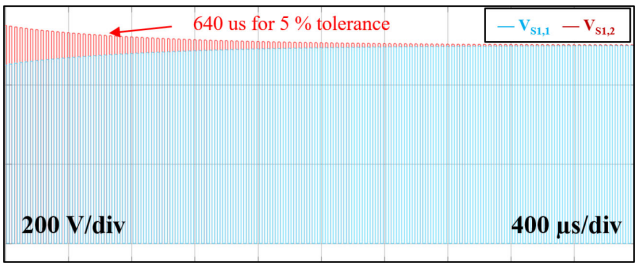


FIGURE 15. MATLAB/Simulation results of two series-connected submodules at 1 kV.

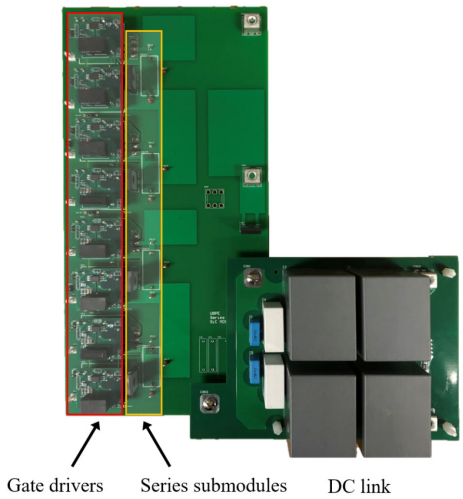


FIGURE 16. Hardware test board.

TABLE 1. Circuit Parameters for Three Different Test Scenarios

Parameters	Scenario I	Scenario II	Scenario III
Device (SiC MOSFET)	SCT3120AL	SCT3120AL	C2M0280120D
System voltage (V_{dc})	2 kV	1 kV	3 kV
Load current (I_{load})	5 A	17 A	3.25 A

$V_{ref,n}$, the duty ratio of each submodule can be calculated, and then the pulsewidth difference between the two main switches can be obtained. The pulsewidth difference is the charging time of the current switching cycle. Since the charging time is a known value, the amount of charged voltage can be calculated using eq. (1). Then the unbalance voltages are updated with the calculated charged voltage. With the updated unbalanced voltages, $V_{ref,n}$ can be calculated again and the above-mentioned process keeps updating the unbalanced voltage. Eventually, balanced voltage is reached, and the voltage balancing time can be calculated by counting the number of iterations. This is the same as the number of switching cycles required for voltage balancing. With known switching

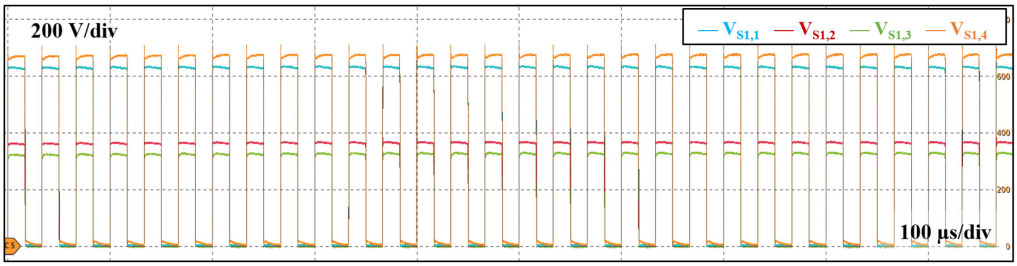


FIGURE 17. Unbalanced voltages of SCT3120AL SiC MOSFETs without the VBC at 2 kV.

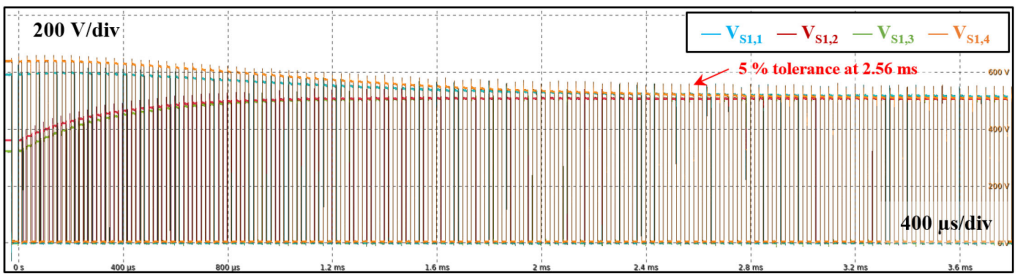


FIGURE 18. Balanced voltages of SCT3120AL SiC MOSFETs with P-controller at 2 kV.

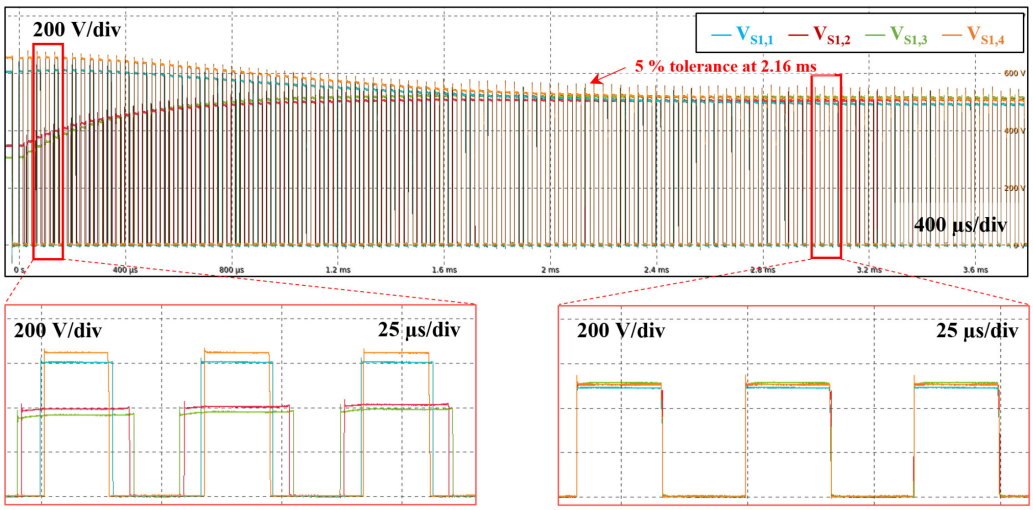


FIGURE 19. Balanced voltages of SCT3120AL SiC MOSFETs with the proposed VBC using PI-controller at 2 kV.

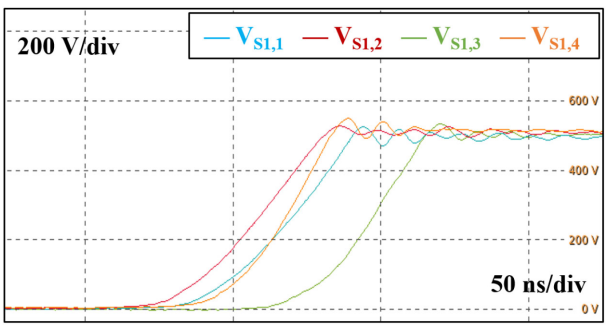


FIGURE 20. Dynamic voltage sharing of SCT3120AL SiC MOSFETs at 2 kV.

frequency and the number of switching cycles, the theoretical voltage balancing time can be estimated.

The aforementioned process is summarized in the flowchart in Fig. 14. With the given initial condition of capacitor voltages ($V_{c,n,1}$), the theoretical voltage balancing time can be calculated as $\frac{a}{f_{sw}}$, where a is the calculated number of iterations/switching cycles needed to reach voltage balance, and f_{sw} is the switching frequency. Two series-connected submodules at 1 kV are considered for voltage balancing time comparison study.

Following the above procedure, theoretical voltage balancing time is calculated as 633.3 μs, which is very close to

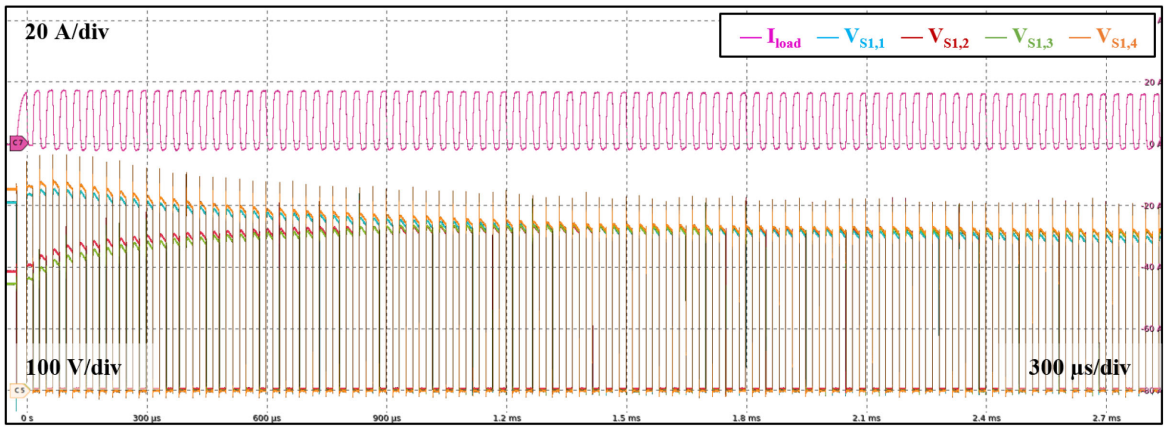


FIGURE 21. Balanced voltages of SCT3120AL SiC MOSFETs with the proposed VBC using PI-controller at 1 kV, 17 A.

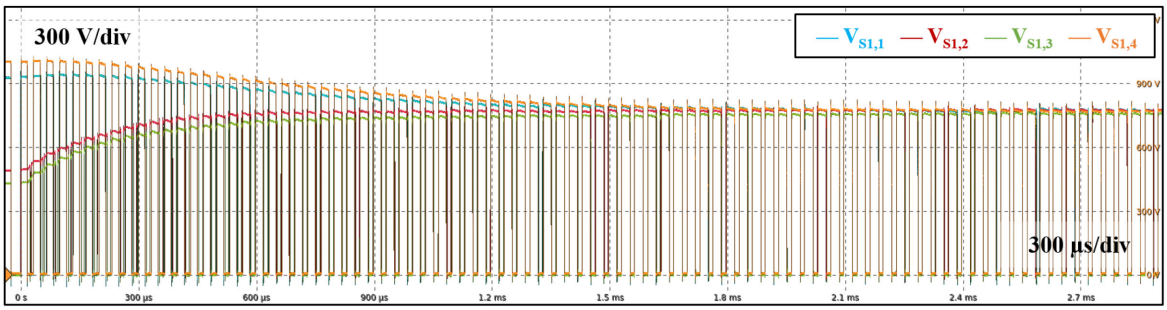


FIGURE 22. Balanced voltages of C2M0280120D SiC MOSFETs with the proposed VBC using PI-controller at 3 kV.

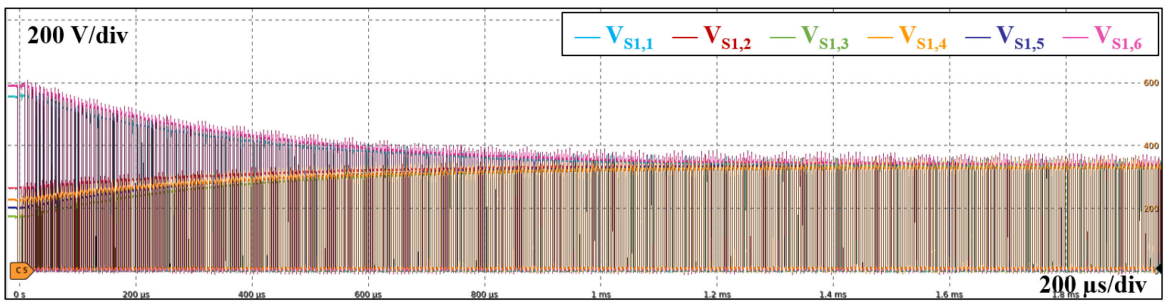


FIGURE 23. Balanced voltages of six series-connected SCT3120AL SiC MOSFETs with the proposed VBC using PI-controller at 2 kV, 150 kHz.

the 640 μs balancing time from simulation shown in Fig. 15. Experimental results showed a 750 μs balancing time, which is still in good agreement with the theoretical and simulation. Details on experimental balancing time are presented in Section V.

V. EXPERIMENTAL VERIFICATION

A. TEST SETUP

The circuit configuration of Fig. 1 is implemented in hardware as shown in Fig. 16. A TI TMS320F28335 DSP, which operates at 150 MHz with 32-bit CPU, is used in this work and provides a 12-bit resolution of the analog to digital converter. Device voltages are measured with THDP0200 200 MHz high voltage differential probes, and TCP0030 A 120 MHz current probes are used for measuring currents. Two different MOSFETs are adopted for this test: a Rohm semiconductor SiC MOSFET (SCT3120AL, 650 V, 21 A) [32] and a CREE SiC MOSFET (C2M0280120D, 1.2 kV, 10 A) [33]. They are tested in three different test scenarios as listed in Table 1. Scenario I is to study the VBC at 2 kV which is 76.9% of blocking voltage of four series-connected SCT3120AL devices. Scenario II is for higher current test condition which is in a case when the system current is 81% of the SCT3120AL device current rating, and Scenario III is to test the proposed VBC at a higher

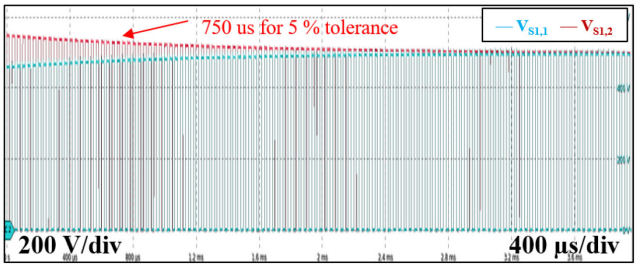
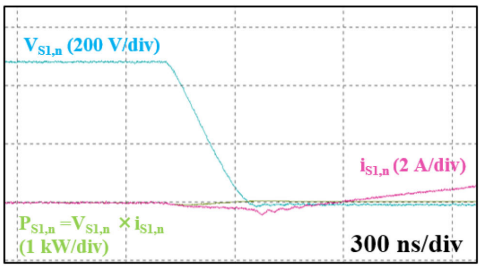
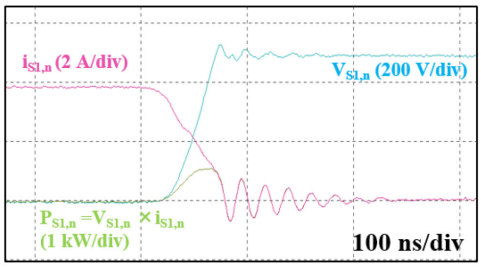


FIGURE 24. Experimental results of two series-connected submodules at 1 kV.



(a) Turn-on transient



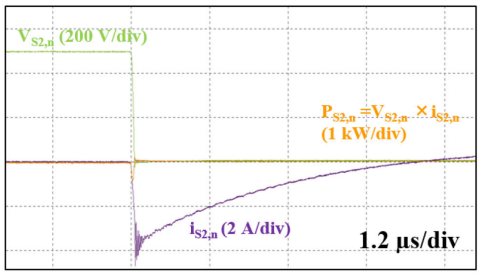
(b) Turn-off transient

FIGURE 25. Transient waveforms of main switch.

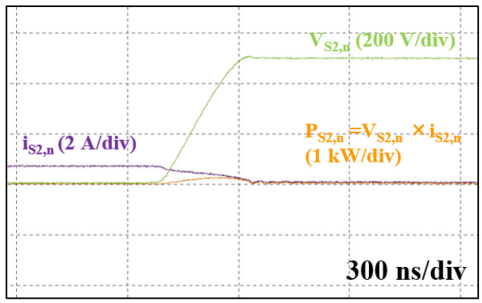
dc voltage with C2M0280120D devices. 2 μF of $C_{c,n}$ is used for all experimental tests.

B. EXPERIMENTAL RESULTS

Experimental results of Scenario I are shown in Figs. 17–21. Fig. 17 shows the unbalanced voltages of $S_{1,n}$ at 2 kV without VBC. To study the performance of the PI-controller, voltage balancing time is measured and compared with that of P-controller when all the voltages are within 5% of the targeted balanced voltage. With the P-controller, voltage balancing is achieved in 2.56 ms as shown in Fig. 18. For the proposed VBC with PI-controller, voltage balancing is achieved in 2.16 ms which is 15% faster than the P-controller as shown in Fig. 19. The experimental result of 2.16 ms is 0.2 ms longer voltage balancing time than simulation study in Fig. 13. All $V_{S1,n}$ is within 2.2% of the targeted balanced voltage which is 500 V. Specifically, $V_{S1,1}$, $V_{S1,2}$, $V_{S1,3}$, and $V_{S1,4}$ have percentage errors of 2.2% (489 V on average), 0.6% (503 V on average), 0.4% (502 V on average), and 1.2% (506 V on average), respectively.



(a) Turn-on transient



(b) Turn-off transient

FIGURE 26. Transient waveforms of auxiliary switch.

Fig. 19 shows that different devices have different pulsewidths for voltage balancing as with simulation results in Fig. 13. Since $V_{S1,2}$ and $V_{S1,3}$ have to be increased for voltage balancing, the pulsewidths of the $S_{1,2}$ and $S_{1,3}$ PWM signals are decreased. Therefore, pulsewidths of $V_{S1,2}$ and $V_{S1,3}$ are increased, which results in charging of the capacitors. Alternatively, the pulsewidths of $S_{1,1}$ and $S_{1,4}$ PWM signals are increased to reduce $V_{S1,1}$ and $V_{S1,4}$. When the voltages are unbalanced, the pulsewidth of each PWM signal is controlled to charge or discharge capacitors. According to Fig. 19, when voltage balancing is achieved, the duty ratio of each device is the same as a predefined value depending on $V_{ref,d}$ which is 50% duty ratio in this test. Dynamic voltage sharing of devices is shown in Fig. 20. A voltage rise time (t_{rise}) of 40.5 ns is measured as an average value of the four devices.

To validate the VBC at a higher current condition, Scenario II is tested as shown in Fig. 21. It is observed that voltage balancing is achieved as well at 17 A which is 81% of the device current rating. The targeted balanced voltage per device is 250 V in Scenario II, and the maximum average percent error is 1.6% ($V_{S1,3}$ equal to 246 V).

A CREE SiC MOSFET (C2M0280120D, 1.2 kV, 10 A) is adopted to study the VBC at higher dc voltage. In Scenario III, 3 kV is tested with 750 V of targeted balanced voltage per device. The VBC is verified at 3 kV with 3.9% of the maximum average percent error ($V_{S1,3}$ equal to 721 V) as shown in Fig. 22.

As a result, the proposed VBC is experimentally validated at not only 76.9% of device blocking voltage, but also 81% of device current rating. It is verified at 3 kV system voltage as well, and accurate voltage balancing within 3.9% of the

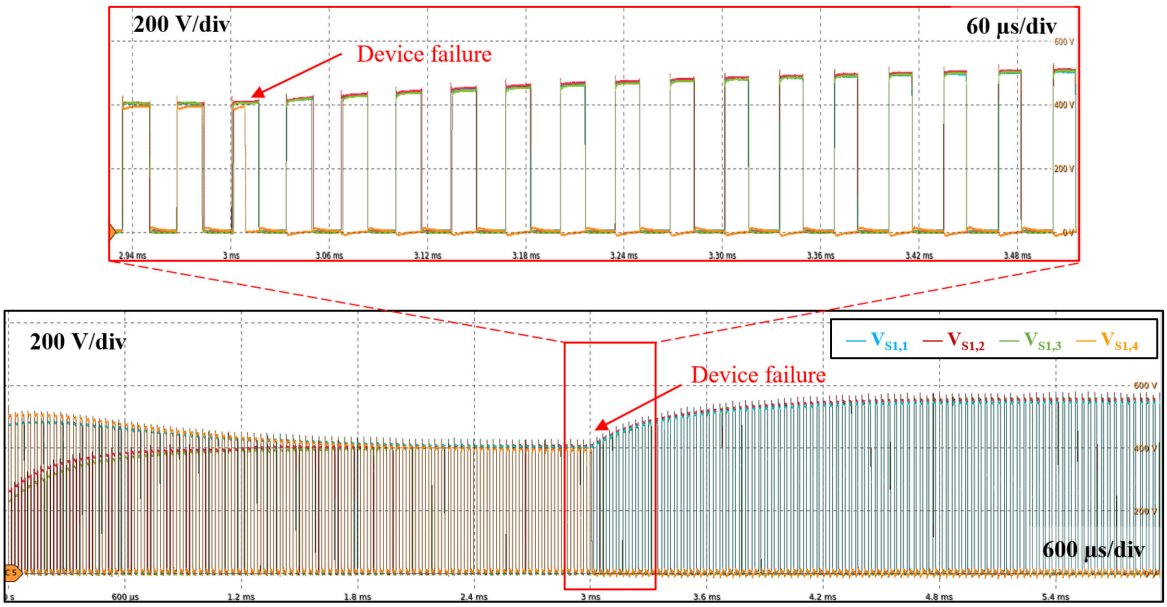


FIGURE 27. Voltage balancing with one device failure at balanced voltage condition.

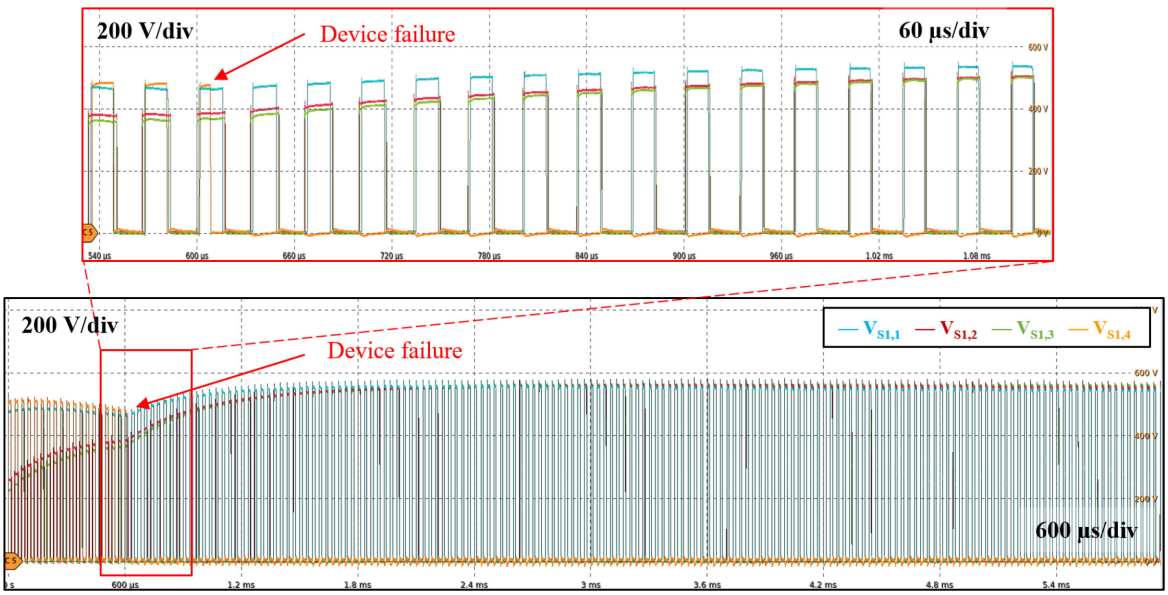


FIGURE 28. Voltage balancing with one device failure at unbalanced voltage condition.

targeted balanced voltage is achieved in all three different scenarios. Lastly, the proposed VBC is validated with six series-connected submodules at the highest 150 kHz switching frequency as shown in Fig. 23.

The proposed method requires isolated auxiliary power converter for each gate driver, which can be considered a drawback. It also requires several switching cycles to achieve voltage balancing if the initial imbalance exists. However, the proposed method offers many advantages compared with other existing methods, especially in the aspects of switching speed, switching frequency, the number of series-connected devices, and the accuracy of voltage balancing, which can be a preferred option for many applications.

C. BALANCING TIME AND SWITCHING LOSS ANALYSIS

For the voltage balancing time comparison between theoretical analysis, simulation, and experiment, two series-connected submodules are tested at 1 kV as shown in Fig. 24. The experimental results shows 750 μs voltage balancing time which is 110 μs difference form simulation study in Fig. 15. This translates to only 3.3 switching cycle differences (3.3 =

110 $\mu s \times 30\ kHz$) which can be considered as good agreement with theoretical analysis and simulation.

Switching transients of $S_{1,n}$ are shown in Fig. 25 when the voltages are balanced at 500 V with 3.95 A. During the turn-on transient of $S_{1,n}$, a negative current spike is measured and the current gradually increases. When $S_{1,n}$ is turned on, the RL load current starts to flow through $S_{1,n}$. Therefore, the drain current of $S_{1,n}$ ($i_{S1,n}$) gradually increases even though $S_{1,n}$ is fully turned on. The negative current flows through the body diode and induces loss that can be estimated as follows: $\frac{1}{2}V_{fvd}I_{peak}\Delta t_r = \frac{1}{2} \times 3.2\ V \times 0.44\ A \times 520\ ns = 0.37\ \mu J$, where V_{fvd} is the forward voltage of body diode obtained from datasheet. I_{peak} is the absolute value of the peak current, Δt_r is the time duration of the negative current. Since no positive current flows through drain to source of $S_{1,n}$, there is no turn-on switching loss energy in $S_{1,n}$. The turn-off transient is shown in Fig. 25 (b) and turn-off switching energy loss is calculated as 23.3 μJ using the following equation: $E_{off} = \int V_{ds}(t)i_{ds}(t)dt$. Finally, the total switching energy loss of $S_{1,n}$ is 23.67 μJ.

Fig. 26 shows the transient waveforms of auxiliary switch ($S_{2,n}$). During the turn-on transient of $S_{2,n}$, a negative current is observed which is the capacitor charging current through body diode of $S_{2,n}$. It causes the loss of body diode which can be estimated as follows: $\frac{1}{2} \times 3.2\ V \times 4.1\ A \times 4.4\ \mu s = 28.9\ \mu J$. The turn-off switching energy loss is calculated as 23.6 μJ. Therefore, the total switching energy loss of $S_{2,n}$ can be obtained as 52.5 μJ which is the energy loss of auxiliary branch.

The loss of RC snubber circuit is the dissipated energy of C_{snb}. To calculate the energy loss of RC snubber circuit, 10 nF is selected based on the snubber circuit study for SiC MOSFETs [11]. The energy loss of RC snubber circuit can be calculated as follows: $E_{Csnb,loss} = \frac{1}{2}C_{snb}V^2 = \frac{1}{2} \times 10\ nF \times (500\ V)^2 = 1250\ \mu J$. It is shown that the proposed auxiliary branch has much smaller energy loss of 52.5 μJ which is 4.2% of the RC snubber energy loss.

D. VOLTAGE BALANCING TEST WITH DEVICE FAILURE

Assuming a device fails during operation and creates a shorted path meaning the device is always conducting, dc source voltage will be applied to the other three normal devices. Also assume that the device voltage rating has sufficient margin to handle the increased voltage stress. For the circuit to function until it can be safely shut down, voltage balancing is required among the remaining functioning devices. Tests were conducted to verify the voltage balancing performance when one of four series devices failed at 1.6 kV dc source voltage. Two different scenarios were considered depending on whether the original voltage balancing had been achieved or not when the device failed. Fig. 27 shows the first case which demonstrates that voltage balancing was maintained after one device failed. The voltages were evenly distributed to the other three devices and reached the balanced voltage at 533.3 $V = \frac{1.6\ kV}{3}$. Fig. 28 demonstrates that the proposed VBC method was capable of gaining voltage balance even if one device failed while the voltages were still unbalanced.

VI. CONCLUSION

A VBC with PWM method was proposed for series-connected SiC MOSFET submodules. The VBC adjusted the reference voltages of the PWM signals to control the capacitor voltages actively for balancing. DSP was used as a central controller, and it directly controlled the PWM signals without additional analog control circuits. The proposed VBC was simulated in MATLAB/Simulink and was experimentally validated with four series-connected SiC MOSFET submodules. Two different SiC MOSFETs (SCT3120AL, C2M0280120D) were adopted to test the VBC at three different test scenarios. SCT3120AL SiC MOSFETs were tested in Scenario I and II, in which the system voltage was 76.9% of device blocking voltage and the system current was 81% of device current rating, respectively. To test the proposed VBC at higher voltage level, C2M0280120D SiC MOSFETs were tested at 3 kV in Scenario III. It was shown that the proposed VBC achieved an accurate voltage balancing at all three scenarios within 3.9% tolerance without sacrificing the switching speed of SiC MOSFETs.

The proposed VBC was validated as well with six series-connected submodules at 150 kHz. The energy loss of auxiliary branch was shown to be much smaller than passive RC snubber circuit. Moreover, a case study with one of the series-connected devices suddenly failing and creating a short path demonstrated that the proposed method was capable of gaining voltage balance even if one device failed.

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