A gentle parasitic growth removal process to enable low temperature magneto-transport characterization in confined epitaxial lateral growth of InGaAs

Aranya Goswami[1], Brian Markman[1], Simone T. Šuran Brunelli[1], Shouvik Chatterjee[1], Jonathan Klamkin[1], Mark Rodwell[1], Chris J. Palmstrøm[1,2]*

[1] *Electrical and Computer Engineering Department, University of California Santa Barbara, Santa Barbara, CA 93106, U.S.A.*

[2] *Materials Department, University of California Santa Barbara, Santa Barbara, CA 93106, U.S.A.*

***** *Correspondence to: cjpalm@ucsb.edu*

Abstract:

Template assisted selective area growth techniques have gained popularity recently for their ability to grow epitaxial materials in geometries defined by prefabricated dielectric templates. Such dielectric templates can be used to grow nanostructured devices, eliminating the need for post-processing, thus avoiding material damage induced by various etching processes. However, parasitic growth on the dielectric mask, sometimes much larger than the grown nanostructures, provide significant hurdles to etching vias and making contacts and electrostatic gates to these nanostructures. Here, we demonstrate a novel process flow to etch off the parasitic growths without affecting the nanostructures in $In_{0.53}Ga_{0.47}As$ confined epitaxial lateral overgrowth (CELO) samples with heavy parasitic growth. Thereafter, successful fabrication of ohmic contacts on these nanostructures with precise alignments is demonstrated. Shubnikov-de Hass oscillations observed in low temperature magnetotransport measurements are analyzed to estimate effective mass, carrier density and mobilities in doped InGaAs CELO structures.

Semiconductor nanostructures have attracted interest in recent years for their novel electronic[1] and optical properties[2]. Quantum confinement effects, which dominate in the sub-micron length scales of the nanostructures, have potential applications in diverse fields such as quantum computing[3–5], high speed transistors[6–11], spintronics[3,12,13] and on-chip integrated photonic circuits[14–16]. It is essential to fabricate high-quality nanostructures with custom geometries and integrate them on a wide range of substrates for optimal performance of such quantum devices. To this end, confined epitaxial lateral overgrowth (CELO) has

emerged as one of the most promising techniques for growing defect-free nanostructures on lattice mismatched substrates[17,18]. CELO is a bottom-up template-assisted growth method that uses epitaxial selective area growth on substrates with prefabricated dielectric templates. Selective area growth restricts nucleation of precursors to the dielectric-free areas of the substrate[19]. The templates act as defect filters using aspect ratio trapping and thereafter confine the growth and its direction on the substrate. CELO thus allows the growth of nanostructures in pre-determined custom geometries and orientations, eliminating the need for post-growth processing. Channel dimensions can be scaled down to tens of nanometers, without the challenges of dry-etch induced defects, which are common for top-down fabrication routes. As a result, CELO has the potential to fabricate high quality photonic lasers[14], transistors[20] and devices to study quantum transport in low-dimensional nanostructures[21,22].

Despite its benefits, CELO growths often exhibit unwanted III-V nucleations (Fig. 1A) on the dielectric mask, also known as parasitic growth[23]. Growing CELO nanostructures with no parasitic nucleations is challenging and often requires constraining the growth parameters within a narrow window. However, the growth conditions required for achieving high quality growths might often fall outside this narrow set of conditions required for perfect selectivity. Parasitic growths affect the growth rates of the nanostructures inside the CELO templates by acting as a nucleation sink. Epitaxial growths of a few hundred nanometers inside the CELO templates often result in parasitic nucleations that are tens of microns in size[24]. Further, clear and precise alignment marks are essential for device processing requiring sub-micron alignments. Preferential nucleation of parasitic growths on rough edges of the patterned dielectric often cover these alignment marks completely. This renders alignment, along with further processing of CELO structures nearly impossible. In addition, due to the rough oxide topography resulting from nucleations, there is a high failure rate in forming metal contacts to the nanostructures. Hence, a process for preferential removal of parasitic growths would allow a much larger growth window for optimization to be explored and still allow for device processing.

Because parasitic growths impede CELO device fabrication, they inherently limit characterization of materials grown using this technique. This is problematic because material properties in nanostructures often deviate significantly from those of planar epitaxial structures grown under similar conditions[25–27]. For example, depending on growth conditions, CELO-grown III-V materials exhibit variations in defect densities[28] , spatial gradients in ternary compositions and facet specific group-III incorporations[29,30]. As a result, electrically characterizing CELO nanostructures is crucial for both understanding material qualities and optimizing growth conditions. Therefore, removal of parasitic growths can enable reliable fabrication of device structures for electrical characterization of CELO nanostructures.

Removal of parasitic growths post growth is however nontrivial. A conventional wet etch does not preferentially remove parasitic growths, because it will also etch the devices. Likewise, highly anisotropic plasma-based dry etches can result in significant damage to the sample active region (Fig 2). In this letter, we demonstrate a rapid, yet gentle multi-step etch process, which removes the parasitic growths while leaving the growths inside the template undisturbed. Here, we combine dry and wet etching, while using a conformal oxide as a protective layer for the nanostructures. This etch process produces CELO samples with a smooth surface topography and restores usability of alignment marks previously covered with parasitic growths. This process flow is generalizable to any CELO-grown materials for which a reliable wet etch is known.

With the successful removal of parasitic growths, it is now possible to fabricate devices to extract material parameters through electrical measurements. In this study, we explore the technologically relevant InGaAs system. This material's high electron mobility and direct bandgap makes it attractive for a wide range of electronic and photonic applications, especially for telecommunications, high frequency electronics and topological quantum computing. Electrical transport measurements at low temperatures can allow us to extract parameters important for the use of InGaAs in semiconductor nanowire networks for Majorana fermions[31], spin field effect transistors [32–34], high-performance nanoelectronics[35], terahertz detectors[36] or optoelectronic devices[37]. Here, we demonstrate fabrication of ohmic contacts and perform low temperature magneto-transport on InGaAs CELO samples free of parasitic growths. From the observed Shubnikov de Haas (SdH) oscillations, we extract doping concentration, effective mass and quantum mobility in these nanostructures. These measurements clearly reveal variability in growth and material qualities. Thus, the use of our etching process flow allows one to grow a wider range of III-V materials and their heterostructures using the CELO geometry, optimize the material quality, and fabricate electronic and photonic devices with greater control.

CELO templates were fabricated by depositing a 5 nm Al_2O_3 etch stop layer using atomic layer deposition and a 20 nm bottom dielectric SiO_2 via plasma-enhanced chemical vapor deposition (PECVD). Seeds were lithographically defined, and a 50 nm sacrificial chemically semi-amplified positive electron-beam resist (CSAR) resist layer was spin coated and patterned using electron beam lithography (EBL). Next, hydrogen silsesquioxane (HSQ) was spin coated as the 100 nm top dielectric, in which source holes were lithographically defined. The sacrificial layer was removed with 1-methyl-2-pyrrolidone stripper (NMP) followed by remote oxygen plasma at 350°C. A final tetramethylammonium hydroxide (TMAH) wet etch removes the alumina layer exposing the seed, and a dilute HF dip is executed before growth. Growth using Metal Organic Chemical Vapor Depositions (MOCVD) was done in a horizontal reactor using trimethylindium (TMIn), trimethylgallium (TMGa), tertiarybutylphosphine (TBP),

tertiarybutylarsine (TBA) with H_2 as carrier gas. The samples were grown at 600°C, with a group III flux of 5×10^{-6} mol/min and a V/III ratio of 570. For the samples discussed in the study, the growth was initiated with a few monolayers of InP, before switching the growth to n-doped InGaAs. Si doping is incorporated in the InGaAs layer with a disilane flux of 1.43×10^{-8}mol/min. More details on the fabrication, growths and structural characterization of CELO can be found in other references[24,30].Planar epitaxial Si-doped InGaAs samples for carrier density comparison was grown at 600°C, with a group III flux of 3.82×10^{-5} mol/min, a V/III ratio of 8.8 and a disilane fluxes of 1.43×10^{-8}mol/min.

The procedure used for parasitic growth removal is shown schematically in Fig 1. After rinsing the sample in acetone and isopropanol, 6nm aluminum oxide (Al_2O_3) was deposited on the sample in an atomic layer deposition (ALD) chamber using a trimethylaluminum-water (TMA-H_2O) recipe at 300° C. This conformally coats the sample including the outside surface of the growth inside the CELO templates and the parasitic growth (Fig 1C). The samples are then etched in an inductively coupled plasma (ICP) chamber using BCl_3 /Cl_2 chemistry for 15 seconds with an approximate etch rate of 80nm/min. Since ICP etching is highly anisotropic, the etch removes Al_2O_3 that are in line of sight of the ions that are accelerated towards the bottom cathode. Al_2O_3 that covers the outer surfaces of the overgrowths inside the CELO templates, thus remain protected from the ion beams by the thick silicon dioxide on top of it (Fig 1D). This also applies to Al_2O_3 that is underneath the parasitic growths and thus are protected from the incoming ions. The ICP etching effectively exposes the top of the parasitic growths while keeping the nanostructures of interest inside the cavity protected by Al_2O_3.

Using a wet etch these parasitic growths were etched away without affecting the overgrowths in the CELO templates (Fig 1E). For InGaAs etch we used a $H_3PO_4/H_2O_2/H_2O$ (1:1:20) etch for 12 minutes to etch away the parasitic growths (Fig 1E). For CELO having InGaAs growths ending with a thin InP layer, we used a 30 second dilute HCl (HCl: H_2O 1:1) etch for 30 seconds before etching the InGaAs. After careful inspection of the samples to make sure that all parasitic growths have been etched completely, the samples were put into AZ 300 MIF (Metal Ion Free 0.261N Tetramethylammonium hydroxide) developer solution for 5 minutes to etch away any remaining Al_2O_3 (etch rate of 1.6nm/min) and rinsed in acetone and to clean any residues. The samples are thus clean of any parasitic growths and with the original overgrown structures intact (Fig 1F). Dark outlines are sometimes observed after the entire cleaning process in the positions where the parasitic growths initially existed. These are believed to be local changes in the oxide due to parasitic growths nucleations. These are of negligible thickness and usually do not pose any problems while aligning samples or depositing contacts.

The alignment marks, free of all parasitic growths, can now be used in the electron beam lithography tool to etch vias or align contacts on these CELO growths. Using an EBL process with CSAR,

vias were defined (Fig 1G). The vias were etched in the silicon dioxide top layer of the CELO templates, using a $CHF_3/CF_4/O_2$ recipe in the ICP (Fig 1H). After cleaning the samples using plasma ashing and solvent rinse, contacts were patterned using a bilayer resist process. The resist stack consists of 100nm of copolymer EL9 (Ethyl Lactate 9%) and 400nm of PMMA 950K. A 30s dilute HCl (1:10) etch was performed immediately before the metal deposition to etch any remaining oxides. The metal stack consisted of 10nm of Ti followed by 10nm of Palladium and 200nm of Au deposited by electron beam evaporation (Fig 1I).

Fig 2 shows the samples before (Fig 2A-2C) and after (Fig 2D-2F) the wet etching process was performed. Most of the parasitic growths are etched out by this process. Large micro-wire parasitic growths (Fig 2C) are also completely removed (Fig 2F). The contrast from the InGaAs growth inside the templates remains unchanged in the optical microscope and SEM images, indicating that the CELO growths inside the templates are unaffected by this etching process. We compared the effects of our etching process to a conventional plasma assisted dry etch using a methane/hydrogen/argon chemistry in a Reactive Ion Etcher (RIE). Although, RIE based etches work partially in removing the parasitic growths, the etch rates of such dry etches were found to be low and the time to completely remove thick parasitic growths (which are often tens of microns thick) was found to be consistently long (>30-40 minutes). Even though the nanoscale growths of interest are supposed to be protected by a top oxide layer during the plasma etch, atomic force microscopy (AFM) scans revealed that a 20-minute RIE etch results in an extremely rough oxide (Fig 2H). Such plasma processes are known to introduce highly mobile defects in semiconductors[38] and deteriorate the quality of the exposed oxide and are thus generally unfavorable. Similar AFM scans on our wet etch process shows that the root mean square roughness of the oxide, after undergoing such a process is considerably lower (Fig 2G).

To characterize the material properties of these nanostructures after sample cleaning and fabrication of devices, we use two-terminal magneto-transport measurements (in both two-probe and four-probe configuration) instead of conventional Hall measurements. Such transport measurements can help reveal variations in electrical properties of these nanostructures grown under different growth conditions, as well as spatial variations in a single sample. Given the small dimensions of the nanostructures, two-terminal devices offer advantages in terms of fabricating reliable contacts[39,40], compared to a conventional Hall device which requires at least four terminals. Geometries of contacts fabricated on the InGaAs nanostructures, are shown in Fig 3. The devices were measured in a Quantum Design Physical Property Measurement System (PPMS). The devices were wirebonded to a PPMS puck using a $25\mu m$ gold wire. The devices were found to be extremely sensitive to electro-static discharge, so extreme caution was taken to ground the sample while bonding and transfer. The InGaAs devices were measured using standard low

frequency lock-in technique at temperatures ranging from 2K to 50K. The contacts were found to be ohmic at all temperatures from 300K to 2K (Fig S1.A). The resistance of the device increases with decreasing temperatures (Fig S1.B).

Longitudinal resistance R_{xx} was measured as a function of a perpendicular magnetic field (applied out of plane to the sample surface) at 2K. The resistance exhibits positive magnetoresistance with well-defined superimposed oscillations at high fields. Measurements corresponding to two different samples grown under the same growth conditions and similar Si doping concentrations are shown (Fig 4). Sample 1 (Fig 4A-C) was measured using a 4-probe configuration, while sample 2(Fig 4D-F) was measured in a 2-probe configuration (for 2-probe configuration, total line resistance of 4kΩ is effectively added to the device resistance). A parabolic background is observed in the magneto-resistance plots (Fig 4A,4D) which typically arises from the Drude conductivity being inversely related to $(1+(\mu B^2))$, μ being the mobility and B the magnetic field. A 3rd order polynomial background subtraction is performed to analyze the observed oscillations (Fig 4B,4E). At B (>2T), ΔR_{xx} oscillates periodically in 1/B. This can be interpreted as Shubnikov de-Haas oscillations due to the formation of Landau levels (LL) in high magnetic field. Fast Fourier analysis of the oscillations (Fig 4C,4F) reveals frequencies of B_F=39T and B_F=45T corresponding to the sample 1 and sample 2, respectively. Assuming a spherical Fermi surface, the Fermi wavevector corresponding to these two frequencies are $k_{F1} = 0.3463nm^{-1}$ and $k_{F2} = 0.3695nm^{-1}$ with corresponding doping levels of $1.4 \times 10^{18}\ cm^{-3}$ and $1.9 \times 10^{18}\ cm^{-3}$ respectively. These two samples were expected to show similar behaviors because of the same growth conditions, but surprisingly revealed variabilities of doping incorporations between different growth runs – underscoring the importance of characterizing CELO growths. The expected doping concentration based on the Si flow rates in the MOCVD is extracted from room temperature Hall measurements on planar samples. It is not straightforward to compare doping densities from planar growth to CELO nanostructures, since CELO growths typically require a significantly lower group-III flux compared to planar epitaxial growth, to lower parasitic growth rates. The planar sample was grown with the same disilane flux as for the CELO samples (1.43×10^{-8} mol/min) but with a lower V/III ratio. The doping concentration measured in this sample was $2.53 \times 10^{18}\ cm^{-3}$. Since Si doping in planar InGaAs growths decreases significantly with increasing V/III ratio[41], the Si incorporation at a V/III ratio comparable to a CELO growth is likely lower than this number. As a result, Si doping incorporation in InGaAs CELO appear to be comparable to doping incorporation in planar epitaxial growths.

The electron effective mass in these nanostructures can be obtained from the temperature dependence of SdH oscillations in ΔR_{xx}. The amplitude of the SdH oscillations decreases with increasing temperature but the oscillations are observed distinctly till 50 K (Fig 5A). Taking the resistance values at

the peak corresponding to $\frac{1}{B} = 0.092\ T^{-1}$ we fit the peak amplitudes to the Lifshitz-Kosevich equation (LK) [42]

$$\frac{\mathrm{X}}{\sinh(\mathrm{X})}, \text{ where } \mathrm{X} = \frac{\left(2\pi^2 k_B m_e \left(\frac{1}{B}\right) m^* T\right)}{(\hbar e)}$$

Here, k_B is the Boltzmann constant, m_e is the rest mass of an electron, m* is the dimensionless effective cyclotron electron mass, i.e. $m^*=m/m_e$ where m is the mass of electrons in InGaAs, T is the temperature in Kelvin, $\hbar = \frac{h}{2\pi}$, h being the Planck constant and e is the charge of an electron in Coulombs. Fitting the temperature dependence of the peak amplitude to the LK equation (Fig 5B), the effective mass is estimated to be $m=0.075*m_e$. This value is higher than the value of electron effective mass in $In_{0.53}Ga_{0.47}As$ ($0.040 *m_e$ for InGaAs lattice matched to InP [43]). The increase in electron effective mass can be because of combination of factors such as higher band parabolicity due to quantum confinement in the nanostructures[44,45], penetration of electron wavefunction into the barrier oxide layers[46] or possible higher subband occupations[47]. The scattering time τ can be extracted from the slope of the plot of $\mathrm{Ln}(\frac{\Delta R_{xx} sinh(\mathrm{X})}{\mathrm{X}})$ vs 1/B for the peaks in ΔR (Fig 5C). This slope corresponds to $\left(-\frac{\pi.m}{e.\tau}\right)$. The slope value of -45.9 corresponds to an estimated quantum lifetime of $\tau = 2.919\ e^{-14} s$ and a Dingle temperature $T_D = h/ (4\pi^2 \mathrm{x}\ k_B \tau)$, of 41.6 K. These values of effective mass and scattering time corresponds to a quantum mobility of

$$\mu = \frac{e.\ \tau}{m^*.\ m_e} = 684\ \frac{cm^2}{V.s}$$

and a scattering length of

$$l_F = \tau \times \frac{\hbar\ .\ k_F}{m} = 15.6\ \mathrm{nm}$$

The low scattering length and low mobility points to the presence of a large number of defects in this particular sample. This correlates well with transmission electron microscopy studies of these nanostructures exhibiting high density of stacking faults at a high growth temperature[28]. Low field ΔR_{xx} data, show signatures of weak localization (WL) in both samples (Fig S2) which also indicates the presence of disorder in these nanostructures.

In summary, in this letter, we have demonstrated a gentle wet etch process which removes microns of parasitic growth in InGaAs CELO, without affecting the nanostructures of interest. Even with samples that had poor selectivity and had alignment marks completely covered by parasitic growths, this process flow allowed us to achieve perfect alignment of vias and fabricate contacts on these nanostructures. The

method described here, is generic and can be used for CELO growth of most material on a suitable substrate. Since parasitic growths can be effectively removed post-growth with this process, the constraint of being in the narrow window of CELO growth to achieve perfect selectivity becomes less critical. In order to extract important material parameters, we fabricated two-terminal devices to perform electrical measurements in magnetic fields upto 14T. This avoids the unreliability of contacts when four or more contacts need to be fabricated for conventional Hall devices. Low-temperature magneto-transport showed well formed Shubnikov de-Haas oscillations in the longitudinal resistance of these nanostructures, from which approximate doping concentrations were extracted. The dopant incorporations were found to be comparable to the values measured from planar InGaAs growths. We demonstrated how growth variabilities from different growth runs with similar parameters can be extracted using these measurements. We also extracted effective mass, carrier scattering lifetimes and quantum mobilities from analysis of the SdH oscillations. Our work establishes that the etching process combined with low temperature two terminal characterization is extremely useful in characterizing material parameters for CELO nanostructures that might be otherwise difficult to analyze.

This research is funded by the National Science Foundation (NSF 1640030) and by the Semiconductor Research Corporation (2016-EP-2694-A) and made use of shared facilities of the UCSB MRSEC (NSF DMR 1720256) and the Nanotech UCSB Nanofabrication facility.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

REFERNCES:

1. C.Zhang & X.Li III-V nanowire transistors for low-power logic applications: A review and outlook. *IEEE Trans. Electron Devices* **63**, 223–234 (2016).

2. S.W.Eaton, A.Fu, A.B.Wong, C.Z.Ning & P.Yang Semiconductor nanowire lasers. *Nat. Rev. Mater.* **1**, 16028 (2016).

3. S.Nadj-Perge, S.M.Frolov, E.P.A.M.Bakkers, & L.P.Kouwenhoven Spin-orbit qubit in a semiconductor nanowire. *Nature* **468**, 1084–1087 (2010).

4. V.Mourik, K.Zuo, S.M.Frolov, S.R.Plissard, E.P.A.M. Bakkers, L.P. Kouwenhoven Signatures of majorana fermions in hybrid superconductor-semiconductor nanowire devices. *Science.* **336**,

1003–1007 (2012).

5. S. Gazibegovic, D. Car, H. Zhang, S. C. Balk, J. A. Logan, M. W. A. de Moor, M. C. Cassidy, R. Schmits, D. Xu, G. Wang, P. Krogstrup, R. L. M. Op het Veld, K. Zuo, Y. Vos, J. Shen, D. Bouman, B. Shojaei, D. Pennachio, J. S. Lee, P. J. van Veldhoven, S. Koelling, M. A. Verheijen, L. P. Kouwenhoven, C. J. Palmstrøm & E. P. A. M. Bakkers Epitaxy of advanced nanowire quantum devices. *Nature* **548**, 434–438 (2017).

6. T.Bryllert, L.E.Wernersson, T.Löwgren, & L.Samuelson Vertical wrap-gated nanowire transistors. *Nanotechnology* **17**, S227 (2006).

7. P.Long, J.Z.Huang, M.Povolotskyi, D.Verreck, J.Charles, T. Kubis, G.Klimeck, M.J.W.Rodwell, B.H.Calhoun A tunnel FET design for high-current, 120 mV operation. *International Electron Devices Meeting(IEDM), San Francisco, CA,USA,* 30.2.1-30.2.4 (2016).

8. C.Convertino, C.Zota, H.Schmid, D.Caimi, M.Sousa, K.E.Moselund, L.Czornomaz InGaAs FinFETs Directly Integrated on Silicon by Selective Growth in Oxide Cavities. *Materials*. **12**(1), 87. (2019)

9. W. Lu, P.Xie, & C.M.Lieber, Nanowire transistor performance limits and applications. *IEEE Trans. Electron Devices* **55**, 2859–2876 (2008).

10. D.Cutaia, K.E.Moselund, H.Schmid, M.Borg, A.Olziersky, and H.Riel Complementary III–V heterojunction lateral NW Tunnel FET technology on Si, IEEE Symposium on VLSI Technology, Honolulu, HI, USA, 2016, pp. 1-2 (2016)

11. S. Lee, C. -W. Cheng, X. Sun, C. D'Emic, H. Miyazoe, M. M. Frank, M. Lofaro, J. Bruley, P.Hashemi,J. A. Ott, T. Ando, W. Spratt, G. M. Cohen, C. Lavoie, R. Bruce, J. Patel, H. Schmid, L. Czornomaz,V. Narayanan, R. T. Mo and E. Leobandung High Performance InGaAs Gate-All-Around Nanosheet FET on Si Using Template Assisted Selective Epitaxy. IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, pp. 39.5.1-39.5.4.(2018)

12. Y.Tian, S.R.Bakaul, & T.Wu Oxide nanowires for spintronics: materials and devices. *Nanoscale* **4**, 1529 (2012).

13. P.Uredat, M.T.Elm, R.Horiguchi, P.J.Klar, and S. Hara The transport properties of InAs nanowires: an introduction to MnAs/InAs heterojunction nanowires for spintronics. *J. Phys. D. Appl. Phys.* **53**, 333002 (2020).

14. S. Mauthe , N. V. Triviño, Y. Baumgartner ,M. Sousa, D. Caimi, T. Stöferle, H. Schmid , and K.E.

Moselund InP-on-Si Optically Pumped Microdisk Lasers via Monolithic Growth and Wafer Bonding. *IEEE J. Sel. Top. Quantum Electron.* **25**(6), pp. 1-7 (2019).

15. S.Wirths, B.F.Mayer, H.Schmid, M.Sousa, J.Gooth, H.Riel, and K.E. Moselund Room-Temperature Lasing from Monolithically Integrated GaAs Microdisks on Silicon. *ACS Nano* **12**, 2169–2175 (2018).

16. B. Shi & K.M.Lau *Growth of III–V semiconductors and lasers on silicon substrates by MOCVD*. *Future Directions in Silicon Photonics* pp. 229-282 Elsevier (2019).

17. P.Staudinger, S.Mauthe, K.E.Moselund, & H.Schmid Concurrent Zinc-Blende and Wurtzite Film Formation by Selection of Confined Growth Planes. *Nano Lett.* **18**, 7856–7862 (2018).

18. M.Knoedler, N.Bologna, H.Schmid, M.Borg, K.E. Moselund, S. Wirths, M.D. Rossell, and H.Riel Observation of twin-free GaAs nanowire growth using template-assisted selective epitaxy. *Cryst. Growth Des.* **17**, 6297–6302 (2017).

19. A.Okamoto, & K.Ohata, Selective epitaxial growth of gallium arsenide by molecular beam epitaxy. *Appl. Phys. Lett.* **51**, 1512–1514 (1987).

20. L. Czornomaz, E. Uccelli, M. Sousa, V. Deshpande, V. Djara, D. Caimi, M. D. Rossell, R. Erni, J. Fompeyrine Confined Epitaxial Lateral Overgrowth (CELO): A novel concept for scalable integration of CMOS-compatible InGaAs-on-insulator MOSFETs on large-area Si substrates. Symposium on VLSI Technology (VLSI Technology), Kyoto, Japan, pp. T172-T173 (2015)

21. J. Gooth, M. Borg, H. Schmid, V. Schaller, S. Wirths, K. Moselund, M. Luisier, Si. Karg, and H. Riel Ballistic One-Dimensional InAs Nanowire Cross-Junction Interconnects. *Nano Lett.* **17**, 2596–2602 (2017).

22. J. Gooth, M. Borg, H. Schmid, N. Bologna, M. D Rossell, S. Wirths, K. Moselund, K. Nielsch and H. Riel Transition to the Quantum Hall regime in InAs nanowire cross-junctions. *Semicond. Sci. Technol.* **34**, 035028 (2019).

23. P. Aseev, A. Fursina, F. Boekhout, F. Krizek, J. E. Sestoft, F. Borsoi, S. Heedt, G. Wang, L. Binci, S. Martí-Sánchez, T. Swoboda, R. Koops, E. Uccelli, J. Arbiol, P. Krogstrup, L. P. Kouwenhoven, and P. Caroff Selectivity map for molecular beam epitaxy of advanced III-V quantum nanowire networks. *Nano Lett.* **19**, 1, 218–227 (2019)

24. S. T. Šuran Brunelli, B. Markman, A. Goswami, H.-Y. Tseng, S. Choi, C. Palmstrøm, M. Rodwell, and J. Klamkin Selective and confined epitaxial growth development for novel nano-

scale electronic and photonic device structures. *J. Appl. Phys.* **126**, (2019).

25. J.Wallentin & M.T.Borgström Doping of semiconductor nanowires. *J. Mater. Res.* **26**, 2142–2156 (2011).

26. S.A.Dayeh, R. Chen, Y.G. Ro, & J.Sim, Progress in doping semiconductor nanowires during growth. *Mater. Sci. Semicond. Process.* **62**, 135–155 (2017).

27. N. Bologna, S. Wirths, L. Francaviglia, M. Campanini, H. Schmid, V. Theofylaktopoulos, K. E. Moselund, A. Fontcuberta i Morral, R. Erni, H. Riel, and M. D. Rossell Dopant-Induced Modifications of Ga xIn(1- x)P Nanowire-Based p-n Junctions Monolithically Integrated on Si(111). *ACS Appl. Mater. Interfaces* **10**, 32588–32596 (2018).

28. A. Goswami, S. T. Šuran Brunelli, B. Markman, A. A. Taylor, H.-Y. Tseng, K. Mukherjee, M. Rodwell, J. Klamkin, and C. J. Palmstrøm Controlling Facets and Defects of InP Nanostructures in Confined Epitaxial Lateral Overgrowth. *Phys. Rev. Mater.* **4,** 123403 (2020)

29. M. Borg, L. Gignac, J. Bruley, A. Malmgren, S. Sant, C. Convertino, M. D Rossell, M. Sousa, C. Breslin, H. Riel, K. E Moselund and H. Schmid Facet-selective group-III incorporation in InGaAs template assisted selective epitaxy. *Nanotechnology* **30**, (2019).

30. S. T. Šuran Brunelli, A. Goswami, B. Markman, H.-Y. Tseng, M. Rodwell, C. Palmstrøm, and J. Klamkin Horizontal heterojunction integration via template-Assisted selective epitaxy. *Cryst. Growth Des.* **19**, 7030–7035 (2019).

31. Ma. Friedl, K. Cerveny, P. Weigele, G. Tütüncüoglu, S. Martí-Sánchez, C. Huang, T. Patlatiuk, H. Potts, Z. Sun, M. O. Hill, L. Güniat, W. Kim, M. Zamani, V. G. Dubrovskii, J. Arbiol, L. J. Lauhon, D. M. Zumbühl, and A. Fontcuberta i Morral Template-Assisted Scalable Nanowire Networks. *Nano Lett.* **18**, 2666–2671 (2018).

32. P. Chuang, S.-C. Ho, L. W. Smith, F. Sfigakis, M. Pepper, C.-H. Chen, J.-C. Fan, J. P. Griffiths, I. Farrer, H. E. Beere, G. A. C. Jones, D. A. Ritchie & T.-M. Chen All-electric all-semiconductor spin field-effect transistors. *Nat. Nanotechnol.* **10**, 35–39 (2015).

33. T.Schäpers, J.Knobbe, & V.A.Guzenko Effect of Rashba spin-orbit coupling on magnetotransport in InGaAs/InP quantum wire structures. *Phys. Rev. B - Condens. Matter Mater. Phys.* **69**, 1–5 (2004).

34. K.Takase, Y. Ashikawa, G. Zhang, K.Tateno, & S.Sasaki Highly gate-tuneable Rashba spin-orbit interaction in a gate-all-around InAs nanowire metal-oxide-semiconductor field-effect transistor.

Sci. Rep. **7**, 1–9 (2017).

35. J. J. Hou, F. Wang, N. Han, H. Zhu, K. Fok, W.C. Lam, S.P. Yip, T.F. Hung, J. E.-Y. Lee, and J.C. Ho Diameter dependence of electron mobility in InGaAs nanowires. *Appl. Phys. Lett.* **102**, (2013).

36. R. Rana, L. Balaghi, I. Fotev, H. Schneider, M. Helm, E. Dimakis, and A. Pashkin Nonlinear Charge Transport in InGaAs Nanowires at Terahertz Frequencies. *Nano Lett.* **20**, 3225–3231 (2020).

37. I. Yang, X. Zhang, C. Zheng, Q. Gao, Z. Li, L. Li, M. N. Lockrey, H. Nguyen, P. Caroff, J. Etheridge, H. H. Tan, C. Jagadish, J. Wong-Leung, and L. Fu Radial Growth Evolution of InGaAs/InP Multi-Quantum-Well Nanowires Grown by Selective-Area Metal Organic Vapor-Phase Epitaxy. *ACS Nano* **12**, 10, 10374–10382 (2018).

38. Avram, M., Avram, A., Purica, M., Popescu, A. M. & Voitincu, C. Characterization of defects generated during reactive ion etching. *Proc. Int. Semicond. Conf. CAS* **1**, 249–252 (2009).

39. F.Léonard & A. A. Talin Electrical contacts to one- and two-dimensional nanomaterials. *Nat. Nanotechnol.* **6**, 773–783 (2011).

40. A. Guo Nano-scale metal contacts for future III-V CMOS. *Phd. Thesis* 1–66 (2012).

41. J.B.Yoo, J.S. Kim, D. H. Jang,B.-H. Koak, D.-K. Oh, H.-M. Kim, Y.-T. Lee Effects of V/III ratio on Si-doping in InGaAs lattice-matched to InP grown by organometallic vapor phase epitaxy. *J. Cryst. Growth* **132**, 43–47 (1993).

42. E.M.Lifshits, A.M.Kosevich Theory of the Shubnikov-de Haas effect. *J. Phys. Chem. Solids* **4**, 1–10 (1958).

43. R. J. Nicholas, J. C. Portal, C. Houlbert, P. Perrier, and T. P. Pearsall An experimental determination of the effective masses for $Ga_xIn_{1-x}As_yP_{1-y}$ alloys grown on InP. *Appl. Phys. Lett.* **34**, 492–494 (1979).

44. D. Schneider, L. Elbrecht, J. Creutzburg, A. Schlachetzki, and G. Zwinge In-plane effective mass of electrons in InGaAs/InP quantum wells. *J. Appl. Phys.* **77**, 2828–2830 (1995).

45. R. W. Martin, S. L. Wong, D. M. Symons, R. J. Nicholas,M. A. Gibbon, E. J. Thrush and J. P. Stagg Selective area epitaxy of InGaAs/InGaAsP quantum wells studied by magnetotransport. *Semicond. Sci. Technol.* **11**, 735–740 (1996).

46. A. M. Kurakin, S. A. Vitusevich, S. V. Danylyuk, H. Hardtdegen, N. Klein, Z. Bougrioua, A. V. Naumov, and A. E. Belyaev Quantum confinement effect on the effective mass in two-dimensional electron gas of AlGaN/GaN heterostructures. *J. Appl. Phys.* **105**, (2009).

47. D.Schneidera,F.Hitzela,A.Schlachetzkib,P.Boensch Dependence of electron effective mass on the subband occupation in $In_{0.53}Ga_{0.47}As$/InP quantum wells. *Phys. E Low-Dimensional Syst. Nanostructures* **12**, 562–565 (2002).

FIGURES:

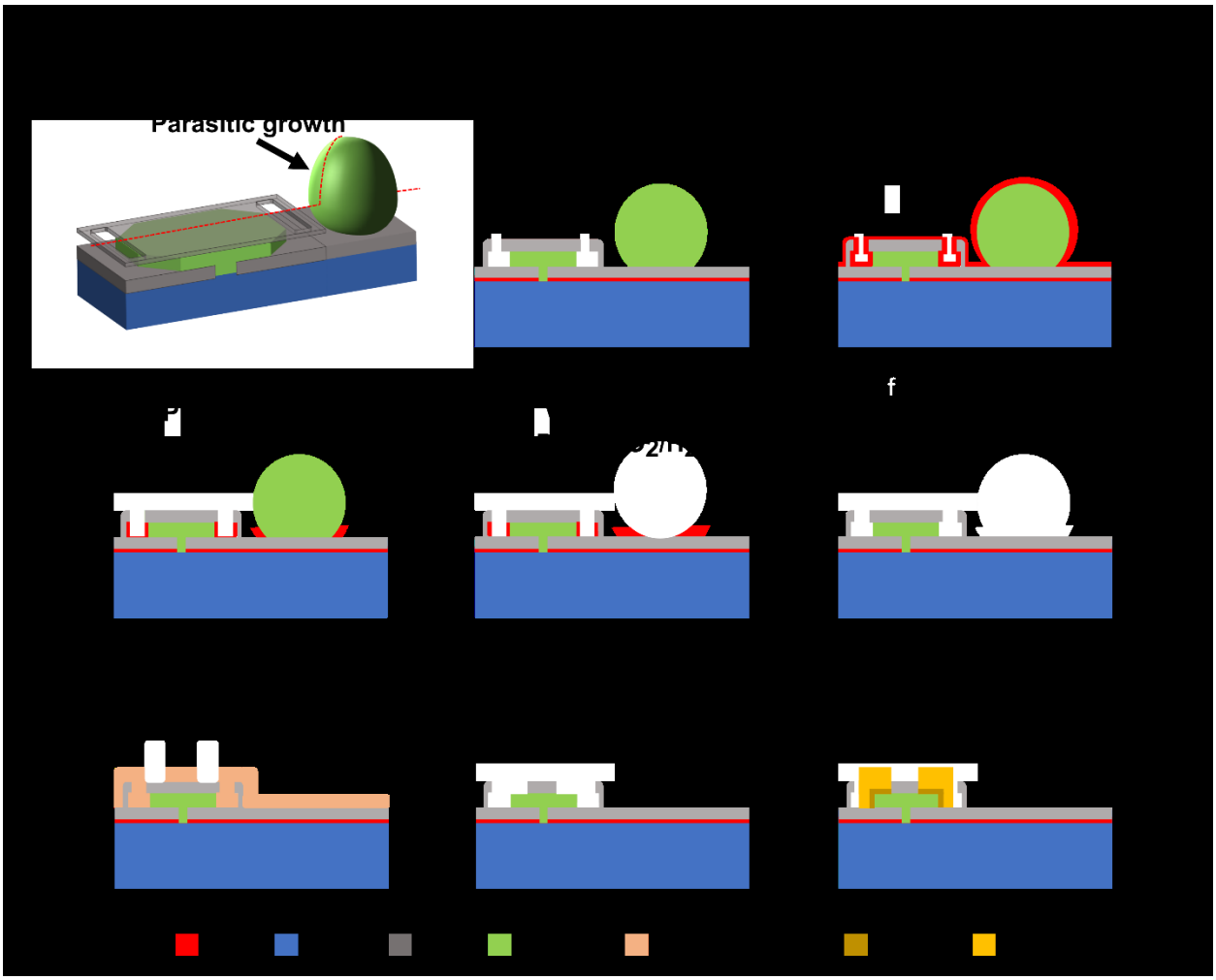

Figure 1: (A) shows the 3D schematic of InGaAs CELO growth along with a parasitic growth. (B) shows a cross section schematic taken along the red dashed line in (A). (C)-(I) shows the process flow for selectively cleaning parasitic growth and fabrication of vias and contacts

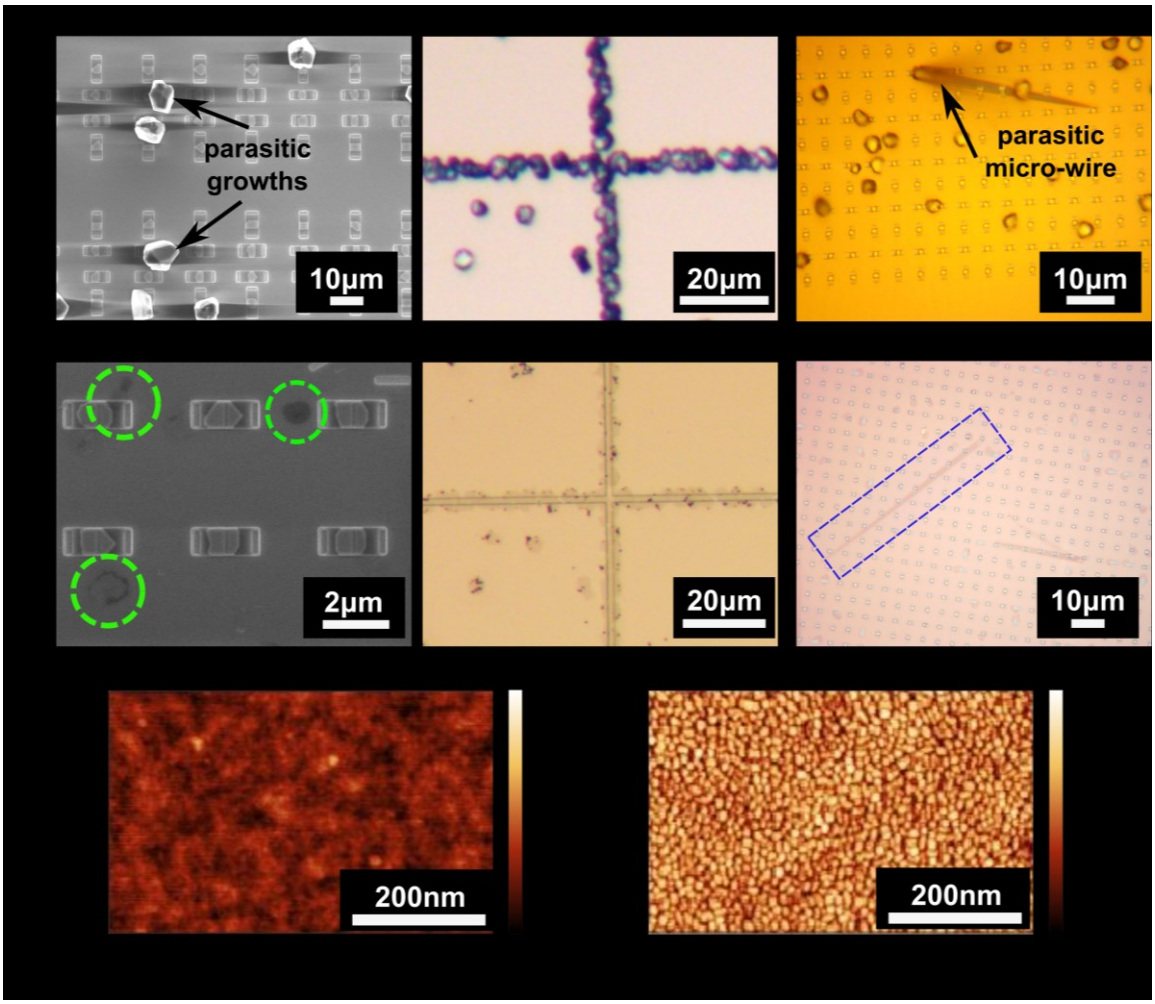

Figure 2: (A), (B), (C) show a CELO InGaAs sample and (D), (E), (F) the corresponding samples after the cleaning processes described in the text. (A) and (D) are SEM images while (B),(C),(E),(F) are optical microscope images. Green circles in (D) show where parasitic growths were before the cleaning process. Dashed box in (F) shows a region (different from C) where a parasitic microwire growth existed before etching. (G) shows the surface of the SiO2 after the wet etch process. (H) shows the SiO2 surface after 20 minutes of exposure to MHA plasma etch in the RIE.

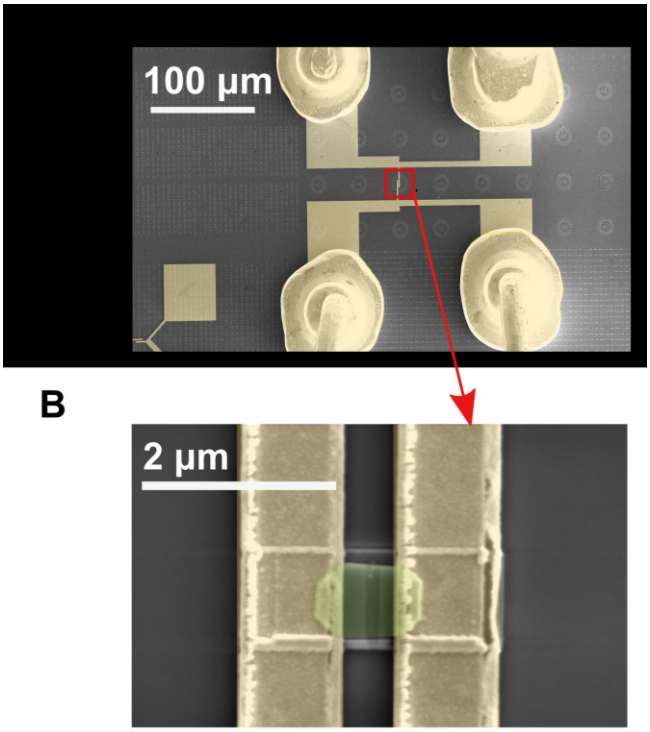

Figure 3:(A) False color SEM images of contact with device (B) magnified SEM image of InGaAs CELO device (marked in green) with etched vias and contacts

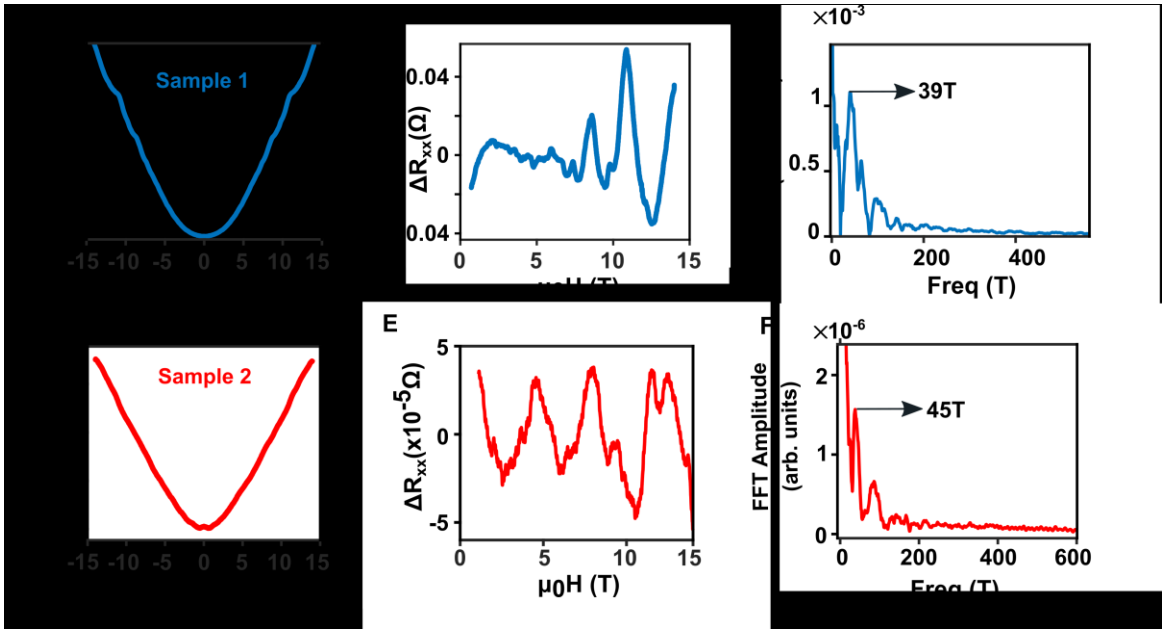

Figure 4: Low temperature magneto-transport. (A-C) shows measurements for sample 1 and (D-F) shows measurements of sample 2. (A,D) shows longitudinal magnetoresistance for sample 1. (B,E) shows data in (A,D) after background subtraction, respectively. SdH oscillations are visible in both samples. (C,F) shows the FFT of the oscillations for the two samples. Peaks are observed for subband oscillations corresponding to 39T and 45 T for sample 1 and 2. These correspond to doping concentrations of $1.4 \times 10^{18} cm^{-3}$ and 1.9×10^{18} cm^{-3} respectively. Sample 1 was measured in 4-probe configuration while sample 2 was measured in 2-probe configuration (with 4kΩ series line resistance).

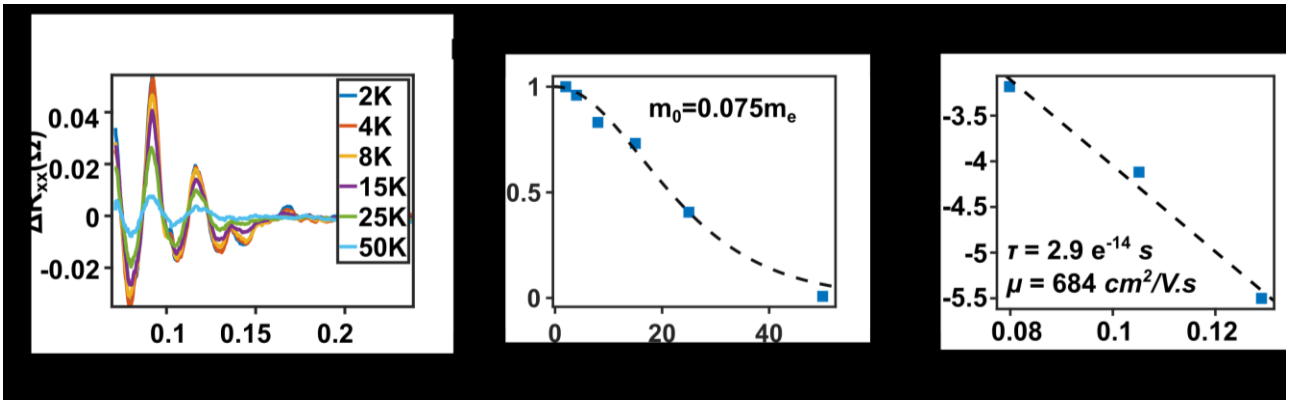

Figure 5: (A) shows the background subtracted magnetoresistance for sample 1 (Fig 4A-C) in inverse field at temperatures from 2K to 50K. (B) Fit of peak amplitude to Lifshitz-Kosevich equation to extract effective mass of m=0.075*m_e. (C) shows the Dingle plot extracted from peak amplitudes in (A). Slope from linear fits gives quantum scattering lifetime and quantum mobility.

Supplementary information: A gentle parasitic growth removal process to enable low temperature magneto-transport characterization in confined epitaxial lateral growth of InGaAs

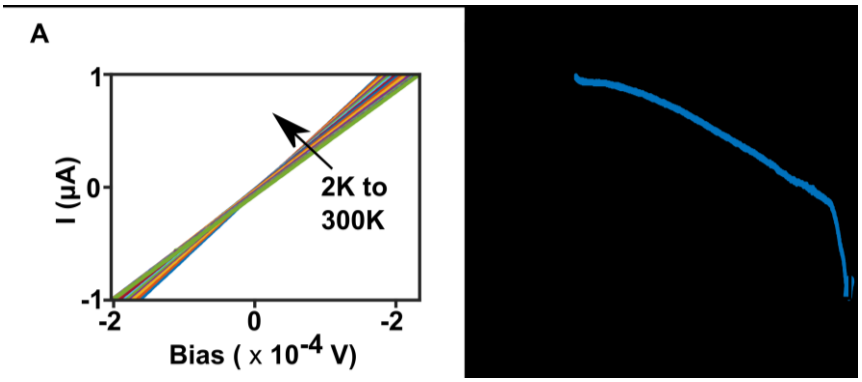

Figure S1: (A) I-V curves at different temperatures (B) Resistance vs Temperature curve for longitudinal resistance measured in 2-probe configuration for sample 2.

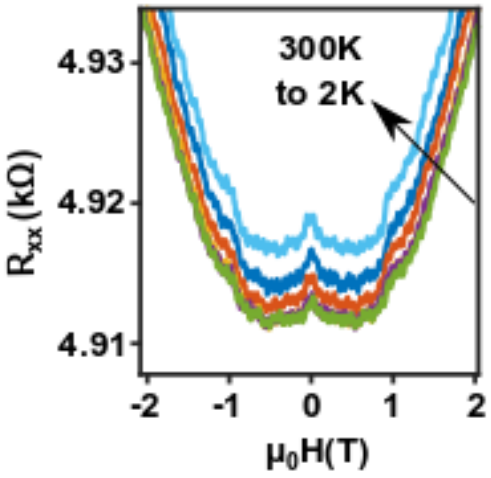

Figure S2: Longitudinal magnetoresistance of sample 2, measured in 2-probe configuration showing peaks at low field (<1T) pointing to signatures of weak localization in the sample. The peak amplitude decreases with increasing temperatures.