Atomic Layer Deposition of TiN/Ru Gate in InP MOSFETs

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InP-channel planar and vertical MOSFETs utilizing atomic layer deposition of a TiN/Ru gate are fabricated. The performance of the TiN/Ru gate is compared to a Ru-only gate based on C-V characteristics of MOS (Metal Oxide Semiconductor) Capacitors (MOSCAPs), and peak transconductance (g_m) and subthreshold swing (SS) in planar MOSFETs. Compared to devices with conventional Ni/Au gate metal, these having a 70mV/dec SS,[1] the long gate length TiN/Ru gate devices exhibit an average 68 mV/dec SS , a record low value of InP, suggesting a high quality, low-damage high-k/InP interface. A record high peak g_m of 0.75 mS/μm at V_{DS} = 0.6 V on an InP channel is achieved in a planar gate length (L_g) = 80 nm device. A vertical MOSFET shows a reasonably conformal Ru coverage of the vertical fin, and a high 0.42 mS/μm peak g_m for a L_g = 50 nm device. The results of planar and vertical MOSFETs show that TiN/Ru gate metallization via atomic layer deposition is promising for non-planar III-V MOS devices.

III-V MOS structures are of potential interest in III-V MOSHEMTs,[2,3] targeting applications in mm-wave receivers, and in the gate structure of tunnel FETs for ultra-low voltage VLSI logic.[4–7] MOSFETs with subthreshold swings approaching 60 mV/decade have been demonstrated with ZrO_2 and HfO_2 gate dielectrics on InGaAs, InAs, and InP channels, indicating dielectric/semiconductor interface trap densities (D_{it}) less than 3×10^{12} $cm^{-2}eV^{-1}$.[1,8–10] Previous results have generally used gate metals deposited by sputtering or thermal evaporation. For nonplanar finFETs and next generation gate-all-around (GAA) nanowire transistors, a more uniform and conformal high-k metal gate (HKMG) are necessary to ensure a low gate resistance and a consistent threshold voltage distribution.[4,11,12] Thus, atomic layer deposited (ALD) HKMG, with its superior uniformity in thickness and conformity, had been demonstrated in InGaAs FinFETs.[13] There have been no reports of ALD HKMG with low D_{it} on InP channels. Here we present an ALD low D_{it} Ru/TiN/ZrO_2 HKMG on InP with a lowest SS of 68mV/dec in long gate length planar devices, as well as comparable peak g_m on vertical MOSFETs.

Ruthenium has a desirable metal workfunction for III-V N-MOSFETs, as well as low resistivity, and good thermal stability. One key to the successful ALD growth of Ru is controlled nucleation on dissimilar materials.[14] Nucleation and growth initiation of ALD Ru appear to vary with substrates used. Rough and non-uniform growth on SiO_2, low-k dielectrics, and TaN surfaces has been reported.[15–17] Films with poor nucleation have also exhibited poor electrical properties.[18] Yim *et al.* reported ALD Ru with an improved nucleation on a thin SiN_x or heavily NH_3-plasma activated (50 minute exposure) SiO_2 surface according to TEM analysis.[16] M. Zhang *et al.*, on the other hand, demonstrated improved ALD Ru nucleation with an Al_2O_3 surface layer.[19] Overall, it was suggested that one can improve the nucleation of Ru growth by surface energy engineering, which helps the adsorption of Ru precursors.[20] The addition of an Al_2O_3 interlayer and plasma treatment prior to Ru deposition in MOS structures, however, may degrade device electrical performance due to increased effective-oxide-thickness (EOT), increased interface trap density, and a shift in the MOS threshold voltage. Therefore, it is important to consider tradeoffs in ALD Ru HKMG design between Ru film quality and overall device performance. In this work, a thin ALD TiN layer (~2 nm) is deposited as a nucleation/stiction layer in Ru gate devices.[21] TiN/Ru gates and Ru-only gates on InP channel are compared. Capacitance-voltage (C-V) characteristics of MOSCAP structures, and SS and peak g_m of planar MOSFETs, are employed to evaluate the performance of the two metal gate stacks. Ru growth is further optimized for a better conformity. At last, vertical MOSFETs with conformal TiN/Ru gates are demonstrated. Transfer and output characteristics of vertical MOSFETs are compared to their planar counterpart.

Planar MOSFETs were fabricated on semi-insulating (S.I.) (100) Fe-doped InP substrates. The fabrication started with epitaxial growth of the channel by metal organic chemical vapor deposition (MOCVD). The MOCVD channel growth was performed at 600℃, and consists of a bottom 9 nm, 8×10^{17} cm^{-3} Zn-doped *P*-InP layer to compensate for the donor impurities at the growth interface, and a top 9 nm unintentionally-doped (U.I.D.) InP layer. After channel growth, a dummy gate was defined by electron beam lithography (EBL) using hydrogen silsesquioxane (HSQ) resist for subsequent self-aligned raised source/drain MOCVD regrowth. A 1-minute dip in HCl: H_2O 1:10 was done prior to the regrowth. For the source/drain, a 9 nm U.I.D. InP spacer, 10nm, 2×10^{19} cm^{-3} Si-doped N^+-InP , and 110 nm, 4×10^{19} cm^{-3} Si-doped N^+-$In_{0.53}Ga_{0.47}As$ layers were grown at 600℃. Devices were then isolated by selective wet etch using HCl- and H_3PO_4:H_2O_2-based solutions. After a two minutes buffered HF (BHF) dip followed by one cycle of a HCl-based digital etch to remove the dummy gate and surface oxides, high-k and metal gate layers were deposited in an Oxford FlexAL ALD system. The high-k deposition process includes initial surface passivation using 9 cycles of alternating N_2-plasma and trimethylaluminum (TMAl) dosing (~1 nm AlO_xN_y)[9,22] followed by 40 cycles of H_2O and tetrakis(ethylmethylamido)zirconium (TEMAZ) dosing (~2.5 nm ZrO_2) at 300℃.[23] To further passivate surface dangling bonds, a 30 minute ALD in-situ H_2 anneal was performed at 350℃. Metal gate deposition at 300℃

utilizes a 35 cycles of TiN nucleation layer (~2 nm) first deposited using Tetrakis(dimethylamido)titanium (TDMAT) together with a N_2- and H_2-plasma (400W inductively coupled plasma (ICP) power). 500 cycles of ALD Ru (~30 nm) was then deposited using (ethylbenzene)(1,3-cyclohexadiene)ruthenium (EBCHDRu) and O_2 cycles at 300℃. EBCHDRu is a zero-valent organometallic precursor (Hansol Chemical, Korea). In-situ post-metal annealing in H_2 ambient at 350℃ was employed for 30 minutes to recover plasma damage at the high-k/InP interface. The Ru metal gate patterns were dry etched using an O_2-based ICP etch (catalyzed with a small of amount of Cl_2).[24] The TiN and the high-k dielectric layers were etched via a 1-minute BHF dip. Source and drain metal contacts (Ti/Pd/Au) were deposited by lift-off. Devices were finally passivated using Al_2O_3 (~3 nm) deposited by ALD.

The vertical MOSFETs were fabricated in a top-down process. The epitaxial stack consisted of, from bottom to top, a Fe-doped S.I. (100) InP substrate, a 90 nm thick Si-doped N^+-$In_{0.53}Ga_{0.47}As$ (4×10^{19} cm^{-3}) source layer, 5 nm thick Si-doped N^+-InP (2×10^{19} cm^{-3}) layer, a 50 nm thick Zn-doped P-InP (1×10^{18} cm^{-3}) channel layer, a 5 nm thick Si-doped N^+-InP (2×10^{19} cm^{-3}) drain layer, and a 10 nm thick Si-doped N^+-$In_{0.53}Ga_{0.47}As$ (4×10^{19} cm^{-3}) contact layer. All layers were grown by MOCVD at 600℃. A refractory Mo/TiW (20/500 nm) drain metal contact was deposited by electron beam deposition and DC sputtering, respectively, and then patterned using EBL followed by ICP etching.[25] A 20 nm SiN_x sidewall was formed by plasma-enhanced chemical vapor deposition (PECVD) followed by an anisotropic CF_4-based plasma etch. The 10 nm InGaAs contact layer was wet etched in H_3PO_4: H_2O_2: H_2O 1:1:25. A second 20 nm Si_3N_4 sidewall was then formed. The InP drain and channel were wet etched in HCl:H_3PO_4 1:4. The vertical surface sidewalls of the p-type InP layer acted as the transistor channel. Prior to high-k deposition, 5 cycles of HCl-based digital etching were performed for native oxide removal on the channel surface. The high-k deposition, H_2 annealing and TiN deposition processes were identical to the fabrication of the planar MOSFET's detailed above. The ALD Ru deposition, on the other hand, had to be carried out at a lower temperature of 250℃ to ensure conformal growth on the sidewalls of the vertical MOSFET structure (avoiding a small precursor decomposition on the structure at 300℃).[26,27] To avoid formation of surface RuO_2 during this lower temperature Ru process, a layer which inhibits the growth of a metallic Ru layer, H_2 is added as a reducing co-reactant in the ALD growth cycle.[28] The same post-metal annealing and TiN/Ru patterning steps for planar MOSFETs were employed. Ti/Pd/Au source contact metal was evaporated and lifted off. Ti/Au metal posts were deposited on source and gate contacts for back-end wiring. A 30 nm PECVD SiN_x passivation layer was deposited prior to planarization with spin-on dielectric benzocyclobutene (BCB). The BCB dielectric was baked at 250℃ for 1 hour, and ashed back with a ICP CF_4/O_2 plasma. The SiN_x passivation layer was removed in a BHF dip to expose the TiW drain contact. Excess Ru/TiN/high-k stack that surrounded the TiW/Mo drain contact was wet etched using ruthenium etchant

(Transcene RU-44) and BHF. A thick 60 nm SiN_x sidewall spacer was formed by PECVD followed by CF_4-based plasma etch to prevent drain-to-gate short. Finally, Ti/Au (15/10000 nm) metal pads were lifted off to finish the back-end wiring.

Non-uniform substrate color after Ru deposition on ZrO_2 was sometimes observed, suggesting a less than ideal Ru nucleation on ZrO_2. By depositing a thin TiN layer (via ALD) prior to Ru growth, uniform nucleation on any arbitrary substrate can be realized. Fig. 1 shows the C-V characteristics of InP MOSCAPs with (a) TiN/Ru and (b) Ru gates measured from 1kHz to 1MHz. The threshold voltage of TiN/Ru gate MOSCAP is 0.25 V, which is lower than the 0.4 V measured for the Ru-only gate. The large apparent increase in capacitance in accumulation at low frequencies f is a measurement artifact due to gate leakage, as the conductivity dI/dV becomes comparable to $2\pi fC$, where C is the capacitance. The leakage current of the MOSCAPs is ~ 30 mA/cm^2 at V_g = 1 V and is similar for both Ru and TiN/Ru gates. A larger frequency dispersion for Ru gate MOSCAP in depletion can be seen. In comparison, the TiN/Ru gate MOSCAP shows smaller frequency dispersion, suggesting a metal-semiconductor interface with low defect density. Furthermore, the C-V characteristic of the TiN/Ru gate MOSCAP is comparable with that using a thermally evaporated Ni/Au gate, which confirms a high quality high-k/InP interface and a low-damage gate metallization process.[1] This suggests that the adding a thin TiN layer not only improves the nucleation of Ru, but also resolves the frequency dispersion in the case of Ru-only gates.

Fig. 2 shows the schematic planar MOSFET structure used in this study (a) and the TEM images of a L_g = 30 nm MOSFET (b). The recess structure and U.I.D InP spacer are used to suppress band-to-band tunneling (BTBT) arising at the high-field region near the drain end of channel.[29] The regrowth facet with HSQ mask shows a ~30° incline at the channel after InP growth and a ~54° incline after InGaAs growth. The corresponding InP spacer thickness at the channel is approximately 5 nm. The inner highlight in Fig. 2(b) is high-angle annular dark-field imaging (HAADF) STEM image. The interfacial layers contain ~1/2.5/2 nm AlO_xN_y/ZrO_2/TiN, as indicated by layer 1, 2 and 3, respectively. In addition, the thickness of Ru film in the channel is ~10 nm, which is much thinner than thickness in-field (~25 nm). This variability in thickness does not affect the DC performances of the planar MOSFETs, but could potentially increase the gate resistance or even result in gate open-circuits in more complex vertical transistor structures that require the gate metal to contacting the sidewall channel. Therefore, a more conformal Ru deposition is needed for vertical MOSFETs, and a process to improve Ru conformity will be discussed later.

The gate length of fabricated planar MOSFETs ranges from 30 nm to 2 μm. The transfer and output characteristics of TiN/Ru gate planar MOSFETs with L_g = 30, 80, 200 nm are shown in Fig. 3. The regrown N^+ S/D layer sheet resistance is ~14 Ω, while the S/D contact resistivity is 7 Ω-μm^2, as determined by transmission line method (TLM). At L_g > 200 nm, a more than 5 orders of magnitude on/off ratio is achieved. The peak g_m of ~0.75 mS/μm is for a L_g = 80 nm MOSFET at V_{DS} = 0.6

V. This is the highest peak g_m reported for InP channel MOSFETs. Due to a comparably thick channel of ~18 nm, MOSFETs with L_g < 80 nm suffer short-channel effects. At L_g = 30 nm, the on/off ratio drops to of order 1000:1, and the peak g_m decreases. In addition, all the planar MOSFETs here reported have significant gate leakage ($|I_G|$) of ~10^{-4} mA per μm of gate width, as can been seen in the transfer curves. The high $|I_G|$ arises from parasitic TiN/Ru present on the sidewalls of the N^+ S/D mesa. Given the large perimeter of the transistor mesa, the estimated parasitic area so covered is ~100:1 greater than the device active gate region. The gate leakage per total MOS junction area, gate and sidewall, in the planar MOSFETs is similar to that observed in the MOSCAPs.

Fig. 4 summarizes (a) peak g_m vs L_g at V_{DS} = 0.6 V and (b) $S.S.$ vs L_g with ALD Ru gates, TiN/Ru gates (this work) and thermal evaporated Ni/Au gate MOSFETs.[1] Note that the channel thickness in this work is ~18 nm, which is ~4 nm thicker than for the Ni/Au gate MOSFETs plotted in Fig. 4. Transistors with ALD TiN/Ru gates had the highest peak g_m of ~0.75 mS/μm for a L_g = 80 nm transistor. In comparison, Ru-only gates show lower peak g_m, which is consistent with the larger observed frequency dispersion in C-V characteristics as shown before. In addition, the Ru-only gate MOSFETs showed wide variations in characteristics between devices and low yield due to poor nucleation of Ru on the high-k gate dielectric. Correlating with the observed C-V dispersion of MOSCAPs using Ru-only gates, the SS of MOSFETs using Ru-only gates is >80 mV/dec. even at long gate lengths.

A record low SS, for an InP channel, of 68 mV/dec at V_{DS} = 0.1 V for TiN/Ru gate MOSFETs is measured over 10 different > 800 nm-L_g devices. This value is lower than the previously reported 70 mV/dec on thermal Ni/Au MOSFETs.[1] From this, we calculate an D_{it} of ~1×10^{12} $cm^{-2}eV^{-1}$, consistent with MOSCAP test structure results. Compared to the thermal Ni/Au gate, the ALD TiN/Ru gate exhibits a lower MOSCAP frequency dispersion under depletion, indicative of lower D_{it} near to band edge. This is consistent with the superior g_m and SS observed with MOSFETs using the ALD TiN/Ru gate.

As pointed out earlier, although ALD growth of Ru at 300°C yields a high conductivity metallic film, it is compromised by inadequate conformality on sidewalls due to a small amount of thermal decomposition of the precursor.[26,27] For improved step/sidewall coverage, an essential requirement for non-planar structures, deposition at 250°C is employed on vertical MOSFETs instead. Fig. 5 (a) and (b) show the cross-sectional and top-view of a vertical MOSFET structure. The TEM image, as shown in (c), is the cross-sectional cut along A and A' as indicated in Fig. 5 (b). The image shows the InP channel is covered by a uniform TiN/Ru film. The 250°C Ru film shows conformally underfilling of notches near to InP channel and almost constant thickness on the sidewalls and in the field, on top of N^+ InGaAs source. The TEM image shows an air gap between

the BCB planarization material and the Ti/Au pad metal; this may be due to BCB contraction during the relatively high temperature Ti/Au deposition.[30]

The I_D-V_D and I_D-V_G characteristics of vertical MOSFETs with TiN/Ru gate are shown in Fig 6 (a) and (b). As can be seen, strong short-channel characteristics are observed. The low aspect ratio between gate length and fin width (50:90 nm) results in poor gate electrostatics. Despite the higher bulk potential barrier in P-InP channel with doping concentration of 1×10^{18} cm^{-3}, high leakage current density in the thick InP is present. To overcome this issue, a higher P channel doping or a higher aspect ratio between L_g and body thickness (t_{body}) is needed. Nevertheless, peak g_m at V_{DS} = 0.6 V of the vertical MOSFETs measures 0.42 mS/μm, comparable with the L_g = 50 nm TiN/Ru gate planar MOSFET. This confirms ALD TiN/Ru/high-k gate's low surface trap density on non-planar InP device structures.

In summary, planar and vertical InP channel MOSFETs using ALD TiN/Ru gate are fabricated. The TiN/Ru gate exhibits better performance than Ru-only gates in MOSCAP C-V characteristics, and in the SS and g_m in planar MOSFETs. TiN/Ru gate also shows less frequency dispersion along with a record low average SS of 68 mV/dec in long gate length devices, indicating a high quality ZrO_2/InP interface and a low-damage gate metallization process. By utilizing TiN/Ru gates in scaled planar MOSFETs, a record high ~0.75 mS/μm peak g_m for InP is observed at L_g = 80 nm and V_{DS} = 0.6 V. Vertical MOSFET utilizing TiN/Ru gates are also demonstrated. The vertical transistor shows a similar ~0.42 mS/μm peak g_m at V_{DS} = 0.6 V at the same 80nm gate length as the planar MOSFET, which confirms the applicability of this gate metallization process in non-planar structures.

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The data that support the findings of this study are available from the corresponding author upon reasonable request.

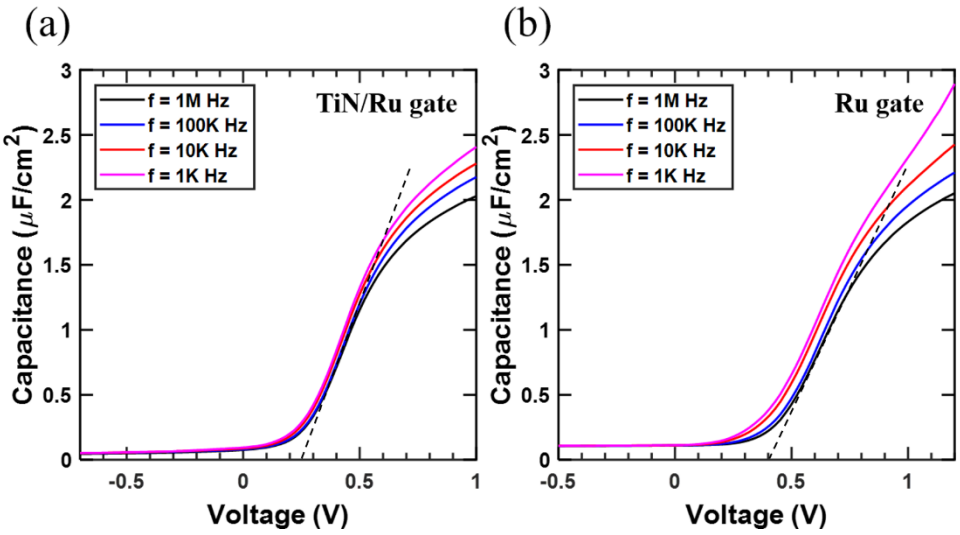

FIG. 1. The C-V characteristic of InP channel MOSCAPs with (a) TiN/Ru gate and (b) Ru gate. The large increase in capacitance in accumulation region at low frequencies is a measurement artifact due to gate leakage, arising when G/ω becomes comparable to the capacitance. TiN/Ru gate shows much less frequency dispersion in depletion region, indicating a high quality high-k/InP interface and low damage gate metallization.

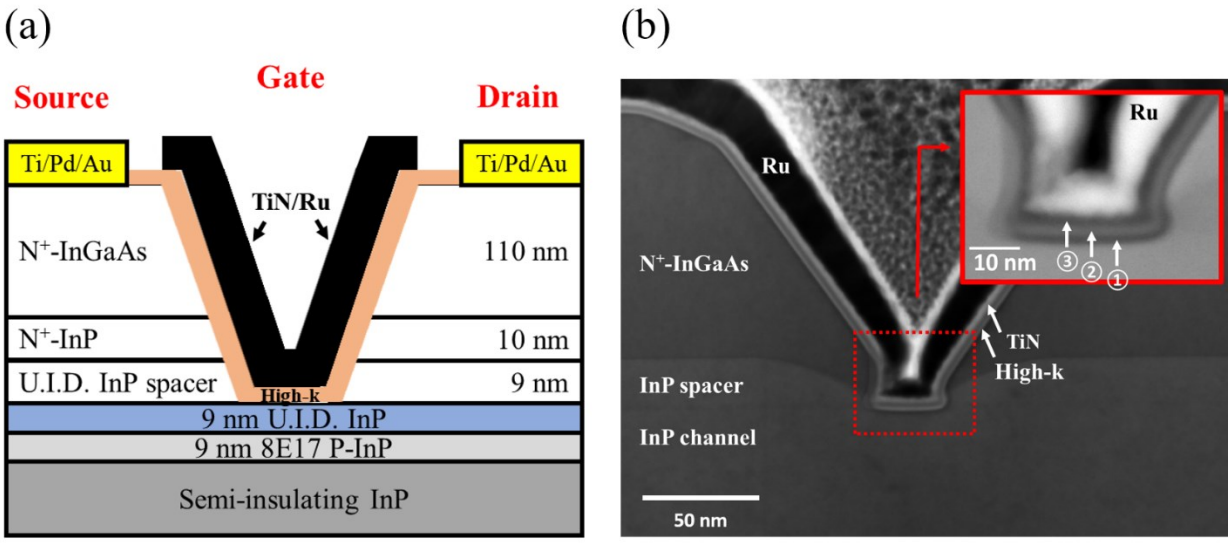

FIG. 2. (a) The cross-sectional planar MOSFET structure and (b) the STEM image of a L_g = 30 nm MOSFET with TiN/Ru gate. The inner plot in (b) is the HAADF-STEM image highlighting the structure at InP channel. Layer 1, 2, and 3 represent ~1 nm AlO_xN_y, ~2.5 nm ZrO_2 and ~2 nm TiN, respectively.

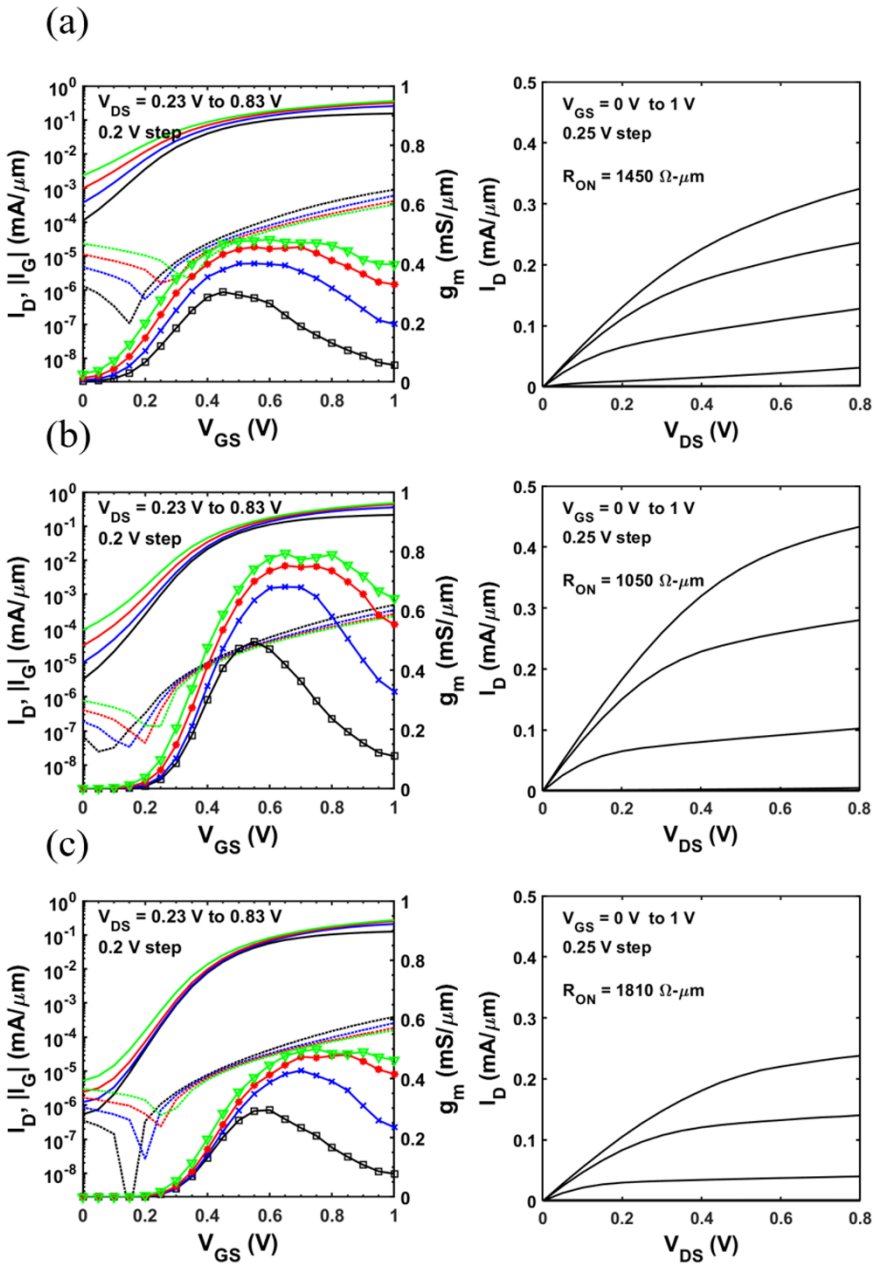

FIG. 3. Transfer (left) and output (right) characteristics of TiN/Ru gates planar MOSFETs with L_g = 30 nm (a), 80 nm (b), 200 nm (c). In transfer characteristics, solid lines, dotted lines, and symbolic lines represent I_D, $|I_G|$, and g_m, respectively.

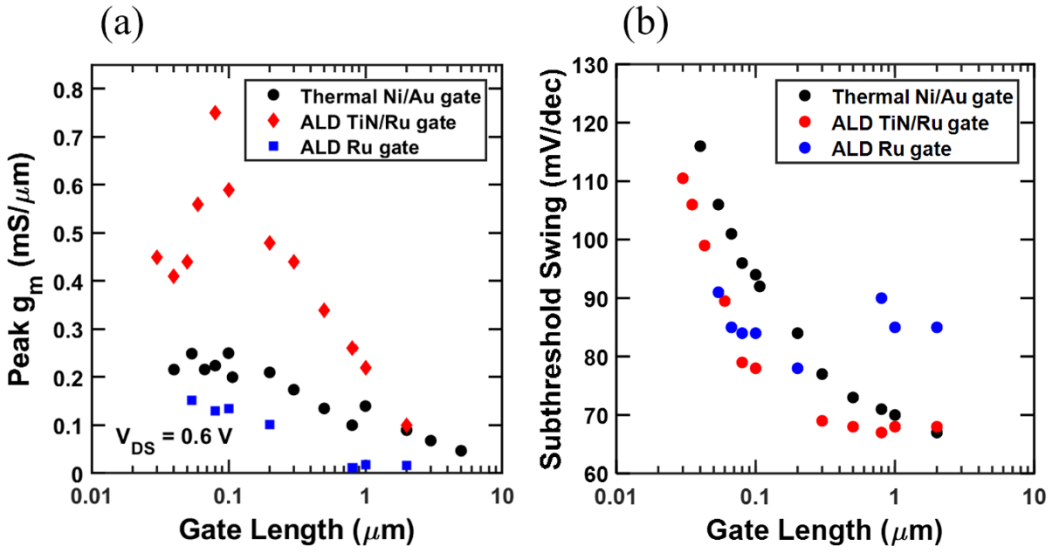

FIG. 4. The comparison of peak g_m vs L_g (a) and the minimum SS vs L_g (b) for InP planar MOSFETs with thermal evaporated Ni/Au gates,[1] ALD TiN/Ru gates, and ALD Ru gates. The average minimum SS for 10 MOSFETs (L_g > 800 nm) with TiN/Ru gates is 68 mv/dec, which is the record low SS for InP channel MOSFETs.

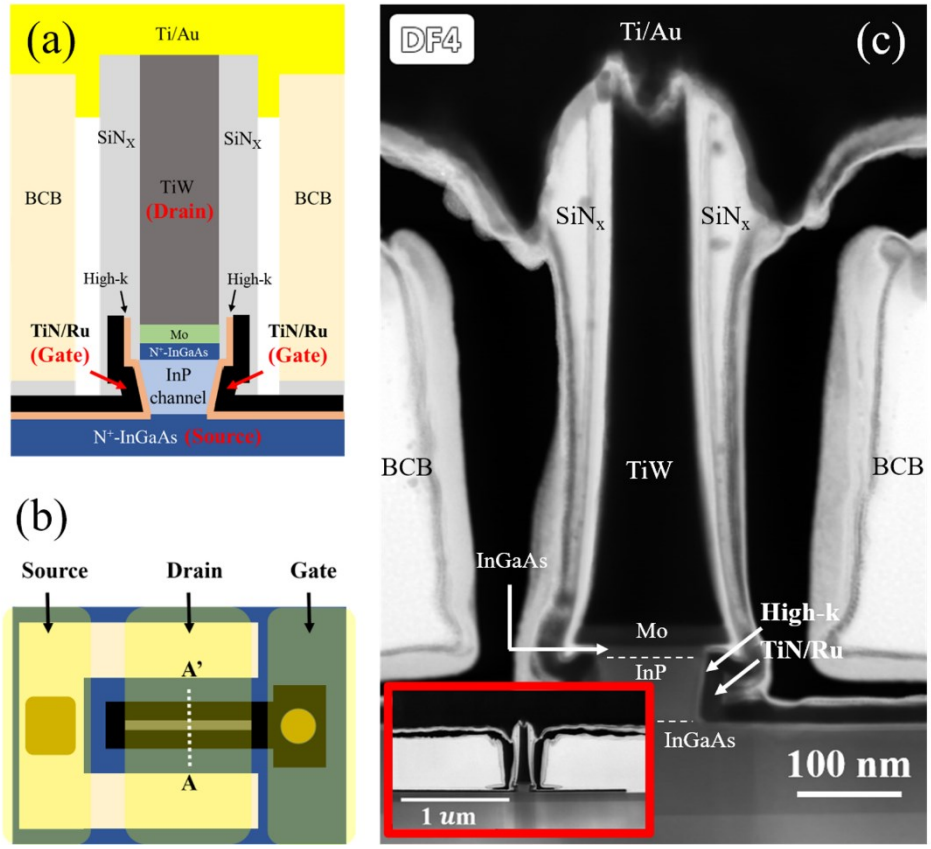

FIG. 5. The schematic (a) cross-sectional and (b) top view vertical MOSFET structure, and (c) the cross-sectional STEM image of the vertical MOSFET with TiN/Ru gate cutting along A and A', as indicated in (b). The P-InP channel length is 50 nm in this study, while the TiW/Mo drain metal stack is as thick as ~520 nm to facilitate contacting the drain. The inner plot in (c) is the image in a large field.

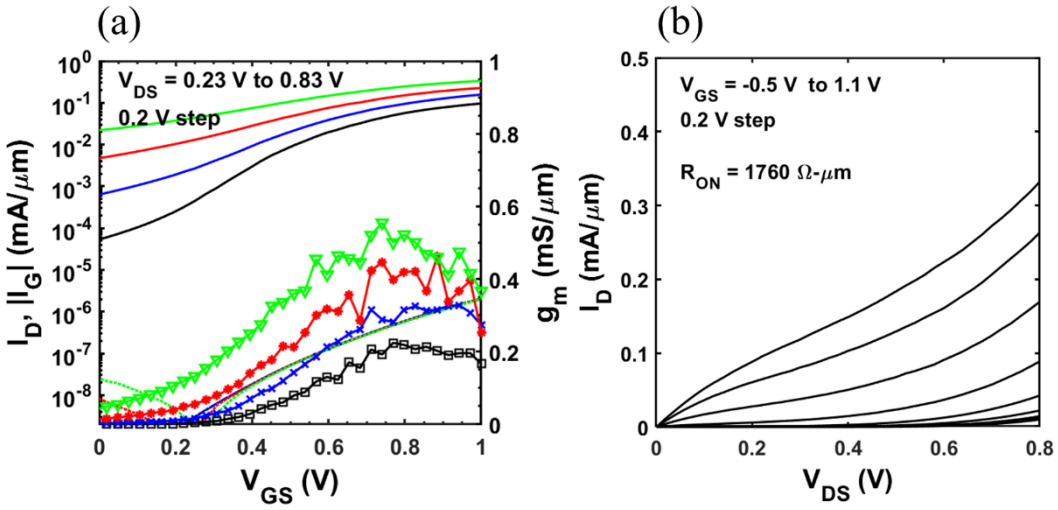

FIG. 6. The transfer (a) and output (b) characteristics for vertical MOSFETs with TiN/Ru gate. In transfer characteristic, solid lines, dotted lines, and symbolic lines represent I_D, $|I_G|$, and g_m, respectively. Low ratio between gate length and fin width (50 nm: 90 nm) results in a poor gate control and shows a strong short channel behavior. The peak g_m at V_{DS} = 0.6 V is ~0.42 mS/μm, which is closed to planar MOSFET with L_g = 50 nm as shown in Fig. 4(a).

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