Leveraging 3D Vertical RRAM to Developing Neuromorphic Architecture for Pattern Classification

Bokyung Kim
Electrical and Computer Engineering
Duke University
Durham, USA
bokyung.kim828@duke.edu

Hai Li
Electrical and Computer Engineering
Duke University
Durham, USA
hai.li@duke.edu

***Abstract*—The crossbar architecture with resistive random-access memory (RRAM) devices presents many advantages in realizing matrix-based computations and achieves success in neural network implementation. However, the rapid growth of network size demands even denser structures. In this paper, we investigate the neuromorphic hardware design based on the three-dimensional vertical RRAM (3D VRRAM) with an even/odd word line (WL) structure. The increased interconnects of VRRAM aggravate the chronic problems of the crossbar structure like the sneak path currents. We address this issue by attaining a balanced structure with high nonlinear RRAM devices. Furthermore, the impact of complicated signal routing and control due to the vertically stacked structure can be alleviated through architectural level optimization. A three-layer VRRAM structure is demonstrated for neuromorphic design by showing that 8×8-pixel images were successfully classified into three alphabet characters on this structure. The example design also verifies that the 3D VRRAM with even/odd WL structure is beneficial to acquire high area efficiency.**

***Keywords*-3D RRAM; 3D neuromorphic system; vertical resistive random access memory (VVRAM).**

I. Introduction

In recent years, machine learning has accomplished tremendous achievements, particularly at the algorithm and application levels. The development of hardware systems, however, falls far behind due to the lack of support in real-time learning and high power consumption of the conventional von Neumann architecture [1]. Neuromorphic systems that mimic the high parallelism of neuro-biological architectures have attracted much attention as a replacement of the von Neumann design. The use of emerging non-volatile memories (eNVM) as synaptic devices further advances the potential of the neuromorphic hardware design. Among all the eNVM technologies, the resistive random-access memory (RRAM) has been taken as one of the most promising candidates for its advantages of good scalability, fast switching speed, and inherent multilevel states [2], [3]. The simple two-terminal structure of RRAM naturally forms the two-dimensional (2D) crossbar array that enables large-scale parallel computations. In particular, the strength of performing vector-matrix multiplication (VMM) has accelerated the use of the 2D RRAM-based crossbar structure [4].

As neural networks have been rapidly evolving, even denser structures are demanded to match the ever-growing size of neural network models. As such, three-dimensional (3D) crossbar arrays are emerging to substitute the use of 2D arrays. Comparing the two common types of 3D structures — horizontally stacked 3D RRAM (HRRAM) and 3D vertical RRAM (VRRAM) [5], [6], VRRAM is considered to be more promising for neural network deployment, mainly because of its high bit-cost scalability [7], [8].

According to the shape of stacked word lines (WLs), 3D VRRAM is usually organized in two ways: *the plane WL structure* and *the even/odd WL structure*. The former adopts an entire metal plane as a WL and stacks multiple WLs vertically. Due to its simple structure, the 3D VRRAM with plane WL structure has been investigated for deploying machine learning algorithms [8]–[10]. The even/odd WL 3D VRRAM uses the comb-shaped plane WLs, which can be obtained by processing an additional etch step on the plane WL structure. A previous study [11] showed that the even/odd WL 3D VRRAM can contain doubled cell bits than the WL plane structure, indicating a high potential in neural network implementation. However, the split WLs increase the interconnect lines, which necessitate a sophisticated control mechanism to cell accesses and exacerbate the sneak path issue. For this reason, the application of the 3D VRRAM with even/odd WL structure is remarkably lacking.

In this work, we explore the neuromorphic design based on the 3D VRRAM with the even/odd WL structure by considering the structural features. The split even/odd WLs are used to represent the synapses and connected to the positive/negative lines of current-sense amplifiers, which generate a corresponding result after computing. A balanced structure to avoid elongating the sneak leakage path is attained by arranging inputs/outputs in view of 3D architecture. Instead of including additional devices to alleviate the sneak path issue, we leverage the high nonlinearity of Ta_2O_5 RRAM. Furthermore, we define a weight adjustment method to harmonize with the use of even/odd lines and devise a sequential operation to ensure to program only intended cells.

The proposed design enables a modified reinforcement learning algorithm to be directly executed on the 3D hardware system. In the paper, we present a design example of classifying 8×8-pixel images into three alphabet characters on the structure. Compared to implementation based on the 2D crossbar array, our design achieves $6\times$ improvement in area density. To evaluate the design approaches, the impact of the sneak path currents is analyzed. The analysis verifies the effectiveness of the even/odd WL structure for neuromorphic system implementation.

II. RRAM & 3D VRRAM

Shortly after nano-scale thin-film structures were discovered as *memristors* that had been missed for long, researchers noticed its analogy to the biological synapse [12]. Since then, there have been extensive studies on developing memristor devices (a.k.a. resistive memory or RRAM) toward electric synapses [13], [14]. For example, early exploration by M. Hu et al. [4] showed that the synaptic weighting function, which is abstracted as VMM in neural network models, can be naturally realized through RRAM crossbar arrays based on Kirchhoff's Law.

Practical designs, however, need to deal with many non-ideal properties, such as nonlinearity of device characteristics, signal degradation induced by IR drops, limited data precision, etc. In particular, using multiple binary RRAM devices to represent one synaptic weight has been adopted in many designs [8], [10]. Such an approach promises the high data precision while dramatically degrading the design efficiency. The situation could become even more severe with the ever-growing size of neural networks and associated increasing computation requirements. On the one hand, researchers attempt to reduce the model size through algorithm level techniques like sparsification [15]. On the other hand, continuous efforts have been taken for improving array density and innovating circuit and architecture designs. One of the important approaches is developing 3D RRAM structures to boost area efficiency of neuromorphic systems.

A straightforward way of building 3D RRAM is to stack multiple 2D arrays vertically, i.e., HRRAM. However, it is hard to fabricate such a structure when considering the alignment across layers. Another concern is the cost of the lithographic process, which is proportional to the number of layers. In contrast, the fabrication of multilayer in 3D VRRAM can apply a single critical lithography and etch step regardless of the number of layers by punching through the layers at once [7], [16].

In practice, there are two commonly reported 3D VRRAM structures: *3D VRRAM with plane WL structure* and *3D VRRAM with even/odd WL structure*. As depicted in Figure 1, unlike the 3D VRRAM with plane WL structure that uses an entire metal plane for a WL, the even/odd WL design divides a WL plane into two comb-shaped WL branches, *even* and *odd*, respectively illustrated in orange and blue horizontal lines in Figure 1(b). Memory cells denoted by the small orange or blue portion of vertical pillars are sandwiched between WLs and vertical pillar electrodes (in yellow color). Connecting the vertical pillars to bit lines (BLs), transistors controlled by select lines (SLs) are used to switch-on/-off the pillar electrodes. BLs organized in an orthogonal direction to SLs are used to feed inputs to the vertical pillars. The interplay between BLs, SLs, and WLs enables the random accesses to all the memory cells.

Comparing to the plane WL, the even/odd WL structure requires an additional etch step, but it can integrate twice the number of cells under the same performance constraint [11]. Thus the latter design is more preferable for the neuromorphic designs. Compared with the 2D crossbar, the complicated interconnection of 3D VRRAM makes the design more challenging, mainly due to the following two issues: (1) when programming target cells, non-target cells that share the same lines with the target cells are more vulnerable to be affected; and (2) the sneak leakage path per area increases. As such, 3D VRRAM requires more carefully designed operations.

III. The Proposed Design Method

Despite outstanding area efficiency of the 3D VRRAM with even/odd WL structure, its use for neuromorphic systems is notably lacking. This is because a misplanned control interface could cause unintentionally programming non-target cells and the aggravated sneak path in 3D could degrade learning accuracy. In this study, we propose a hardware design to minimize the side effects induced by the increase of interconnects through a more balanced structure along the three orthogonal directions (WL, BL, and SL), high nonlinear devices with an optimized voltage applying method, and an operation sequence for *in situ* training.

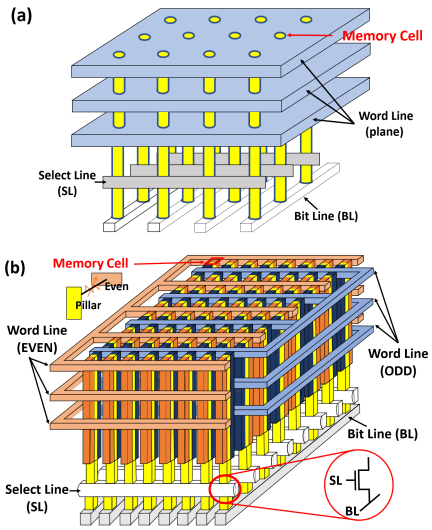

Figure 1: The illustration of three-layer 3D VRRAMs: (a) the plane WL structure; (b) the even/odd WL structure.

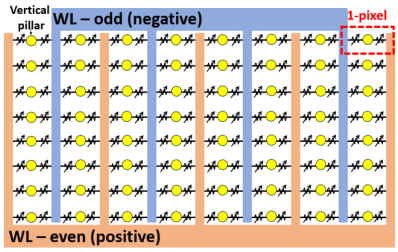

Figure 2: A layer of 3D VRRAM with even/odd WL structure.

A. Hardware Architecture

A 2D crossbar array conducts the matrix computation by applying an input vector to rows and collecting the output from columns. A great number of input parameters with developed neural networks drastically augment the number of the rows, in contrast with the bounded number of columns. Such an unbalanced structure aggravates the extension of the sneak leakage path in 2D crossbar-based designs [9]. Here, we propose to feed input data through the vertical pillar electrodes and detect the output at the WLs. The approach leads to a more balanced array configuration on layers, i.e., similar row and column lengths, which helps reduce the elongated sneak path.

We use each layer of the 3D structure to denote one class of information. As a physical ReRAM device can express only a positive value, two memory cells on a layer are paired to represent one synaptic weight that could be positive or negative, as illustrated in Figure 2. Accordingly, a set of the even and odd WLs is respectively fed to the positive and negative inputs of a sense amplifier to generate an output. When a current sense amplifier of the layer generates a spiking voltage by a certain input, the input is labeled as the class of the layer.

In previous 2D crossbar-based designs, the one-transistor-one-RRAM (1T1R) or one-selector-one-RRAM (1S1R) structure has been widely adopted in memory cells to alleviate the sneak path issue. These structures are not suitable for 3D VRRAM due to the high complexity of 1T1R and the possibility of the short-circuit connection in vertical pillars induced by 1S1R [17]. Alternatively, ReRAM devices with a highly nonlinear I-V (current-voltage) characteristic are employed to reduce the impact of sneak path current. In the following study, the Ta_2O_5 device is adopted, while the proposed design method can apply to other ReRAM devices with high nonlinearity.

B. RRAM Device with High Nonlinearity

We adopt the generalized RRAM modeling method and code the I-V characteristic of the Ta_2O_5 device in Verilog-A for the HSPICE simulation. According to [18], the root mean square error is set below 7% when modeling the characterization data of device structures. The mathematical function set of our modeling is summarized in Equations (1∼6) and the related parameters are shown in Table I.

In our modeling, the current through the device at time t, $I(t)$, is a hyperbolic sine function of its excitation voltage $V(t)$, to implement the threshold effect. The variable b is used to control nonlinearity, which shall be sufficiently large for devices of interest. $I(t)$ is also related to the state variable $x(t)$, which directly affects the conductance and can be taken as an index of the weight state. As such, $I(t)$ can be calculated by

$$I(t) = \begin{cases} a_1 x(t) \sinh(bV(t)), & V(t) \geq 0 \\ a_2 x(t) \sinh(bV(t)), & V(t) < 0 \end{cases}. \quad (1)$$

The change of the state variable over time depends on two functions, $g(V(t))$ and $f(x(t))$, such as

$$\frac{dx}{dt} = g(V(t)) \cdot f(x(t)), \quad (2)$$

where $g(V(t))$ denotes the threshold effect. The positive and negative threshold values are set by V_p and $-V_n$, respectively. Only when $V(t)$ exceeds the threshold, the device can be programmed and its conductance is affected:

$$g(V(t)) = \begin{cases} A_p(e^{V(t)} - e^{V_p}), & V(t) > V_p \\ -A_n(e^{-V(t)} - e^{V_n}), & V(t) < -V_n \\ 0, & otherwise \end{cases}. \quad (3)$$

$f(x(t))$ is a function to oppress the change of x, when it is approaching the boundaries, defined by x_p and x_n. The function limits x between 0 and 1. When $V(t) > 0$, $f(x(t))$ is calculated by (4); otherwise, it is described by (5).

$$f(x(t)) = \begin{cases} e^{-\alpha_p(x-x_p)w_p(x,x_p)}, & x \geq x_p \\ 1, & x < x_p \end{cases} \quad \text{and} \quad (4)$$

$$f(x(t)) = \begin{cases} e^{\alpha_n(x+x_n-1)w_n(x,x_n)}, & x \leq 1-x_n \\ 1, & x > 1-x_n \end{cases}, \quad (5)$$

where

$$w_p(x,x_p) = \frac{x_p - x}{1-x_p} + 1 \quad \text{and} \quad w_n(x,x_n) = \frac{x}{1-x_n}. \quad (6)$$

Figure 3 shows that the I-V curve produced by our model fits well with experimental measurement data of the Ta_2O_5 RRAM device from [19]. We use this type of RRAM for an analog synaptic device and apply short and repeated voltage pulses to adjust weights. Because pulses are not calculated complicatedly to adjust the exact amount of the weights,

Table I: Ta_2O_5 RRAM modeling parameters in this work.

Variable	Value	Variable	Value
a_1	1×10^{-5}	A_n	1×10^{7}
a_2	1×10^{-5}	x_p	0.2
b	2.1	x_n	0.25
V_p	1 [V]	α_p	7
V_n	1 [V]	α_n	6
A_p	3×10^{6}	x_o	0.3

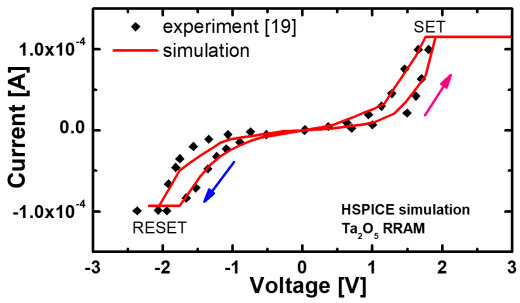

Figure 3: I-V characteristic of Ta_2O_5 RRAM device.

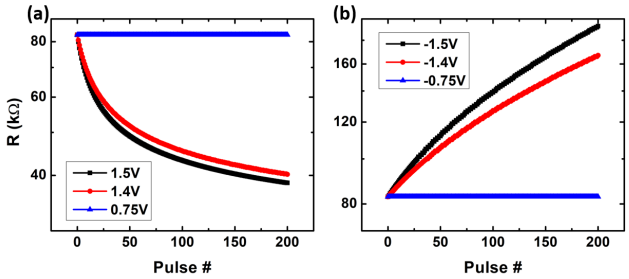

Figure 4: The resistance change when injecting (a) positive and (b) negative pulses.

such a voltage applying approach is conducive to simply using the nonlinear curve.

In the following simulations, we set $\pm 1V$ as threshold voltages to change the resistance state and use $\pm 1.5V$ as write voltages V_w in programming operations. Our simulation result in Figure 4 shows that according to the number of pulses, the device resistance gradually changes when a full range of voltage $V_w = \pm 1.5V$ was applied. Under this condition, the effective voltage amplitude across the device in our system was approximately $1.4V$. Lowering the voltage amplitude to $1.4V$ makes the change of resistance at a slightly slower but almost similar rate. A voltage that is lower than the threshold, e.g, $\pm 0.75V$, does not affect the resistance value as shown in Figure 4.

C. In Situ Training Operation

The weight intensification and weakening can be accomplished by adjusting the relative conductance of the two cells, as shown in Figure 5. When the conductance of the RRAM device connected to the even (positive) line increases and that of the cell to the odd (negative) line decreases, it is regarded as the weight intensification. The opposite conductance change indicates weight weakening. We apply $1.5V$ and $0V$ to the p and n terminals of RRAM to increase the conductance or the reverse voltages are applied to the opposite terminals to decrease the conductance.

Table II: The guide training method.

	***i*-th input**	**W(i, positive)**	**W(i, negative)**
Target	**1**	Increased	Decreased
	0	Unchanged	Unchanged
Non-Target	**1**	Decreased	Increased
	0	Unchanged	Unchanged

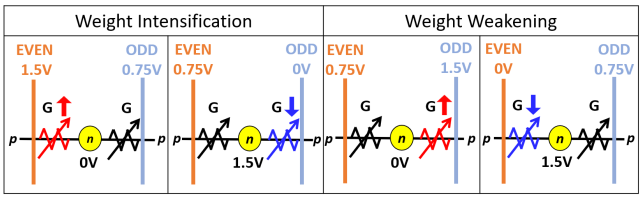

Figure 5: Cases of weight change when data 1 is given.

As a learning algorithm, we apply the *guide training algorithm*, which is a modified reinforcement algorithm for training [20]. The algorithm employs the feature of Hebbian learning, where the weight adjustment is determined based on a correlation between an input and output pair. The training induces a spike of the predefined neuron in accordance with an input by intensifying the target neuron weights and weakening the non-target neurons repeatedly. Such a repetitive weight change method accords with our voltage applying approach of the analog devices and thus is suitable for the hardware implementation with analog synaptic devices.

An input is composed of a vector of binary data, in which the black and white pixels are denoted by 1 and 0, respectively. As shown in Table II, the training process increases or decreases the conductance of black pixels. The weights associated with white pixels are not affected by the weight change. Additionally, the conductance of the even line in the target layer can be further adjusted up to strengthen its weight value.

Figure 6 illustrates our voltage applying sequence example when training Layer 1, the top layer in the structure. As a part of intensifying Layer 1 and weakening other layers, the even line conductance of Layer 1 and the odd line conductance of other layers need to increase. At step 1, these conductance increases are concurrently executed by applying $0V$ to the pillar electrode and $1.5V$ to the even line of Layer 1 and the odd lines of the non-target layers. Likewise, adjusting the conductance downward is also carried out concurrently (Step 3). As aforementioned, Step 2 can be included to further strengthen the target layer.

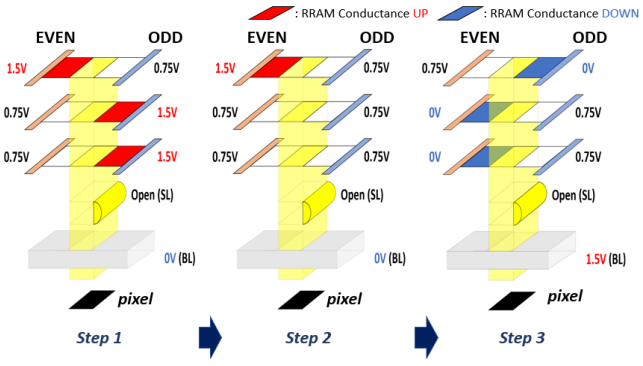

Figure 6: The voltage applying method to adjust the conductance of devices at the cell level. This illustration assumes that the first WL is the target layer.

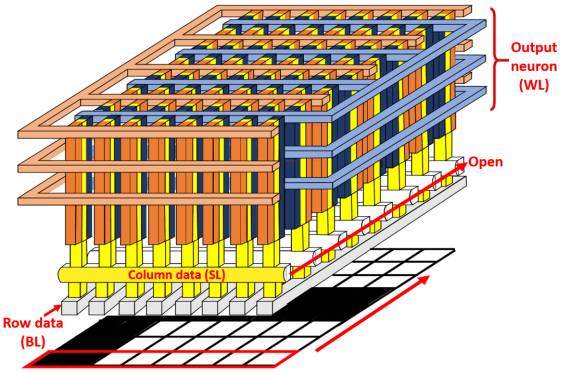

Figure 7: Sequential operation in even/odd 3D VRRAM.

The training steps are sequentially operated by SLs to avoid affecting non-target cells when programming target cells. When an input image is a T-shape image, for instance, the first step is turning on only the first SL, as illustrated in Figure 7. Consequently, only the first column data, i.e., 110000 in this case, are supplied to the BLs. Meanwhile, voltages are applied to the first WL to spike the layer for T, and the opposite voltages are simultaneously applied to other WLs. After completing the writing of the first column, the operation moves to the rest columns.

The computing operation is executed similarly as the writing operation, except for that the applying voltage for data 1 is $1V$ and for data 0 is $0V$.

IV. Result and Discussion

Case study setup. This study takes an example of classifying 8×8-pixel black/white images into three characters (T, X, and V) in the even/odd 3D VRRAM. We used HSPICE for the circuit simulation, and implemented devices and voltage controllers by Verilog-A. The original image data set consisted of the original images of three characters. Training was conducted with 300 sets of original images, then testing was executed five times with defective images. Five testing image sets were consisting of 1-, 2-, 4-, 8-, and 16-pixel flipped image sets as shown in Figure 8. We randomly inverted pixels and each testing image set has 200 images that possibly contain duplicated images.

Independent programming. To examine whether weights of memory cells are adjusted independently during the

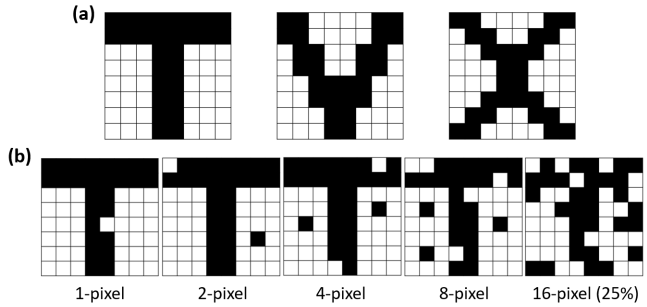

Figure 8: (a) Training and (b) testing images.

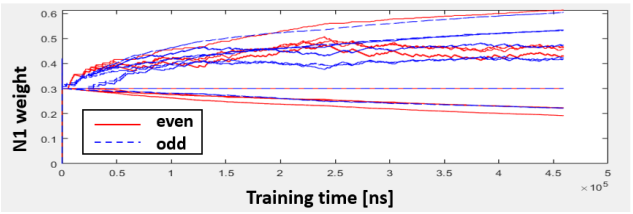

Figure 9: The weight change of Layer 1 over time during training.

training, we plot the weight changes of all the cells. Figure 9 presents those in Layer 1 as an example; red lines stand for device weights in the even branch, while blue lines show device weights in the odd branch. The figure shows that as the training process proceeds, the weights tend to saturate toward an appropriate value determined by the learning process. Similar trends of the weight changes are observed in other layers too.

Testing accuracy. Figure 10 shows accuracy according to the number of flipped pixels. Although the image with more pixels flipped shows lower accuracy, accuracy is 100% until four pixels of 64 pixels are inverted. When the error was 25% of input images, the test result was 98.46%. This result verified that the performance of our design is reliable.

Area comparison. The required area of the even/odd WL structure is much smaller than that of the 2D crossbar array. In [21], processing 3×3 images demands a 9×6 2D crossbar structure. For 8×8 images, 2D architecture with 1T1R or 1S1R needs a 64×6 array and one cell requires at least $4F^2$, where F denotes the feature size. Thus, the overall design area could be $1536F^2$. In contrast, 3D VRRAM requires a $8\times16\times3$ structure to process 8×8 images. When using the 3D VRRAM with plane WL structure, whose cell also requires $4F^2$, the plane area may occupy $512F^2$ [10]. The 3D VRRAM with even/odd structure occupies only $256F^2$ because of its twice density than that of the 3D VRRAM with plane WL structure [11], [17]. The 3D VRRAM with even/odd WL structure shows high area efficiency with the $6\times$ smaller areas than that of 2D crossbar array.

Impact of sneak path current. To figure out the impact of the sneak path, we built a subarray of the even/odd 3D VRRAM and set the same condition up on the subarray as the control group. Because the testing (computing) was also

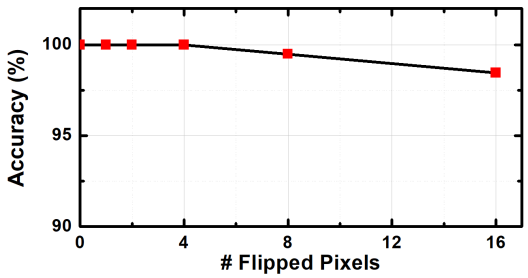

Figure 10: Accuracy according to the number of flipped pixels of images.

executed SL by SL like the training procedure, the subarray size was 8×2. We then measured and compared the currents from the subarray and the corresponding SL of the original system. The results showed only a slight difference: the current of the original system is about $2\mu A$ less than the current of the subarray only, as the latter one is not affected by the other parts of the array. This small difference indicates that the entire system is immune to the sneak path, thanks to the use of the device nonlinearity and the structural features.

V. Conclusion

In this study, the 3D VRRAM with even/odd WL structure was explored for the neuromorphic hardware system. Although the 3D VRRAM with even/odd WL structure is advantageous to improve area efficiency, exploration of the structure is remarkably lacking, due to the comparatively complicated inner organization. We devised an operation scheme to deploy high area efficiency of the even/odd structure, exploring ways to avoid the two largest problems, the sneak path current and writing unintentionally. This work demonstrates the even/odd structure improves the area efficiency. Furthermore, the high accuracy proves that using the 3D even/odd structure for the neural network is reliable. As a result, this study shows the capability of the 3D VRRAM with even/odd WL structure for neuromorphic systems and expands the area of the 3D neuromorphic hardware system.

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