Gamma-Ray-Induced Error Pattern Analysis for MLC 3-D NAND Flash Memories

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***Abstract*— This article analyzes the data corruption pattern in the shared pages of multi-level cell (MLC) 3-D NAND memory under ionizing radiation from a Co-60 gamma-ray source for up to 20 krad(Si) dose. The results show that the radiation-induced error pattern between the shared pages follows a unique correlated behavior. We also find that the error locations within a given page remain uncorrelated, meaning that the occurrence of an error does not force a cluster of errors under ionizing radiation.**

***Index Terms*— 3-D NAND flash, error rate, ionizing radiation, memory controller, multi-level cell (MLC), shared pages, single-event exposure, total ionizing dose.**

I. Introduction

THE radiation tolerance characteristics of commercial off-the-shelf (COTS) 3-D NAND flash memory is a topic of great interest for several applications including nuclear, defense, and the space industries [1]. While 3-D NAND offers high-density, high-capacity, and low-cost storage solutions in a small form factor, it suffers from radiation-induced data corruption issues [2]–[5]. For a given technology node, a higher data corruption rate is observed as we go from a single-level cell (SLC) to a multi-level cell (MLC) and triple-level cell (TLC) NAND [6]. However, in terms of bit density and cost, TLC and MLC memory chips are more attractive compared to SLC memory [7]. Since MLC NAND provides a good balance between density and radiation reliability [4], there is a great economic interest in using MLC NAND instead of SLC NAND in the low/moderate radiation environment (e.g., low-Earth-orbit satellites).

In the MLC NAND flash memory, each memory cell holds two bits of information. Hence, the memory cells in MLC NAND have four different logic states. We illustrate the four logic states using four different flash memory cells in Fig. 1(a), where the memory cells are connected to a given word line. Typically, there are thousands of memory cells connected to the same word line. The number of memory cells belonging to a given word line determines the logical page size of the memory chip. Since each memory cell stores 2 bits of information, there are two logical pages sharing the same word line. The most significant bit (MSB) of the logic states of all the memory cells connected to a given word line forms the logical MSB page. Similarly, the least significant bit (LSB) of the logic states of the memory cells from the same word line forms the logical LSB page. The details of the logical addresses for the shared pages are provided in the datasheet of the corresponding chip.

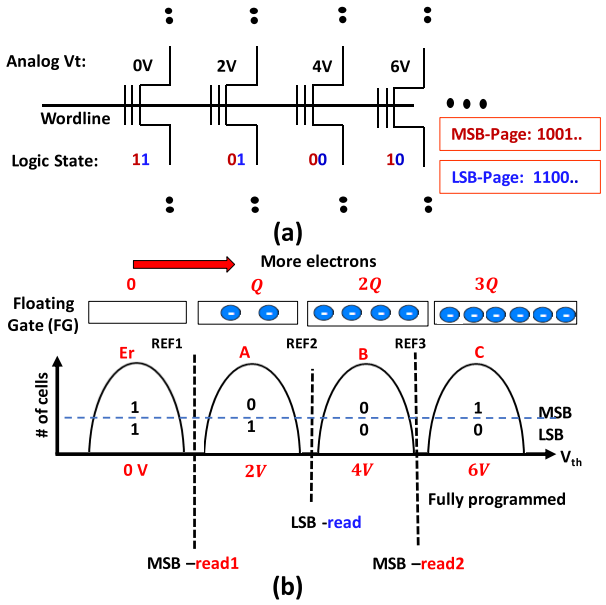

Fig. 1. (a) Arrangement of NAND flash memory cells connected to a single word line. (b) Cell threshold voltage distribution for MLC NAND.

The logic state of a memory cell is decided by its analog threshold voltage, V_t, which is controlled by charge injection on the floating gate during program operation. Fig. 1(b) shows the representative analog threshold voltages corresponding to the four different logic states. There are variations in the analog V_t values of the cells representing a given logic state. Several physical reasons including program noise, cell-to-cell process variation, and read noise are responsible for the cell V_t variation [7]. Hence, the cells corresponding to a given logic

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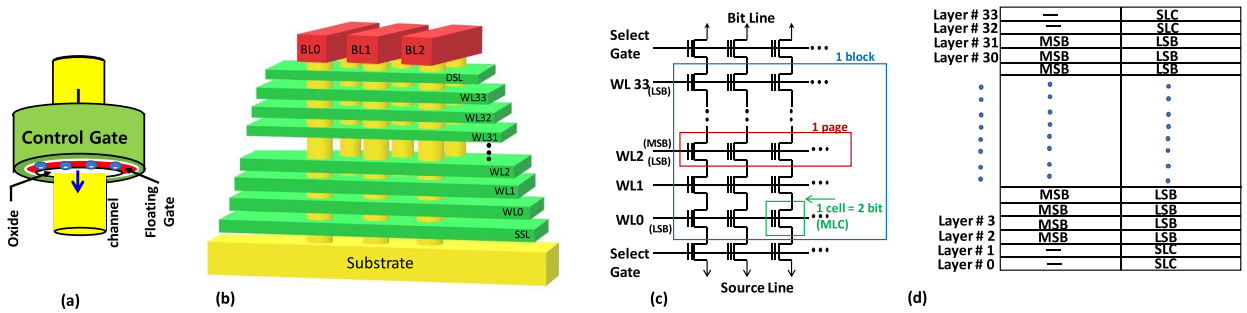

Fig. 2. (a) Schematic of a 3-D NAND flash memory cell. (b) Physical diagram of a NAND flash memory array. (c) Circuit diagram of a NAND memory block (reproduced from Ref. [16]). (d) Logical (LSB and MSB) page distributions across different vertical layers of 3-D NAND.

state show a distribution of V_t values, as illustrated in Fig. 1(b). In addition, Fig. 1(b) shows three different reference voltages that are used to decide the logic state of a cell. There is only one reference voltage required to read the LSB page bits, whereas two reference voltages are needed for the MSB page read [8]. Note that transition from the highest V_t state to the adjacent one (from C to B) will cause a failure in the MSB page but not in the LSB page. Similarly, the transition from the state B to A will result in a failure in the LSB page but not in the MSB page. Since the highest V_t state loses charge more quickly than the other states during total ionizing dose (TID) irradiation [4], [9], we expect to find more failures in MSB pages compared to the corresponding LSB pages.

Several interesting studies have been carried out on the radiation effects on MLC 2-D NAND for both single-event effects (SEEs) and TID response [6], [10]–[14]. Previous studies demonstrated that MLC NAND is more susceptible to data corruption compared to SLC NAND. Additionally, Gerardin *et al.* [14] showed that all the program states of MLC NAND incur bit errors by performing TID-induced error analysis in 25-nm 2-D MLC NAND flash from Micron. Ingalls *et al.* [11] showed a novel method of using logical decode to convert MLC NAND to SLC-like memory to increase its radiation tolerance. Unfortunately, the logical decode method does not apply to the state-of-the-art 3-D MLC NAND as modern MLC chips use internal data randomization before writing user data on the memory array. Additionally, most of the previous studies on MLC NAND were done on 2-D NAND technology which is fundamentally different than the 3-D NAND technology. Thus, it is very important to analyze the radiation susceptibility of MLC memory for 3-D NAND technology before it is adopted for high-density data storage application in a radiation-prone environment.

In this article, we perform radiation-induced error analysis of COTS 3-D MLC NAND memory from Micron Technology. Special emphasis is given on the relative radiation tolerance characteristics of the LSB and MSB pages of the MLC memory. We analyze the TID-induced error characteristics on six different 3-D NAND chips of the same specifications to make our conclusions statistically robust. The details on the chip specifications, the experimental setup, measurement procedure, gamma irradiation conditions, and the data collection method are discussed in Section II. Section III demonstrates the experimental evaluation results and Section IV concludes the article.

II. Experimental Details

A. Device Details

The details of the 3-D NAND fabrication process and cell structure were given in our previous publication [15]. For the sake of completeness, we reiterate the essential features of 3-D NAND memory in this section. Fig. 2(a) shows the device structure of a 3-D NAND flash memory cell, which is essentially a gate-all-around metal oxide semiconductor field effect transistor (MOSFET) with a floating gate. The memory cell is in the programed state (logic 0) when electrons are stored on the floating gate, whereas it is in the erased state (logic 1) when there are no electrons on the floating gate. Fig. 2(b) shows the physical structure of the 3-D NAND memory array. The green layers are the word lines, and the vertical pillars are memory holes that contain the channel of the flash memory cells. Fig. 2(c) shows the circuit diagram of the memory cell arrangement in a NAND flash memory block. Each memory block consists of a fixed number of memory pages. The cells in each memory page are electrically connected through a metal word line. Word line acts as the control gate of the memory cells. Each column (or string) of cells in a block is connected to a different bitline. Memory-read and program operations are performed at the page granularity, whereas erase is performed at the block granularity. Any flash cell that is set to a logic "0" by a program operation on a page can only be reset to a logic "1" by erasing the entire block.

We used COTS NAND flash memory chips from Micron Technology for evaluating the radiation response. The part number for the 3-D NAND memory chips was MT29F256G08CBCBBWP-10: B, which was 256-GB MLC memory chips from Micron. Six different chips were used to improve statistics. Each 3-D memory chip contains 2192 logical blocks, where each block consists of 1024 logical pages of size 18,592 bytes (16,384 bytes of user data with 2208 bytes of error correction codes). The logical pages of a 3-D NAND memory block are distributed across the vertical layers of the 3-D structure. Ideally, each vertical layer should hold 32 logical pages if the pages are uniformly distributed across the 32 physical layers (a total of 1024 pages per block). However, according to the datasheet [16], the chip under test has nonuniform page distribution, especially on the edge layers (top two and bottom two layers) as illustrated in Fig. 2(d). Fig. 2(d) shows the layer-dependent page distribution for a specific sub-block structure (there are a total of 16 identical

sub-blocks in a memory block) in the memory array, and Fig. 2(d) shows the shared and unshared page structures for the 34 different layers. Note that of the 34 physical layers in the 3-D stack, the bottom as well as the top two layers have non-shared memory pages, similar to SLC technology. In other words, the edge layer memory pages operate as SLC storage, while the remaining 30 layers operate as the MLC storage. Since the manufacturer is aware of the intrinsic reliability issues on the edge layers, they designed the edge layers to operate in SLC-type memory storage, which is fundamentally more robust compared to MLC storage.

B. Gamma-Ray Irradiation

The flash memory chips were irradiated using Co-60 sources to evaluate their TID response. The irradiation was carried out at Sandia National Laboratories Gamma Irradiation Facility [17]. The chips received a TID up to 20 krad(Si) at a dose rate of 18.5 rad(Si)/s. If not otherwise stated, all doses in the following are expressed as absorbed dose in silicon. Gamma irradiation was performed on the packaged devices (TSOP) with all the pins grounded. The unpowered state is a common use condition for non-volatile memories, which are designed to retain data without any external power. The unpowered state irradiation ensures minimal damage to the peripheral circuitry (e.g., charge pump) of the chip, which allows us to explore radiation effects mainly on the memory cells. The direction of gamma rays during irradiation was perpendicular to the flat surface of the chip. The entire chip in unlidded condition went through gamma irradiation.

C. Measurement Setup and Procedure

To interface the raw NAND chip with the computer, we used a custom-designed hardware board. The board includes a socket to insert the NAND flash chip and an FT2232H mini module from Future Technology Devices International (FTDI) [18] to interface the memory chip with a computer through universal serial bus (USB) connection. The FT2232H mini module enables USB to universal asynchronous receiver/transmitter (UART) interface. The hardware setup allowed us to access the raw memory bits without any error correction. The hardware setup was not exposed to gamma radiation. It was only used to write/read the memory chips that were irradiated. Before sending the chips for radiation exposure, we wrote a known random data pattern on four to six memory blocks in each chip. We read all the blocks immediately after writing data. We then exposed the NAND memory chips to gamma radiation. Finally, we read the data from the corresponding memory blocks and then computed the failed byte count (FBC). The time gap between data write and irradiation was 3–4 h and the time gap between irradiation and data read was around an hour. We monitored a reference (unirradiated) chip to observe any data retention-related errors and we found little to no increase in FBC within a week's timeframe. On the irradiated chip, we observed some relaxation effects within a week where we found that FBC reduced slightly after a week.

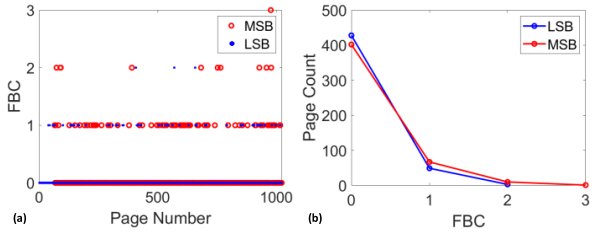

Fig. 3. (a) FBC comparison between LSB (blue symbols) and MSB (red symbols) pages before radiation exposure. (b) Frequency polygon for MSB and LSB FBC for all pages in a block.

III. Experimental Results and Discussion

We have performed the FBC analysis for the 3-D MLC NAND chip following gamma irradiation. Data are read from the chip byte by byte and are compared to the original random data pattern to determine the FBC. In the following sections, we compare the FBC from the LSB and MSB pages for different gamma-ray exposure conditions.

A. Comparison of LSB–MSB Pages Before Irradiation

First, we compare the FBC in the LSB and MSB pages for the pre-irradiation condition. Fig. 3(a) shows the FBC on 1024 logical pages of a given memory block just after writing data, and Fig. 3(b) shows the corresponding frequency polygon plot. The frequency polygon plot in Fig. 3(b) illustrates the histogram representation of the number of pages for the corresponding FBC on the x-axis. For the clarity of comparison, we do not show the histogram bars, so the overlays do not hide each other. Instead, we construct the frequency plot using the bin centers and the page count in that bin for the corresponding histogram. Here, a bin width of 1-FBC is used with the bin centers 0, 1, 2, and so on. Red corresponds to MSB pages and blue corresponds to LSB pages. We find that FBC is very low (FBC $<$ 5 per 18 kB) in all the pages before irradiation. The few errors observed before irradiation are inherent in high-density MLC NAND due to read noise [19] associated with very minimal voltage margins between the programed states. We did not observe a significant difference between the FBC of the LSB and MSB pages before irradiation. The inherent FBC remains almost the same or slightly increases over the period of a few months while kept at room temperature.

B. Post-Irradiation FBC Comparison of the LSB and MSB Pages

In this section, we compare the FBC in the LSB and MSB pages on the irradiated chip. Fig. 4 (a)–(f) summarizes the experimental results; the plots (a)–(c) show the results for TID of 10 krad(Si), whereas the plots (d)–(f) represent the same parameters for TID of 20 krad(Si). In Fig. 4(a), we plot the FBC of the LSB (blue symbols) and MSB (red symbols) pages of the same memory block after 10 krad(Si) of TID exposure. We find that the MSB pages consistently incur slightly higher FBC compared to the corresponding LSB pages. To make the comparison statistically meaningful,

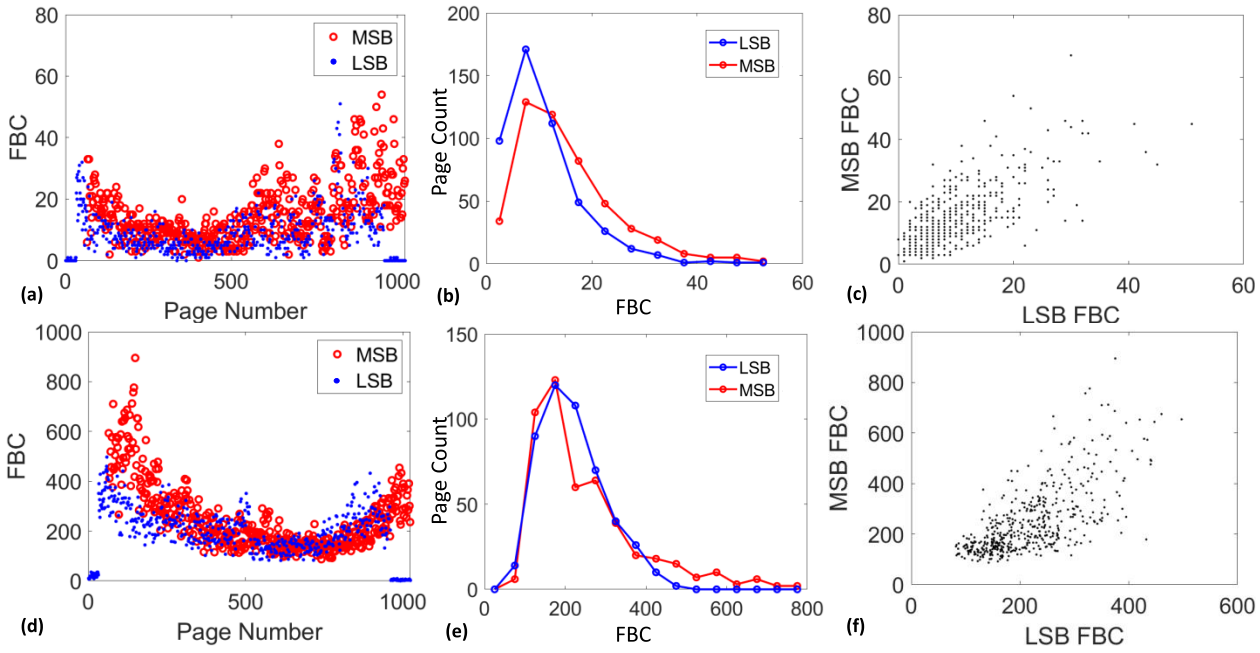

Fig. 4. (a) FBC comparison between LSB (blue symbols) and MSB (red symbols) pages after 10 krad(Si) of TID. (b) Frequency polygon for MSB and LSB FBC for all pages in a block after 10 krad(Si) of exposure (bin size 5). (c) Correlation between FBC of MSB and the corresponding LSB pages. (d)–(f) Similar plots for 20 krad(Si) of TID exposure. Bin size of 50-FBC is used for the frequency polygon in (e).

we show the frequency polygon plot of FBC distribution corresponding to the LSB and MSB pages in Fig. 4(b). We find that the mean FBC for the MSB pages to be 14.86 with a standard error of 0.44, and the LSB pages with a mean of 10.09 and a standard error of 0.33. Next, we compare the FBC of the LSB pages and the corresponding MSB pages using the correlation plot in Fig. 4(c). Note that every LSB page has a unique MSB page sharing the same memory cells. The correlation plot of Fig. 4(c) clearly shows that FBC is strongly correlated (correlation coefficient of 0.70) between the two page types with greater than 99.99% confidence. In Fig. 4(d), we compare the FBC on the LSB and MSB pages for a higher TID of 20 krad(Si). The MSB pages have a mean FBC of 251 with a standard error of 6.16, compared to a mean of 218.7 for the LSB pages with a standard error of 3.7. As before, the FBC on MSB pages remains higher [Fig. 4(e)] and is significantly correlated with that of the corresponding LSB pages [Fig. 4(f)], with a correlation coefficient of 0.69, with greater than 99.99% confidence. The FBC correlation implies that if an LSB page is erroneous, the corresponding MSB pages will also be erroneous to a similar degree.

Another interesting observation, shown in Fig. 5, is the FBC ratio between the MSB and LSB pages. We find that the FBC values between the MSB and LSB pages are not only correlated, but also maintain an average ratio in the range of 1.2–1.5. Fig. 5 shows the frequency plot of MSB/LSB FBC ratios obtained from six different chips; three chips received the TID of 10 krad(Si), and the other three chips received the TID of 20 krad(Si). We find that the average FBC ratio between the MSB and LSB pages remains in the range of 1.2–1.5 across different chips. Thus, we confirm that multiple

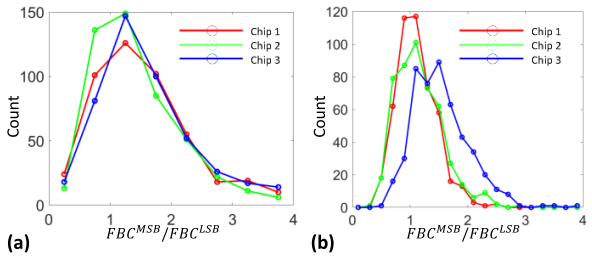

Fig. 5. Frequency plot of the FBC ratios in MSB to those in the corresponding LSB pages for random data pattern for (a) 10 krad(Si) and (b) 20 krad(Si).

chips show similar behavior with respect to LSB and MSB page failures under ionizing radiation.

C. Model for FBC Comparison of the LSB and MSB Pages

The experimental data are very roughly explained by a simple probabilistic model, as shown in Fig. 6. The model essentially treats the memory cell as a capacitor [see Fig. 6(a)] and the radiation damage as reducing the floating gate charge by a combination of removal of floating gate electrons and screening them via uncompensated positive charges in the oxide [20]. Since the electric field in the oxide layers of the memory cell is a key factor for the charge loss during irradiation [21], the failure probability depends on the initial-state floating-gate charge ($Q_{\rm FG}$) that determines the field in the gate oxide ($E_{\rm ox}$). For example, consider a memory cell in the V_t state-C (or "10") which has more charge ($Q^C_{\rm FG}$) on the floating gate compared to the cell in the V_t state-B (or "00"). Fig. 6(a) compares the energy band diagram for these two cells under unbiased condition. For quantitative comparison, we assume $Q^C_{\rm FG} \approx (3/2)Q^B_{\rm FG}$, which is true

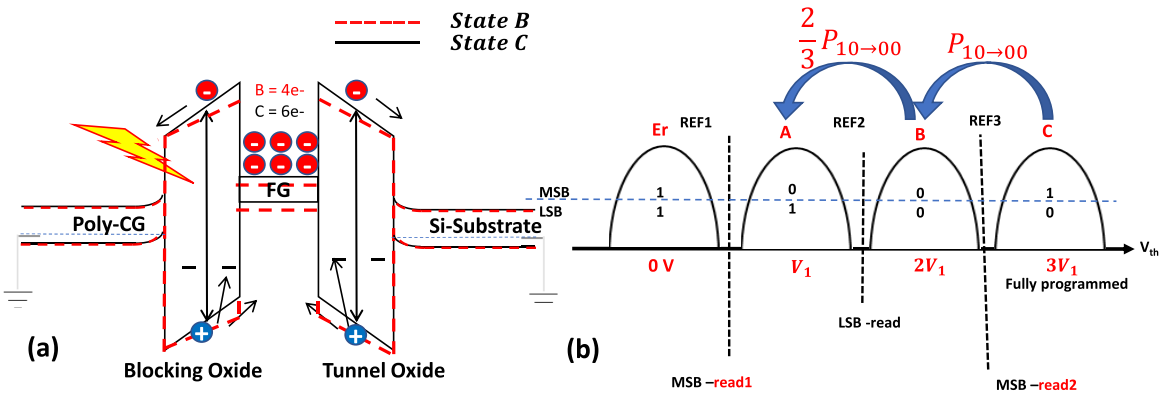

Fig. 6. (a) Energy band diagram of a floating gate transistor at unbiased condition. Solid lines represent energy bands for a cell in state-C, whereas the dashed lines stand for state-B. (b) Cell threshold voltage distribution for four different states in MLC storage. The simplified state transition probabilities are shown in the plot.

if V_t states are equally spaced on the voltage axis. Since field in the oxide layers is directly proportional to the charge on the floating gate at the unbiased condition of the memory array, the oxide fields in the state-C and state-B cells are related as follows: $E_{\text{ox}}^{C} \approx (3/2)E_{\text{ox}}^{B}$. Assuming TID-induced charge loss rate being directly proportional to the field in the oxide [21], the state transition probabilities after irradiation can be expressed as follows:

$$P(10 \to 00) \approx \left(\frac{3}{2}\right) P(00 \to 01). \tag{1}$$

Since the $10 \to 00$ state transition is an MSB fail and the $00 \to 01$ state transition is an LSB fail [Fig 6(b)], we can derive the following relationship for the FBC observed on the MSB and LSB pages:

$$\frac{\text{FBC}^{\text{MSB}}}{\text{FBC}^{\text{LSB}}} \approx 1.5. \tag{2}$$

Please note that (2) is based on certain assumptions as states below.

A1 We assume that TID effects will lower the cell threshold voltage from its pre-irradiation case. This assumption is based on the fundamental charge loss effects due to TID.

A2 We have neglected the V_t shifts for the cells in the "11" and "01" states. Since cells in these states have a lower charge on the floating gate compared to the cells in the "00" and "10" states, their oxide field will be significantly lower leading to negligible V_t change after TID irradiation. Indeed, previous work [4], [9] on V_t distribution measurement on both 2-D and 3-D NAND array after irradiation supports this assumption.

A3 Since the radiation dose is not extreme, we assume that radiation exposure will cause the transition of a state to its next lower V_t state. This assumption is verified from the measured data which shows that none of the cells has a failure in both LSB and MSB bits.

A4 We assume all the four V_t states have an equal number of bits and the V_t states are equally spaced over the voltage range.

Note that this ratio will vary from page to page due to process variation and electronic noise inherently present in the high-density memory array. Hence, Fig. 5 shows a spread in the observed MSB/LSB fail ratio. However, the average MSB/LSB fail ratio lies in the range of 1.2–1.5 for all the chips that we used in this work. Thus, the measured data supports the proposed simplified model and the underlying assumptions (*A1–A4*). Different flash memory manufacturers may design their chips with different amounts of voltage margins between memory states causing some deviation from this model. However, the correlation between the LSB and MSB fails will remain invariant for different memory chips as it is fundamentally tied with the data encoding process where both the LSB and MSB pages share the same set of memory cells.

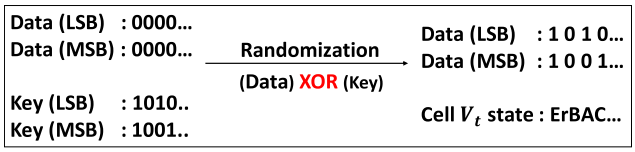

Fig. 7. Illustration of the data randomization process.

D. Internal Data Randomizer and Data Pattern Dependence

The FBC analysis presented in the previous section was obtained for a random data pattern. Random data were used in order to ensure that all four analog V_t states have equal proportions of bits irrespective of a data randomizing algorithm. The chip under test uses an internal data randomizer that randomizes the user data before writing them on the NAND array. Essentially, the randomizer performs a bit-by-bit XOR operation on the input data using an internal key in order to randomize the input data pattern. The goal of such data randomization is to ensure memory reliability by distributing the memory cells in all four analog V_t states. However, the data-encoding scheme as described in Fig. 1 using four different V_t states remains the same and hence our FBC analysis and the corresponding conclusions of the previous section remain valid even after data randomization. We illustrate the data randomization process in Fig. 7 using an all-zero data pattern. As an example, we assume two different keys for the LSB and MSB pages. In the absence of the data randomizer, all-zero

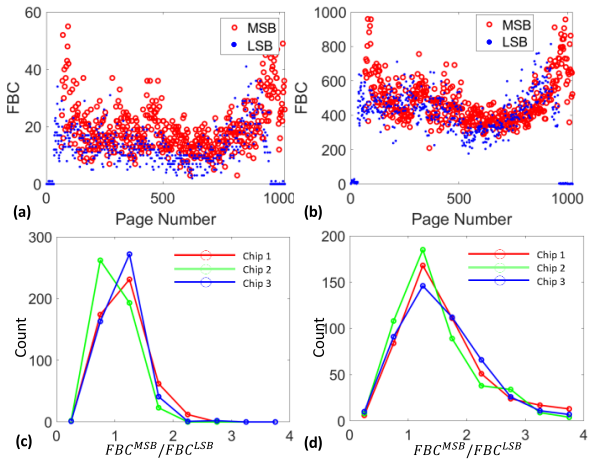

Fig. 8. Page-wise FBC for (a) 10 krad(Si) and (b) 20 krad(Si). Ratio of FBC in MSB and the corresponding LSB pages for all-zero data pattern for (c) TID = 10 krad(Si) and (d) TID = 20 krad(Si).

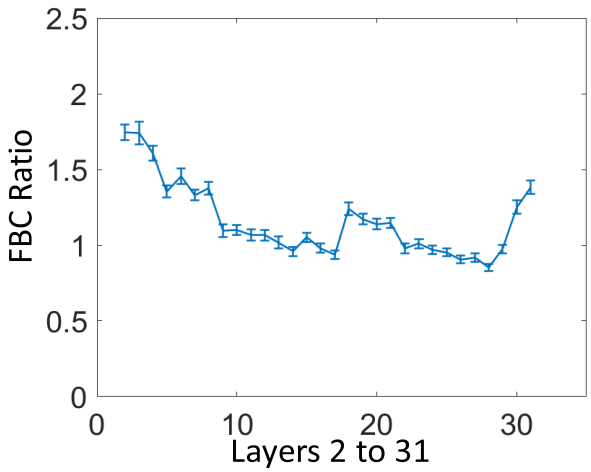

Fig. 9. Ratio of FBC in MSB and the corresponding LSB pages for the 32 different layers in 3-DNAND from six different chips.

data on both the LSB and MSB pages would lead to all cells being programed to the B-state. Due to data randomization, the exact cell V_t state will be decided by the randomization key, which will ensure an even more distribution of V_t states among the memory cells. An even distribution is good for cell endurance and reliability. Thus, randomization is an integral feature in the state-of-the-art NAND flash chip which not only enhances data security, but also ensures memory reliability.

Next, we illustrate the effects of data randomization by writing an all-zero data pattern in the memory array. Fig. 8 presents the FBC comparison between the LSB and MSB pages for the all-zero data pattern after irradiation. Fig. 8(a) and (b) shows the page-by-page FBC pattern for a 10 krad(Si) and 20 krad(Si) of TID, respectively. Note that the FBC values per page with an all-zero data pattern are comparable to the FBC values observed with a random data pattern in Fig 4. This illustrates the effects of data randomizer which ensures uniform FBC irrespective of the user data pattern. In the absence of a data randomizer, all-zero data would have shown significantly higher FBC on LSB pages and significantly lower FBC on MSB pages as all the memory cells were programed in the state-B of the V_t distribution. Such uneven FBC between memory pages is not ideal for error correction code (ECC) engines as it will increase the probability of uncorrectable read errors. Thus, data randomization improves data reliability by ensuring relatively uniform FBC across different memory pages. We have also analyzed the MSB/LSB FBC ratio for the all-zero data in Fig. 8(c) and (d). Since data randomization (depending on the efficiency of the algorithm) ensures the presence of all four V_t states in the memory array with an equal proportion of cells in each state, our model assumptions (Section III-C) hold good even for all-zero data, and hence the MSB/LSB FBC ratio predominantly lies in the range 1.2–1.5.

E. MSB/LSB Page FBC Ratio in Different Vertical Layers

Our previous work [15], [22] had shown a significant layer-to-layer variability under ionizing radiation due to a variation in geometric structure, causing a differential V_t-shift between different layers of the 3-D stack. The data shown in Fig. 4(a) and (d) essentially represent the page-to-page variability within a block which arises from the layer-to-layer variability. Here, we study the FBC ratio between MSB/LSB pages across the different vertical layers in a block. We explore this FBC ratio by taking six different blocks of data. The data is then split into 32 corresponding layers for each block. Upon plotting the FBC ratio for each corresponding layer and the corresponding error bars in Fig. 9, we see a "U"-shaped pattern, with the FBC ratio being much closer to 2 in the lower layers, close to 1.2 in the middle layers, and close to 1.5 in the top layers. The difference in the MSB/LSB FBC ratio across different layers could be due to different program V_t levels and read reference voltages in different layers of the 3-D structure. Since the exact program V_t levels are proprietory information, we speculate that the flash manufacturer introduced different program V_t levels across different layers to counter the geometric variations of the 3-D structure which might have resulted in different FBC ratios between the MSB and LSB pages across different layers.

F. Analysis of Error Location on the MSB/LSB Pages

In this section, we analyze whether there is any relationship between the error location of the LSB and MSB pages. The analysis process is illustrated in Fig. 10(a), where we show the byte position and the corresponding data values of the LSB and MSB pages in the hexadecimal format. There are 18 kB in a page, whereas only the first 9 bytes are shown in Fig. 10(a) as an example. We find that the fails in the LSB and the corresponding MSB pages almost never occur at the same bit position. This is true for all the chips that we analyzed in this work. Thus, we can conclude that even though the FBC values are correlated between the LSB and MSB pages, the fail locations of the LSB and MSB pages are not correlated. We also analyzed the number of bit errors per byte for the irradiated chips in order to confirm whether there is any clustering of error locations. We find that most of the error bytes have only one error bit. However, a few bytes have

(a)

Byte position	1	2	3	4	5	6	7	8	9	•••
LSB page	5F	3A	C1	18	80	1C	7D	A0	E2	•••
MSB page	40	E1	A4	D3	15	A1	2C	1B	70	•••

(b)

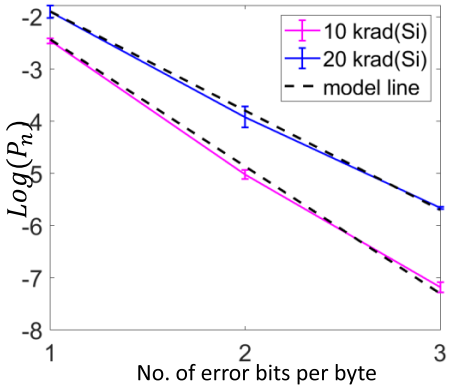

Fig. 10. (a) Illustration of failed byte location (red) on the LSB and MSB pages. Data are represented in hex format. (b) Probability of multi-bit error in a byte from six different chips.

more than one bit in error. If B_n is denoted for the number of bytes having n error bits and B_{Total} as the total number of bytes in a memory block, the probability of having erroneous bytes with n error bits is $P_n = B_n/B_{\text{Total}}$. Fig. 10(b) shows the measured probability P_n from six different chips as a function of n. We find that the data in Fig. 10(b) obeys the following relationship: $P_n = P_1^n$ as the slope of each line is very close in value to P_1. This implies that the location of bit errors in a byte are independent and uncorrelated, that is, one memory cell being in error does not force neighboring cells into error.

IV. Conclusion

In conclusion, we find that the MSB pages have a higher FBC compared to the corresponding LSB pages for a given TID irradiation. The FBC ratio between the MSB and LSB pages varies from 1 to 2 depending on the vertical layer number. We also find a significant correlation between the LSB and MSB page FBC which implies that if an LSB page is erroneous, the corresponding MSB page will also be erroneous. The fail locations on the LSB/MSB pages are not correlated. In other words, the failures do not occur at the same byte position of the LSB/MSB page. In addition, we show that there is no clustering of error bits for ionizing radiation.

The above findings help in designing more intelligent and robust memory controllers for use in high radiation environments. For example, the controller can selectively populate more important data into the LSB pages and relatively less important data into the MSB pages. Additionally, the controller can allocate more parity bits and deploy stronger ECC for MSB pages, especially the lower layers of 3-D NAND as they are more susceptible to errors.

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