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Total-Ionizing-Dose Effects on Long-term Data Retention Characteristics of Commercial 3-D NAND Memories

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***Abstract*—This article evaluates the data retention characteristics of irradiated multi-level cell (MLC) 3-D NAND flash memories. We irradiate the memory chips by a Co-60 gamma-ray source for up to 50 krad(Si) and then write a random data pattern on the irradiated chip to find its retention characteristics. The experimental results show that the data retention property of the irradiated chips is significantly degraded compared to the un-irradiated ones. We evaluate two independent strategies to improve the data retention characteristics of the irradiated chips. The first method involves high-temperature annealing of the irradiated chip while the second method suggests pre-programming the memory modules before deploying them in radiation-prone environments.**

***Index Terms*—3-D NAND flash, ionizing radiation, memory reliability, multi-level cell (MLC), total-ionizing-dose.**

I. Introduction

Continual advances in the three-dimensional (3-D) NAND technology resulted in several generations of 3-D flash memory chips featuring an ever-increasing number of layers, from early 32-layer designs to contemporary 128-layer ones [1]. These advances will enable several data-intensive applications in the future electronic systems designed for nuclear, space, and other extreme environments. However, NAND flash memory technology has several reliability concerns in the ionizing radiation environment. Since ionizing radiation introduces trap states in the oxide layers of Metal-Oxide-Semiconductor (MOS) structures, data written on an irradiated chip may be lost at a faster rate compared to an un-irradiated chip. Thus, it is important to evaluate the data retention characteristics of the irradiated chip depending on the total-ionizing-dose (TID) absorbed by it. Even though several studies were made on the TID-induced immediate data corruption issues in 3-D NAND [1]–[5], no published work is available in the literature on the data retention characteristics of the 3-D NAND chips that had been irradiated with ionizing radiation.

Oldham et al. [6], [7] evaluated the data retention characteristics of irradiated commercial off-the-shelf (COTS) two-dimensional (2-D) NAND chips. Their study confirmed a significant degradation of the data retention characteristics of the irradiated chips compared to the un-irradiated ones due to TID. Similarly, studies in the published literature [8]–[11] revealed that 2-D NAND flash memories subjected to TID can experience higher retention failure due to oxide defects. In addition, several authors [8], [12], [13] reported that data retention of floating gate flash memories degrades significantly after heavy-ion irradiation due to the charge leakage path formed in the oxide [14]–[16]. However, all the previous reports on retention characteristics of the irradiated chip were made on 2-D NAND flash technology, which reached the fundamental scaling limits around 2015. In response, the flash memory industry has transitioned to 3-D NAND flash memory technology. Unfortunately, no studies are available in the literature on the data retention characteristics of the 3-D NAND memories that had been irradiated with ionizing radiation.

In this paper, we evaluate the data retention characteristics of irradiated (TID = 50 krad(Si)) 3-D NAND memory chip with multi-level-cell (MLC) configuration. Based on the measured data, we discuss several key mechanisms for retention loss in 3-D NAND memory. Finally, we propose and experimentally validate two mitigation techniques that will minimize retention degradation on the irradiated 3-D NAND chips.

The rest of the paper is organized as follows. Section II provides the background of NAND flash memory and the fundamental retention loss mechanisms. Experimental details including a description of the samples, gamma-ray irradiation, the experimental setup, and the experimental procedure are discussed in Section III. The experimental evaluation results are given in Section IV. Section V concludes the article.

II. Background

A. Fundamentals of NAND Flash Memory

The schematic of the 3-D flash memory array is shown in Fig. 1(a). The green layers are the word lines (WL) of the memory array. The blue bottom layer is the Si substrate, and the red lines at the top are the bit lines. The purple pillars are the poly-silicon channel. Fig. 1(b) demonstrates the circuit diagram of a NAND flash memory block. Each flash memory chip

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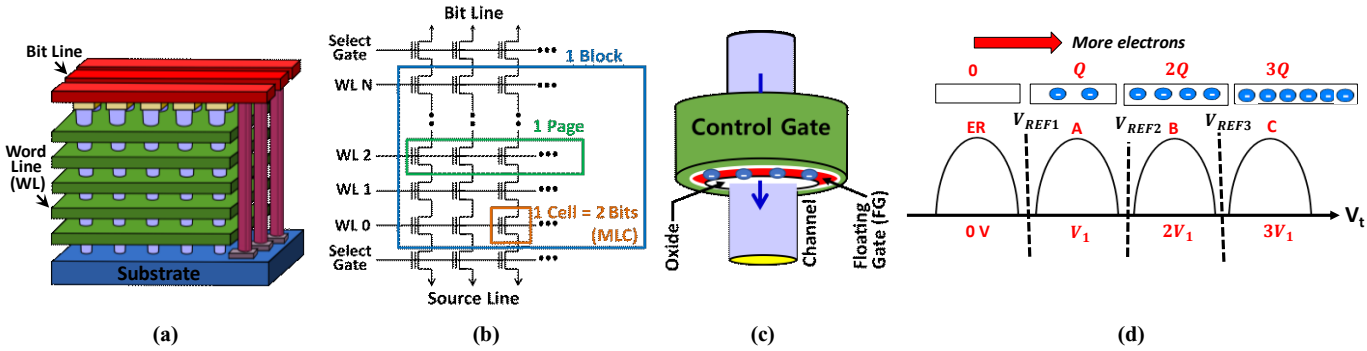

Fig. 1. (a) Schematic of a 3-D NAND flash memory array. (b) Circuit diagram of a NAND flash memory block. (c) Schematic of a 3-D floating gate NAND flash memory cell. (d) Threshold voltage distribution of multi-level cell (MLC) NAND flash memory.

contains thousands of flash blocks while each flash block consists of a certain number of flash pages. Each flash page contains multiple flash cells. The device structure of a single 3-D flash memory cell is shown in Fig. 1(c). The 3-D NAND flash memory cell is essentially a floating gate metal-oxide-semiconductor field-effect transistor (MOSFET) with gate-all-around (GAA) geometry.

A flash memory cell is a charge-based analog memory. Data are stored in the form of the electronic charge in the floating gate. The program operation charges the floating gate with electrons, whereas the erase operation removes the charges from the floating gate via Fowler-Nordheim (FN) tunneling. The stored negative charge effectively increases the transistor's threshold voltage (V_t) relative to the case when there is no charge on the floating gate. Traditional flash memory cells, a.k.a. SLCs or single-level cells, store one bit of information. Recent advances in controlling and sensing different levels of charge on the floating gate allow for flash memory cells that can store two bits of information (MLC – multi-level cell), three bits (TLC – triple-level cell), or even four bits (QLC – quad-level cell). Fig. 1(d) shows V_t distribution of four different memory states of MLC configuration. The read operation involves applying a read voltage (V_{REF}) on the control gate and sensing the cell V_t as shown in Fig. 1(d). The read reference voltage (V_{REF}) is set in between the programmed state distributions, so there is enough noise margin to correctly identify the cell states as shown in Fig. 1(d).

B. Retention Loss Mechanisms

A flash memory cell loses stored electrons over time. This is caused by several mechanisms depending on the location of the stored electrons, the defect density in the oxide layer, and the operating temperature. Fig 2(a) illustrates four fundamental charge loss mechanisms from a programmed memory cell using the 2-D cross-section of the cylindrical GAA memory cell. Fig. 2(b) shows the corresponding energy band diagram of the programmed cell in an unbiased condition, where we illustrate the location of stored electrons. Note that a few electrons might be trapped within the oxide layer instead of being stored on the floating gate during the program operation. Loss of electrons irrespective of the location will cause V_t-shift and corresponding data-loss. The four fundamental charge loss

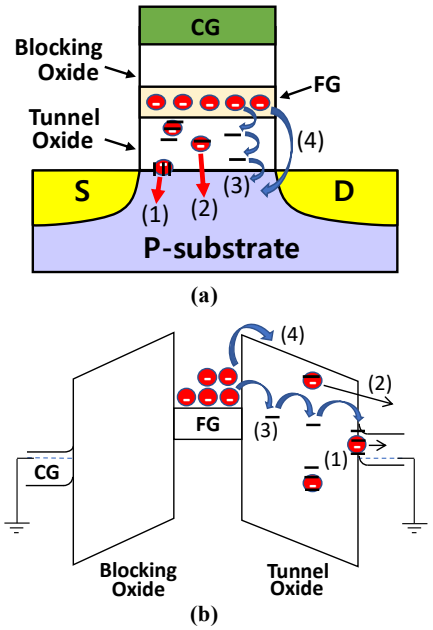

Fig. 2. (a) 2-D Cross-sectional view of the cylindrical GAA memory cell. (b) Energy band diagram of a programmed 3-D NAND flash memory cell. Four different charge loss mechanisms: (1) Interface trap recovery, (2) De-trapping, (3) Trap-assisted tunneling (TAT), and (4) Thermionic emission are explained.

mechanisms are as follows:

1) **Interface trap recovery.** This failure mechanism represents the mechanism-(1) in Fig. 2(b). Interface trap recovery occurs due to the imperfection of the oxide-silicon interface, where electrons can be trapped during the program operation [17], [18]. These trapped electrons are the quickest ones to escape out to the substrate, leading to retention errors over time.
2) **De-trapping.** The oxide layers usually have pre-existing trap states whose density increases as the memory is degraded over time. During the program operation, electrons can be captured in these trap states instead of the floating gate [17]. These electrons will spontaneously escape over time (mechanism-(2) in Fig 2(b)). As a result, the V_t value of the flash cell decreases, leading to retention errors [17], [18].

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3) **Trap-assisted tunneling (TAT).** This is the mechanism-(3) in Fig. 2(b). TAT mechanism takes place when electrons stored in the floating gate escape to the substrate through multiple trap states in the oxide layer [17], [18]. If the trap density in the oxide layer is high, electrons in the floating gate find a percolated tunneling path to the Si substrate [17]. Thus, the V_t of the flash cell decreases resulting in data retention failure [18].
4) **Thermionic emission.** This mechanism occurs when the charge stored on the floating gate leaks out to the Si substrate through thermionic emission over the floating gate-oxide barrier (mechanism-(4) in Fig 2(b)) [17]. Since the barrier height is high, the probability of charge to escape is very low and hence this mechanism contributes the least amount of charge loss at room temperature [17].

All these charge loss mechanisms will be augmented as more traps are created in the oxide layer of the flash memory cell with exposure to ionizing radiation.

III. Experimental Details

A. Description of Sample

We have utilized COTS 3-D MLC NAND flash memory chips (Part#MT29F256G08CBCBBWP-10: B). This memory chip is 32-layer first-generation 3-D NAND from Micron Technology. The device capacity is 256 GB. Each memory chip from this batch was composed of 2,192 logical flash blocks, where each block contains 1,024 logical flash pages. Each page consists of 18,592 bytes (16,384 bytes of user data with 2,208 bytes of Error Correction Code (ECC)).

B. Gamma-Ray Irradiation

To evaluate the TID effects on data retention characteristics, we exposed the flash memory chips to radiation. The irradiation experiment was performed at the Sandia National Laboratories Gamma Irradiation Facility using a Co-60 source at a dose rate of 18.6 rad(Si)/s. The memory chips received the TID up to 50 krad(Si). Gamma irradiation was performed on packaged devices with all pins grounded. The direction of gamma rays during irradiation was perpendicular to the top surface of the chip [19].

C. Experimental Setup

We have used a custom-designed hardware board as shown in Fig. 3 to interface the raw NAND flash memory chip with the computer. The board consists mainly of a TSOP socket adapter to hold NAND flash memory chip and an FT2232H mini module from Future Technology Devices International (FTDI) to interface the memory chip with a computer through Universal Serial Bus (USB) connection. This hardware setup allowed us to perform the basic memory operations such as read, program, and erase. Moreover, it allowed us to access the raw memory bits without any error correction. While the setup was used to perform basic operations, it was not exposed to gamma radiation.

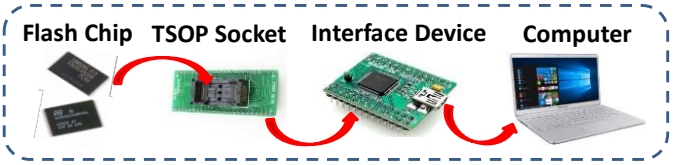

Fig. 3. Experimental setup.

D. Experimental Procedure

The experimental procedure is illustrated in Fig. 4. Data retention experiments were done on multiple identical chips that were irradiated to 50 krad(Si). Note that after 50 krad(Si) irradiation, the memory chips were fully functional. However, irradiating the chips beyond 50 krad(Si) makes the entire chip non-functional due to the failures in the peripheral circuits. Before the memory chips were exposed to radiation, all the memory blocks of the chips are kept at the factory-out erase state. Then, we exposed the chips to gamma radiation. After irradiation, we performed data retention tests. First, we freshly programmed a new set of random data on the irradiated chips and read the memory contents periodically. Then, we computed failed bit count (FBC) from the readout data. Next, we separated the irradiated chips into two groups. The chips in the first group were maintained at room temperature and their FBC was monitored. In the second group, we accelerated the retention loss by annealing the chips at a temperature of 120°C for up to 13 hours. Then, we cooled down the chips to room temperature before taking the FBC readings. To compare the retention loss, we performed the same tests on different un-irradiated chips.

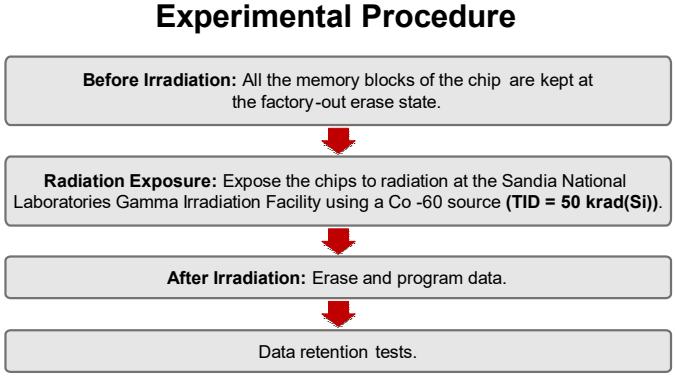

Fig. 4. Experimental procedure.

IV. Results and Discussion

We have performed the FBC analysis as a function of time to characterize retention loss of the memory chips. We read data from the chip byte by byte. Then, we compare the collected data with the original random data pattern to calculate the FBC. We compute the FBC percentage by reading 1,024 memory pages of size 16k bytes as follows:

$$FBC\ (\%) = \frac{total\ FBC}{16384 \times 8 \times 1024} \times 100\% \qquad (1)$$

In this section, we present a comparison between the FBC in the irradiated and un-irradiated chips.

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A. *Effects of TID on Data Retention Characteristics*

NAND flash memory is designed to retain data for a long duration, at least 10 years at room temperature. However, FBC in the data increases cumulatively over time due to several charge loss mechanisms as discussed in Section II B. For NAND storage, Bose-Chaudhuri-Hocquengham (BCH) code is typically used which is a class of cyclic error-correcting codes [20]–[23]. Depending on the code word length, the BCH codes can correct data with a raw bit error rate (or FBC percentage) of ~0.1% [20], [21], [23]. As long as the FBC percentage remains below a certain threshold, the ECC engine is able to correct it and recover the original data. If FBC goes beyond the ECC-threshold, data becomes uncorrectable and permanent data loss takes place. Typically, NAND manufacturers guarantee that FBC will remain below the ECC-threshold for at least 10 years at room temperature. This duration is called the room temperature data retention (RTDR) time. To evaluate RTDR time, NAND manufacturers perform an accelerated retention test by annealing the chip containing user data at a high temperature. This is called the high-temperature data retention (HTDR) test.

In this work, we have performed both RTDR and HTDR tests on irradiated and un-irradiated chips. The results are summarized in Fig 5. Fig. 5(a) compares the FBC percentage from the un-irradiated chips with the irradiated chips at room temperature. The FBC percentage (0.2×10^{-3} %) on both un-irradiated and irradiated chips were comparable when data is read out just after write operation (at 0 hr.). This similarity occurs because the NAND memory chip internally uses alternative program-verify feedback-based writing techniques that ensure similar V_t distributions, irrespective of the irradiation condition of the memory chips. However, a steep rise in the FBC percentage is observed in the irradiated chips compared to the un-irradiated chips as time progressed. For example, after 4,000 hours of room temperature wait time, FBC in the irradiated chip reached 5×10^{-3} %, whereas FBC in the un-irradiated chip was 0.5×10^{-3} %. We also observed chip-to-chip variation in the retention characteristics as depicted with green and orange colors. Such chip-to-chip variability is commonly observed in NAND flash memory technology; however, it is evident from the figure that the retention characteristics are significantly degraded on the irradiated chips.

Next, we compare the HTDR characteristics for the irradiated and un-irradiated chips in Fig. 5(b). Note that the 0-hr. FBC in both irradiated and un-irradiated chips are very similar (0.2×10^{-3} %). However, the average FBC in the irradiated chips steeply rises with time. For example, after 13 hours of bake time, FBC in the irradiated chip reached 27×10^{-3} %, whereas FBC in the un-irradiated chip was 0.7×10^{-3} %. These results confirm that the data retention characteristics are degraded on the irradiated chips. However, the FBC percentage remains significantly lower than the ECC-threshold, implying data is recoverable from the irradiated chip even after 13 hours of annealing at 120°C. The corresponding room temperature retention time can be calculated from the following acceleration factor (AF) equation [7], [24]:

$$AF = \frac{t_{R(room)}}{t_{R(bake)}} = exp\left[\left(\frac{E_a}{k_B}\right)\left(\frac{1}{T_{room}} - \frac{1}{T_{bake}}\right)\right] \qquad (2)$$

where E_a is the activation energy, k_B is the Boltzmann's constant, $t_{R(room)}$ is the retention time at room temperature (T_{room}), and $t_{R(bake)}$ is the retention time at baking temperature (T_{bake}). Note that T_{bake} is 393 K and T_{room} is 298 K. The activation energy in Eq. (2) is typically assumed to be a constant but its value varies significantly in the literature [17]. Assuming E_a = 1 eV, which is previously estimated for 3-D NAND [25], we find that 13 hours of bake time at 120°C corresponds to ~18 years at room temperature. However, it has been reported recently that the E_a value varies depending on failure mechanisms [17]. Since there are multiple failure mechanisms occurring during the HTDR experiment, we need different values of E_a at different time intervals for the accurate retention time estimation. For example, assuming E_a = 0.2 eV for interface trap recovery mechanism [17], we estimate that 13 hours of bake time at 120°C corresponds to ~4 days at room

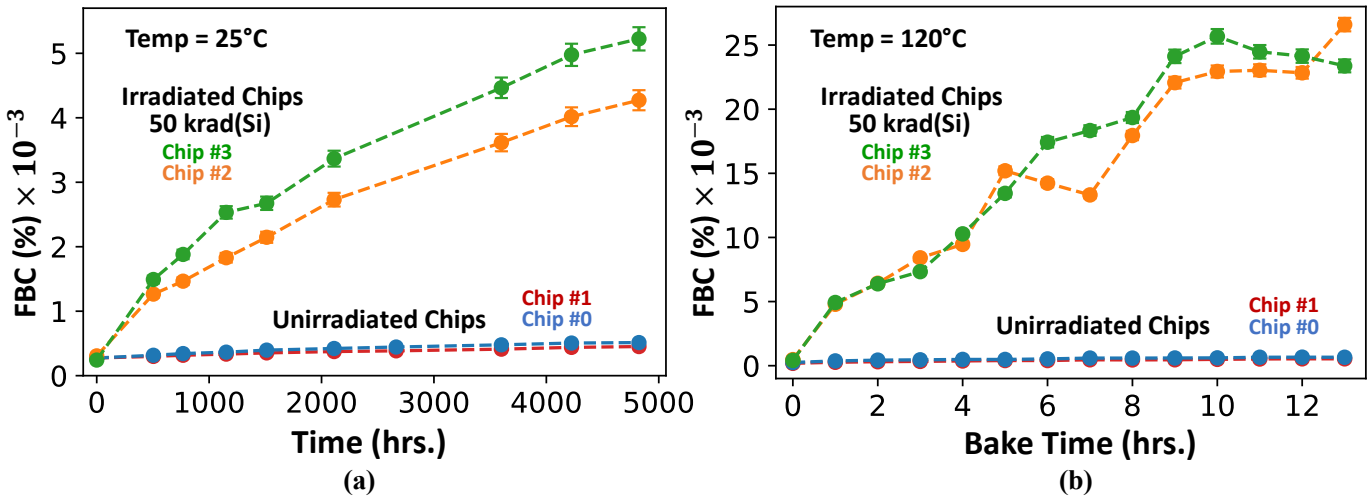

Fig. 5. Comparison of retention characteristics on the irradiated and the un-irradiated 3-D NAND flash memory chips: Plot of FBC in percentage with respect to time under (a) RTDR and (b) HTDR experiments.

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temperature. Therefore, 13 hours of annealing results may be insufficient to predict the actual FBC percentage on the irradiated chips after 10-years at room temperature. Since the goal of this paper is to highlight the general physics of irradiation effects on the retention characteristics of 3-D NAND memory, we limited our annealing time to 13-hours.

In Fig. 5(b), we observe the drop and rise in the FBC at 7 hours and 13 hours of bake time for chip #2. Note that each data point is obtained after baking the memory chip for a certain duration and then subsequent readout at room temperature. We kept a 15-minute cool-down period between the end of baking and the beginning of the readout process. If the temperature of the chip is different than room temperature during readout, such non-monotonic BER may arise. In addition to the temperature effects, there are other factors such as, read noise [26], [27] and defect annealing effects [28], which may also contribute to such a non-monotonic trend. Unfortunately, we cannot provide any conclusive evidence here due to the commercial nature of the chip.

B. *Analysis of Charge Loss Mechanisms*

We explain the retention degradation of the irradiated chips compared to the un-irradiated ones using the energy band diagrams of Fig 6. Fig. 6(a) illustrates the energy band diagram of a programmed memory cell of the un-irradiated chip with all pins grounded, where the trap density in the oxide layer is very low. Fig. 6(b) shows the corresponding energy band diagram for an irradiated memory cell with high trap density in the oxide. Note that both irradiated, as well as un-irradiated memory cells, have the same number of electrons, but their locations are very different. The same number of stored electrons will ensure similar V_t values for both the cells just after program operation. Hence, at t = 0 hr., we do not see a significant difference in the FBC from the irradiated and un-irradiated chips. However, electrons stored in the oxide layer are more vulnerable to escape compared to the ones stored in the floating gate. Hence, we observed a steep data loss for the irradiated chips in comparison to the un-irradiated ones in Fig. 5.

Since the NAND memory chip uses alternative program-verify feedback-based writing techniques, it ensures similar V_t values and correspondingly low FBC just after a program operation, irrespective of irradiation condition of the memory chips, as long as the chips are functional. However, the program operation does not control the location of stored electrons. Since TID introduces trap states in the oxide layer, a significant number of electrons will be stored in the oxide layer during a write operation on the irradiated chip. Thus, retention errors are going to be a fundamental reliability concern for irradiated memory chips.

V. Methods to Minimize Retention Degradation

In this section, we discuss two independent methods to minimize TID induced retention degradation.

A. *High-Temperature Annealing of the Irradiated Chip*

Previous studies had shown that high-temperature annealing removes TID-induced trap states in the MOS structure [29]–[31]. Here, we investigate the high-temperature annealing effects on the data retention characteristics of the irradiated memory chip. Fig. 7(a) describes the experimental steps followed to explore annealing effects. We first bake the irradiated chips for 6 hours and perform the HTDR test. The first round of the HTDR test performed on the irradiated chip is called the "before annealing" test. Since the chip is baked at an elevated temperature during the testing phase (6 hours total), annealing will take place during the first round of the retention tests. The FBC rise observed during this phase, called the "before annealing" FBC, corresponds to the red line in Fig. 7(b). After the first round of the retention tests, we freshly write data on a new set of blocks of the same chip and perform the HTDR test again for another 6 hours. The second round of the retention tests is called the "after annealing" test. The FBC obtained in this phase, called the "after annealing" FBC, corresponds to the blue line in Fig 7(b). Note that the light green line represents the FBC of the un-irradiated chip during the HTDR test.

Based on the experimental results, we observe a significant improvement in the data retention characteristics on the second round of the HTDR test indicating a significant annealing effect. We explain this observation by the annealing of defect states created by ionizing radiation. During the first round of the retention tests, we believe, the TID-induced defect density in the oxide layer gets significantly reduced. As a result, new data gets properly written on the chip after the first round of the retention tests. In other words, after the first round of the retention tests (6 hours of baking), electrons are stored mostly on the floating gate instead of the oxide layer during the write operation. As a result, we observe the improvement in FBC

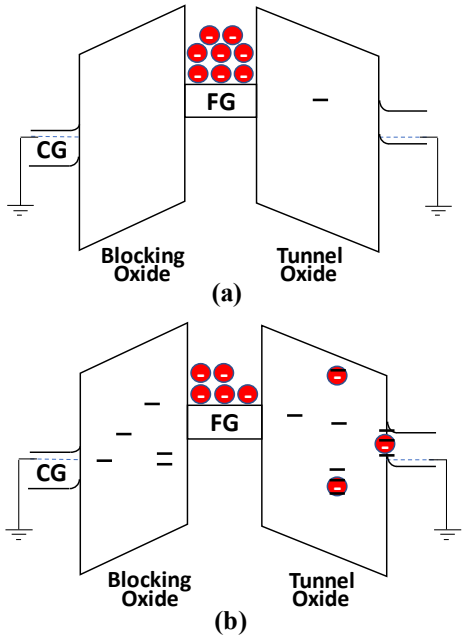

Fig. 6. Energy band diagram of a programmed memory cell with all pins grounded in the (a) un-irradiated chip and the (b) irradiated chip. Since the un-irradiated chip in fresh condition has less defect density in the oxide layer, stored electrons are mostly located on the floating gate, whereas multiple electrons are trapped in the oxide layer on the irradiated chip after program operation.

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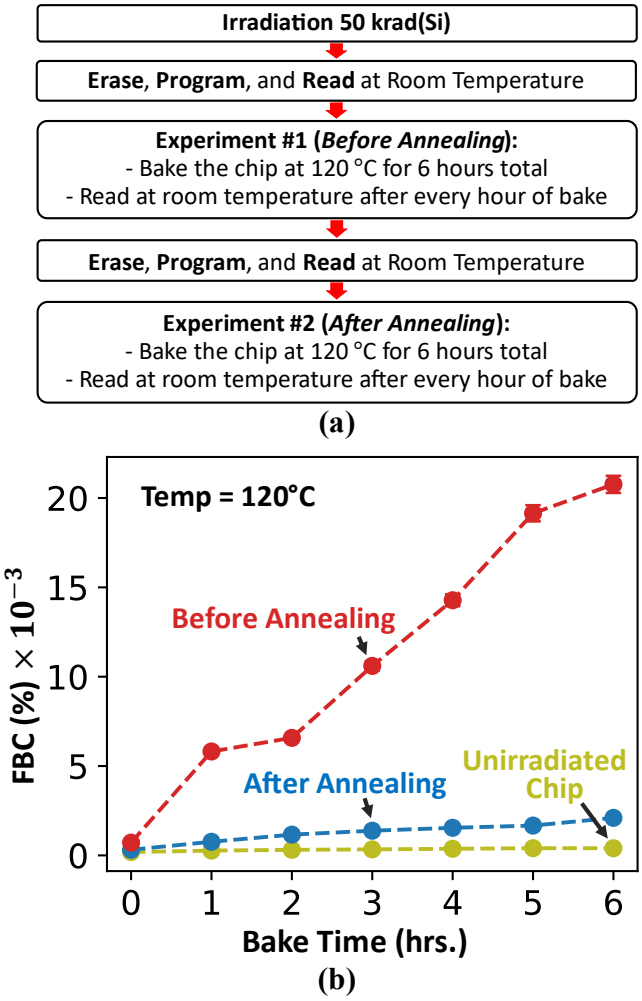

Fig. 7. (a) Block diagram showing the procedure used to evaluate the annealing effects on the irradiated 3-D NAND flash memory chip. (b) Plot of the FBC percentage during 120°C HTDR experiment with respect to bake time indicating a significant data retention improvement resulting from the annealing effects.

during the second high-temperature bake experiment or "after annealing". Thus, we can conclude that high temperature baking of the irradiated chip can improve data retention characteristics of 3-D NAND flash memory by reducing the TID-induced trap states.

B. Preconditioning Memory Modules to a Program State

In this section, we propose a technique to minimize retention degradation by pre-conditioning of the memory chip to a program state instead of leaving them in the factory-out erase state. Our hypothesis is based on experimental observation shown in Fig. 8, where we compare the data retention characteristics of the factory-out erase memory blocks versus blocks that were in the programmed state during irradiation. Note that we freshly write a new set of data on both these types of blocks after irradiation and then perform the RTDR test to collect the FBC. Fig. 8 shows that the factory-out erased blocks lose data at a faster rate compared to the blocks that were in the programmed state during irradiation.

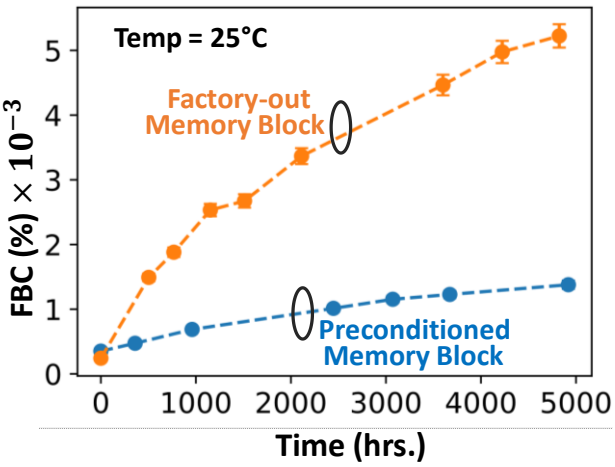

Fig. 8. Data retention comparison between memory blocks that were in the erased (or factory-out) and the programmed (or preconditioned) condition during irradiation.

We explain this result using the energy band diagram in Fig. 9(a) and (b), which correspond to a programmed memory cell and an erase memory cell, respectively. Note that there is an important distinction in terms of radiation-induced defect location for these two cells. In the programmed cell, the holes generated by the ionization in the oxide layer move toward the floating gate, creating more traps near the floating gate. However, the direction of hole movement is opposite in the case of the erased cells. This increases the probability of trap creation at the oxide-channel (Si) interface. Since trap states along the oxide-channel interface are more detrimental for the retention loss, we expect more degradation of the erase-state memory cells compared to the programmed cells on the irradiated chip.

VI. Conclusion

In conclusion, we performed RTDR and HTDR experiments to investigate the effects of TID on long-term data retention characteristics of 3-D NAND flash memory. Based on our TID irradiation up to 50 krad(Si) experiment, the key findings are as follows:

- We find that there is a significant degradation of data retention characteristics of irradiated 3-D NAND chips compared to un-irradiated chips. However, the FBC percentage remains below the standard ECC-threshold. Hence, data is recoverable on the irradiated chip after 4,000 hours of room-temperature retention time as well as 13-hours of high temperature (120°C) bake time.
- We performed high-temperature annealing experiments on the irradiated chip, which shows significant improvement of data retention characteristics. High-temperature annealing of the irradiated chip removes TID-induced defects leading to improvement in data retention characteristics.

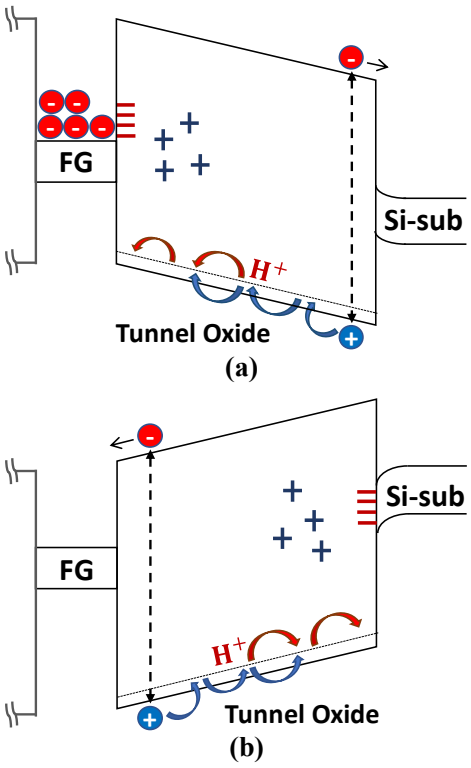

Fig. 9. Energy band diagram of the (a) programmed memory cell and the (b) erased memory cell with all pins grounded during irradiation. Radiation induced defect locations in the oxide layer are quite different based on memory state during irradiation.

- We find that the retention characteristics are more degraded on the memory blocks that were in an erased state during irradiation compared to the programmed blocks in the same chip. Therefore, we propose preconditioning the memory modules to the programmed state before deploying them in radiation-prone environments.

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