Low-Ripple High-Voltage DC Generation Using a Serially Segmented Multiphase Voltage Multiplier

Sanghyeon Park
Dept. Electrical Engineering
Stanford University
Stanford, CA, USA
spark15@stanford.edu

Juan Rivas-Davila
Dept. Electrical Engineering
Stanford University
Stanford, CA, USA
jmrivas@stanford.edu

***Abstract*—This paper presents a voltage multiplier topology that is suitable for a low-ripple high-voltage dc generation. The topology has a number of voltage multipliers connected in series and driven at different phases. Compared to a single-phase multiplier, an n-phase voltage multiplier has an output ripple that is smaller by n times. Since the ripple frequency is simultaneously increased by n times, a simple RC lowpass filter further reduces the ripple amplitude by n times, resulting in ripple reduction of n^2 times. We demonstrate the ripple reduction of the proposed topology using a 6 V-to-800 V power supply with a 16-stage four-phase bipolar voltage multiplier. The output ripple frequency is eight times the converter's switching frequency and the ripple amplitude is significantly smaller than the conventional single-phase voltage multiplier.**

I. Introduction

Low-ripple high-voltage dc is essential for many scientific instruments including X-ray generators [1], particle accelerators [2], image intensifiers [3], mass spectrometers, photomultipliers [4], and many more. It is often difficult to suppress the output noise of a power supply to a sufficient level when the voltage is in the range of kilovolts and higher. This paper proposes a voltage multiplier topology that provides a low-ripple high-voltage dc with a smaller output filter.

Arguably the most popular method of high-voltage dc generation is using a step-up transformer followed by a rectifier. The possible choice for the rectifier includes, among many others, a half-bridge rectifier [5], a full-bridge rectifier [6], or one of the various types of diode-capacitor voltage multipliers such as a voltage doubler [7], a Cockcroft-Walton multiplier [8], or a Dickson multiplier [9]. Since the transformer usually provides galvanic isolation between windings, an input-parallel output-series structure has been used for an even higher voltage gain [7], [10].

When it comes to generating an output voltage with a small ripple, multiphase interleaving can be a solution. Interleaving multiple converters is hardly a new idea, having been explored numerously in the low-voltage realm for buck, boost, SEPIC, and other common types of power converters. Even for high voltage generation, many publications discuss the idea of connecting rectifiers in parallel and driving them with multiphase ac input [7], [11], [12]. (The circuit in [11] reappears later in [13].)

This material is based upon work supported by the National Science Foundation under Grant No. 1808489.

Unfortunately, previous works on multiphase rectifiers [7], [11]–[13] only propose structures that have duplicated voltage multipliers connected in parallel. The downside of the approach is that the component count and the converter size increase with the number of driving phases. This is especially true for the majority of previously mentioned applications that demand low-ripple dc. Those applications need a high voltage for biasing purposes rather than power delivery and hence they draw little to no power from the converter output. In that case, the converter size is heavily influenced by the component count and the complexity.

We propose a voltage multiplier that operates in a multiphase interleaved way without any additional diodes or capacitors. We divide the multiplier into many small segments and drive each segment at a different phase via a transformer. The output voltage ripple becomes lower in amplitude and higher in frequency, leading to significant reduction in the filter size for a given ripple specification.

The proposed topology has been investigated previously by [14] and [15]. However, the discussion in [14] is limited to a two-phase bipolar multiplier. [15] expands the discussion to a multiplier with an arbitrary number of phases, but it does not examine how one can take advantage of the increased ripple frequency for a smaller output filter. The present study provides a more complete understanding of the benefits of a multiphase voltage multiplier.

The paper proceeds as follows. Section II describes the operating principle of the proposed circuit along with its advantages and disadvantages compared to the conventional voltage multiplier. Section III shows experimental results that verify the analysis. Section IV concludes the paper.

II. Multiphase Multiplier

A. Conventional Topology and Its Limitations

Fig. 1 illustrates a typical low-ripple high-voltage dc generator circuit and its operation. The circuit consists of the input ac source and a step-up transformer (bottom left of Fig. 1a), a voltage multiplier (middle), an RC low-pass filter (right), and the load. The voltage source at the bottom left corner provides an ac voltage v_{in} which is amplified to v_a by the transformer.

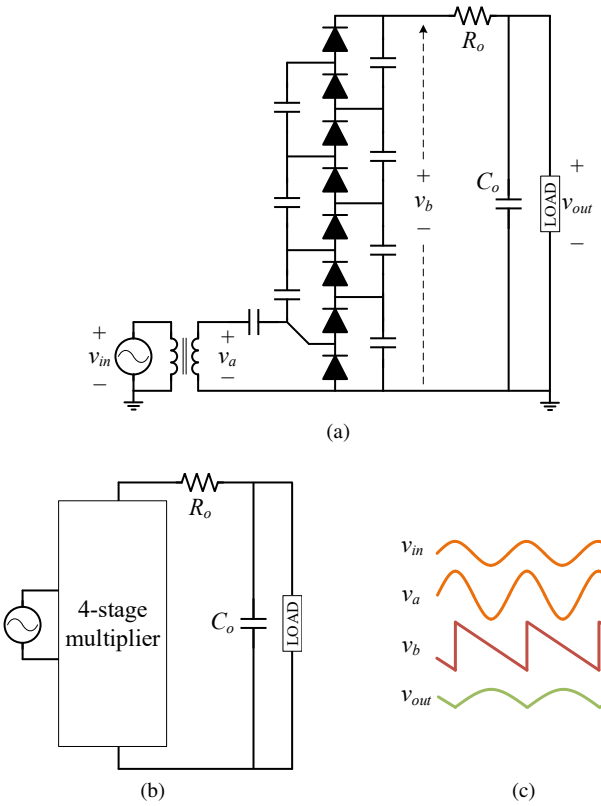


Fig. 1. A typical low-ripple high-voltage dc generator circuit. (a) Schematic. (b) Equivalent block diagram. (c) Illustrative voltage waveforms.

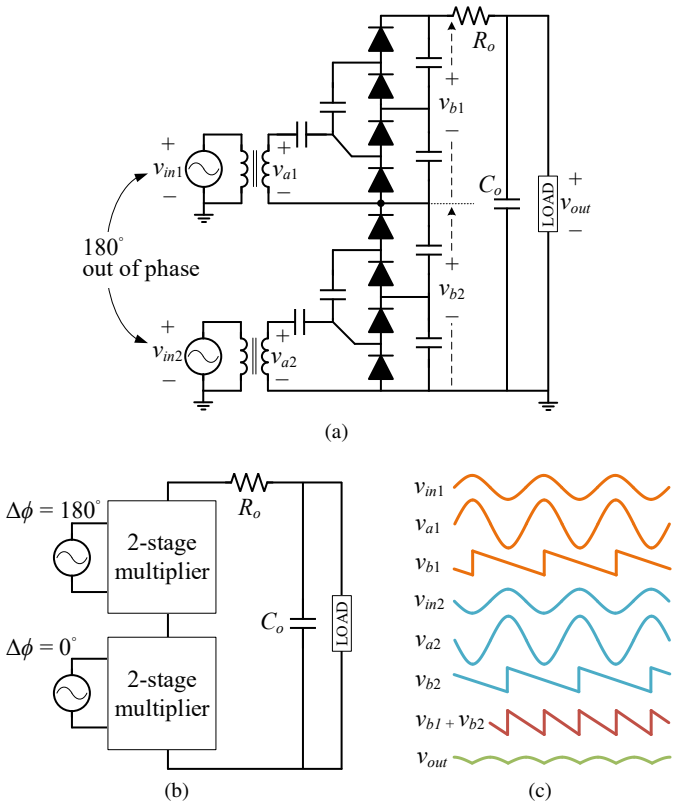


Fig. 2. Proposed serially segmented multiphase voltage multiplier. (a) Schematic. (b) Equivalent block diagram. (c) Illustrative voltage waveforms.

The four-stage multiplier, consisting of eight diodes and eight capacitors, generates a dc voltage v_b that is equal to about four times the peak-to-peak amplitude of the ac voltage v_a. (To see why the output voltage is not exactly four times the input, refer to [16]–[20].)

The RC filter consisting of R_o and C_o in Fig. 1a smooths out the ripple of the multiplier output v_b and provides a low-ripple output voltage v_{out} to the load. It is popular to use an RC filter for high-voltage dc, as can be seen from numerous designs in [4] and academic papers, e.g., [21]. When the filter's cut-off frequency f_c is lower than the multiplier's switching frequency f_{sw}, the amplitude of the output ripple is reduced by roughly (f_{sw}/f_c) times.

When the application demands a lower ripple at the output voltage of the power supply, one may consider increasing the switching frequency f_{sw} or decreasing the cut-off frequency f_c. However, both approaches have their own drawbacks.

Increasing f_{sw} may not be feasible when the transformer has a limited bandwidth. Such is the case in many off-the-shelf ferrite-core transformers or piezoelectric transformers. Not only that, diodes in the voltage multiplier often have a long reverse-recovery time, which limits the switching frequency to a few megahertz or below. This issue is more pronounced in the kilovolts-level regime where Schottky diodes are virtually non-existent.

Decreasing f_c may also prove infeasible. It is often difficult to find off-the-shelf capacitors that are rated more than a few kilovolts; usually they are available only via made-to-order production. Moreover, the capacitor volume easily becomes too large as the output voltage gets higher. This is due to an upper limit on the energy density of any capacitor dielectric material. Because the energy stored in a capacitor is proportional to the voltage squared, the capacitor volume is also proportional to the square of the output level of the high-voltage power supply.

B. Proposed Topology

Fig. 2 shows the schematic of the proposed topology (Fig. 2a), its equivalent block diagram (Fig. 2b), and voltage waveforms (Fig. 2c). The voltage multiplier is segmented into two parts and each segment is driven by an inverter and an isolation transformer. Input voltages v_{in1} and v_{in2} are 180° out of phase, hence ripples at the output of each segment v_{b1} and v_{b2} are also 180° out of phase. The multiplier output $(v_{b1} + v_{b2})$ has the same dc level as v_b in Fig. 1, but with half the peak-to-peak ripple and twice the ripple frequency of v_b in Fig. 1. Due to the attenuation by the RC filter, the final ripple amplitude at v_{out} is only a quarter of that in the conventional circuit of Fig. 1.

The transformation from Fig. 1b to Fig. 2b can be generalized to the case of an arbitrary mn-stage multiplier, where m and n are integers. Fig. 3 shows such a case, where Fig. 3a is the conventional single-phase structure and Fig. 3b is the proposed multiphase structure. The circuit is divided into n

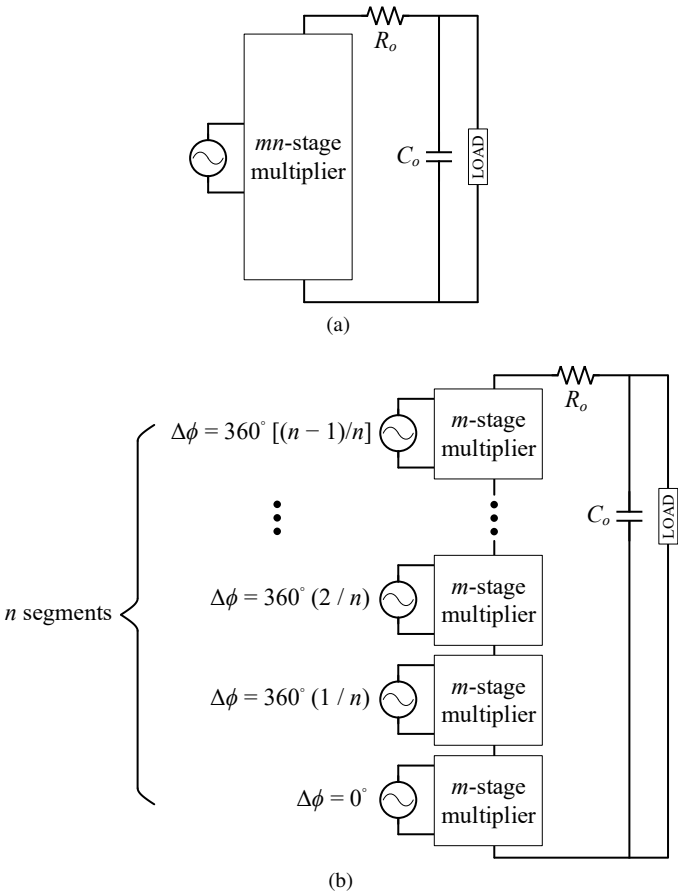


Fig. 3. Transformation of an arbitrary mn-stage multiplier from single phase to multiphase, where m and n are integers. (a) Conventional single-phase structure. (b) Proposed multiphase structure.

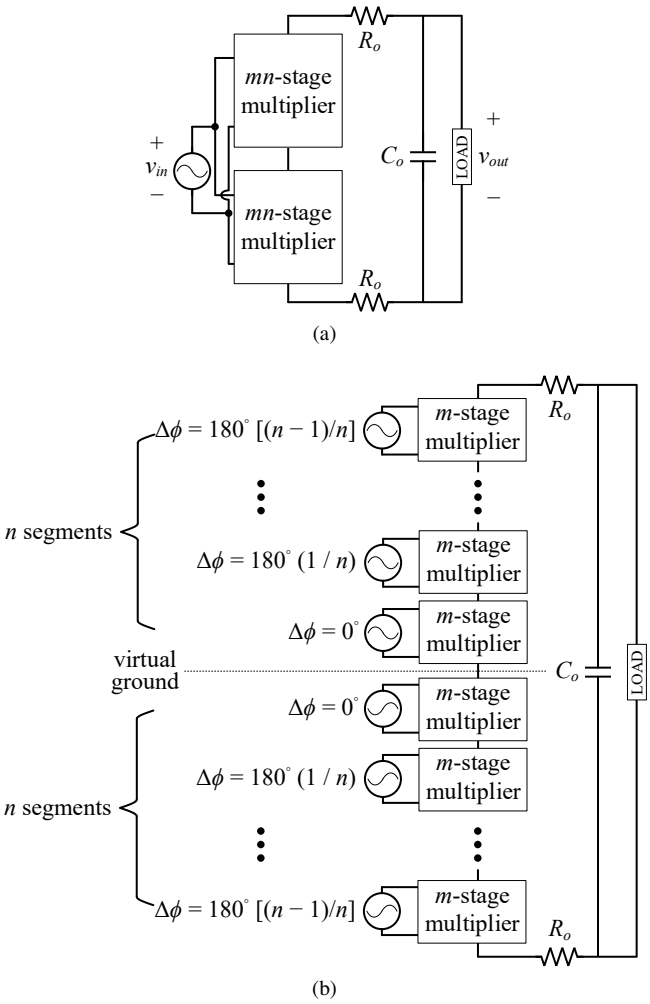


Fig. 4. Bipolar voltage multiplier that produces both a positive and negative output. (a) Conventional single-phase multiplier. (b) Multiphase multiplier.

segments of m-stage multipliers and those segments are driven by ac voltage sources of n evenly staggered phases.

The result is that, without an output filter, the output voltage of Fig. 3b has a ripple that is n times smaller in amplitude and n times higher in frequency compared to Fig. 3a. With an RC filter, the ripple is attenuated by another n times, resulting in an n^2 times smaller ripple amplitude compared to a single-phase multiplier. As long as the filter cut-off frequency is below the converter switching frequency, the capacitor volume can be reduced by a factor of n^2 for a given ripple specification. If allowed, a multi-stage RC filter with the attenuation ratio higher than 20 dB per decade can be used for an even greater benefit.

On the downside, the proposed n-phase topology demands that n transformers be installed instead of a single transformer. Moreover, those transformers should withstand a dc voltage stress comparable to the converter output voltage. Let us assume that the transformer size is mostly determined by the insulation, and that the volume of insulation material is proportional to the voltage it needs to withstand. Then the total volume occupied by transformers is proportional to the number of phases n.

The increased transformer volume may negate the benefit of a smaller filter capacitor. Therefore, the proposed approach should be used when the benefits outweigh the costs. For instance, an input-parallel output-series converter with air-core high-voltage transformers [9], [10], [22] is where the proposed technique naturally fits the circuit topology.

C. Bipolar Multiplier Variant

Fig. 4 illustrates how the proposed approach can be applied to a bipolar voltage multiplier. A bipolar voltage multiplier produces both a positive and negative output. The symmetric configuration doubles the level of the output voltage v_{out}.

Interestingly, in some sense, the conventional bipolar multiplier of Fig. 4a is already a two-phase structure to begin with. The top half of Fig. 4a has its output capacitor replenished at the positive peak of the input voltage, while the bottom half does the same at the negative peak of the input voltage v_{in}. The fact that the top half and the bottom half operate 180° out of phase means that the output ripple frequency is twice the switching frequency even without serial segmentation and multiphase operation.

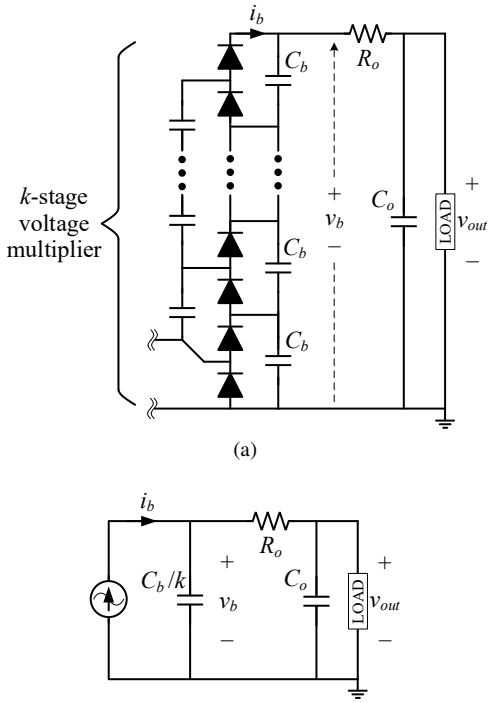


Fig. 5. Circuit model for the RC output filter design. (a) Schematic of the power supply. (b) Equivalent circuit model.

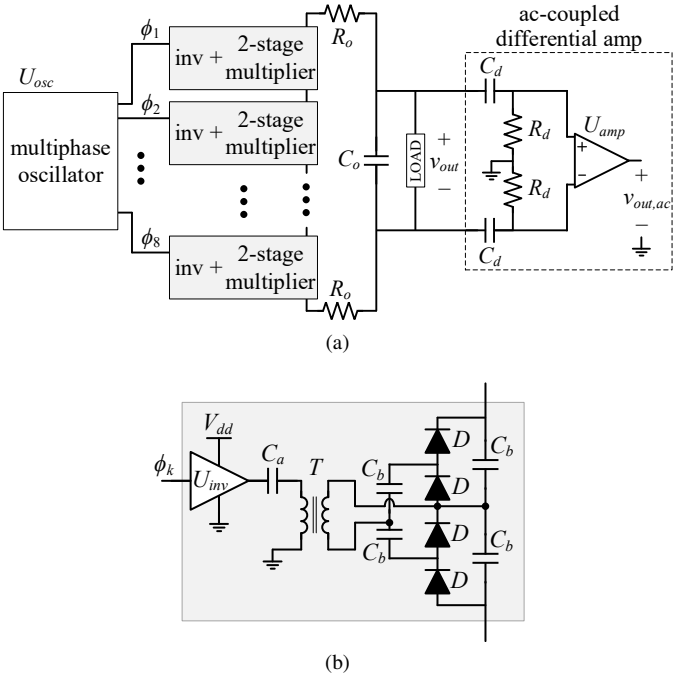


Fig. 6. Diagram for the implemented 16-stage four-phase bipolar voltage multiplier. (a) Overall structure. (b) Detailed structure of the 'inverter + 2-stage multiplier' block in Fig. 6a.

Fig. 4b shows the circuit diagram of a bipolar multiphase voltage multiplier. Top- and bottom-half parts are evenly divided into n segments and they are driven by ac voltage sources at staggered phases. The output ripple frequency becomes $2n$ times the converter switching frequency and its amplitude becomes $1/(2n)$ times that of the single-ended case. Phases of the voltage sources are set in a symmetrical manner with respect to the virtual ground in the middle. This symmetry minimizes the output noise from the common-mode effect and capacitive feedthrough of isolation transformers.

D. Output Filter Design

When designing the RC output filter, it is important to model the voltage multiplier as a pulsed current source with an output capacitor. Fig. 5 describes the circuit model. The rational for such model is that the current from the diode chain is always very spiky, i.e., the time frame of those current pulses is much shorter than any voltage or current changes in the rest of the circuit.

The transfer function of the filter is v_{out}/i_b rather than v_{out}/v_b. Therefore, one should take into account the capacitance C_b/k which is equivalent to serially connected coupling capacitors. For proper ripple attenuation, not only the cut-off frequency of R_o and C_o but also that of R_o and C_b/k should be sufficiently below the ripple frequency.

III. Experimental Results

A. Test Setup

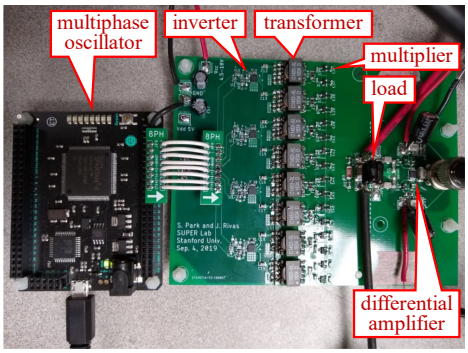
Fig. 6 describes the circuit we implemented. The purpose of this circuit is to verify that the output ripple decreases with the number of phases n when there is no RC filter, and with n^2 when there is one.

TABLE I
Parameters and part numbers for Fig. 6.

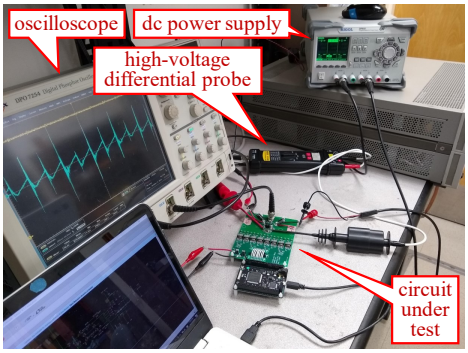
Item	Description
U_{osc}	Mojo v3 FPGA dev. board (Spartan-6 LX9)
$\phi_{1,\ldots,8}$	square wave, 260 kHz; see Fig. 8 for phases.
U_{inv}	UCC27524DSDR, Texas Instruments
C_a	0.047 µF, C0G
T	C1453-AL, Coilcraft
C_b	10 nF C0G
D	BAS31, ON Semiconductor
R_o	0 for section III-B, 1.13 kΩ for section III-C
C_o	0 for section III-B, 1 nF C0G for section III-C
load	1 MΩ resistor
C_d	22 nF C0G
R_d	931 kΩ
U_{amp}	AD8130, Analog Devices

A multiphase oscillator U_{osc}, implemented with an FPGA, provides input stimuli $\phi_1, \ldots, \phi_8$ at 260.42 kHz to eight inverters. Each of those inverters drives a two-stage voltage multiplier via a transformer. All multipliers are connected in series, forming a 16-stage bipolar voltage multiplier. The multiplier output is either directly connected to the load (section III-B) or is followed by an RC low-pass filter (section III-C).

In order to accurately measure the ripple voltage across the load, we add an RC high-pass filter and a differential-

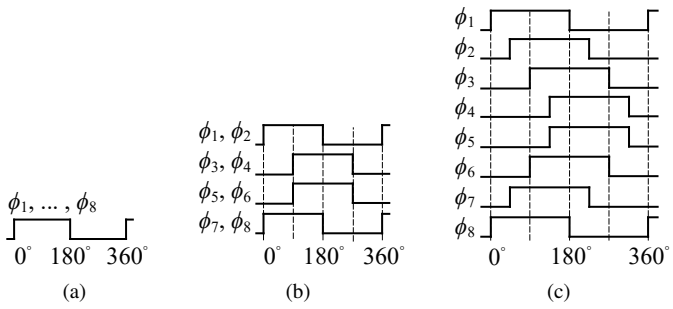


(a)



(b)

Fig. 7. Experimental setup. (a) Implemented high-voltage power supply and auxiliary circuits. (b) Equipment layout.



(a) (b) (c)

Fig. 8. Stimulus patterns from the oscillator U_{osc}. The frequency of each signal is 260 kHz. (a) Single-phase mode. (b) Two-phase mode. (c) Four-phase mode.

to-single-ended amplifier U_{amp}. We use a high-voltage differential probe to measure v_{out} and a direct connection via a coaxial cable to measure $v_{out,ac}$. Table I lists parameters and part numbers for Fig. 6. The implemented circuit and the equipment layout are shown in Fig. 7.

The stimulus pattern from the oscillator U_{osc} is changed between single-phase, two-phase, and four-phase modes as described in Fig. 8. Those stimuli follow the phase relations described in Fig. 4b for n of one, two, and four. Following two sections show the data obtained for those three input patterns.

B. Test Results Without a Filter

In this section, we measure the output voltage ripple while changing the number of phases from one to two, and then four as illustrated in Fig. 8. Throughout the experiment, we maintain the average output voltage at 800 V by adjusting the inverter's supply voltage V_{dd}. The necessary value of V_{dd} ranges from 6.3 V to 6.7 V.

Fig. 9 shows measured waveforms of the output v_{out} and its ripple $v_{out,ac}$. The peak-to-peak amplitude of the sawtooth waveforms matches the analysis in [18]–[20]. As expected, ripple frequencies at one-, two-, and four-phase modes are twice, four times, and eight times the switching frequency of the converter. Meanwhile, the peak-to-peak amplitude of the triangular ripple is halved every time the number of phase doubles. This result corroborates the analysis in section II. Note that high-frequency "spikes" in ripple waveforms are associated with diode turn-on and -off transitions, and can be attenuated with ferrite beads if necessary.

C. Test Results With an RC Filter

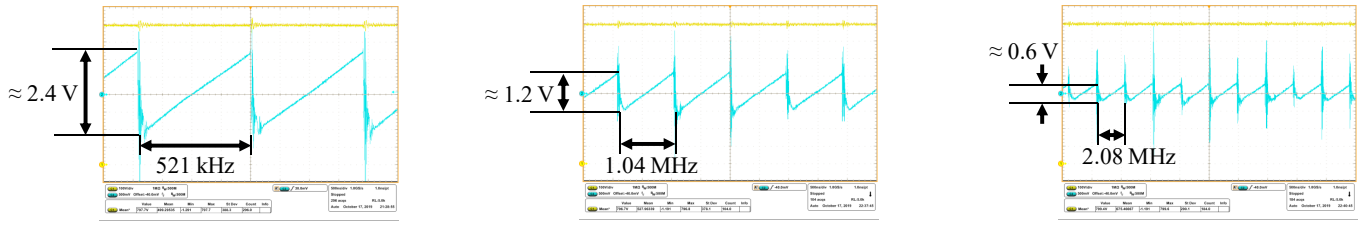
We repeat the measurements with an RC filter added at the output. The cut-off frequency of the filter is 70 kHz which is sufficiently lower than the converter switching frequency. Fig. 10 shows measured waveforms of v_{out} and $v_{out,ac}$. The ripple amplitude excluding high-frequency noises becomes roughly 16 times smaller as the number of phases changes from one to four.

In order to accurately quantify the reduction of the ripple, we perform Fourier analysis with the resolution bandwidth of 7.2 kHz on three ripple waveforms. The frequency spectra are shown in Fig. 11. Besides the 260 kHz peak at the converter switching frequency, the most prominent peaks are at 521 kHz for the one-phase mode, 1.04 MHz for the two-phase mode, and 2.08 MHz for the four-phase mode. Those peaks decrease in magnitude by a factor of 12 dB (equal to 4 times), indicative of the n^2 times ripple reduction as described in section II. As a side note, the spiky noise in ripple waveforms of Fig. 10 appear as a frequency component at around 100 MHz (not shown in Fig. 11).

IV. Conclusion

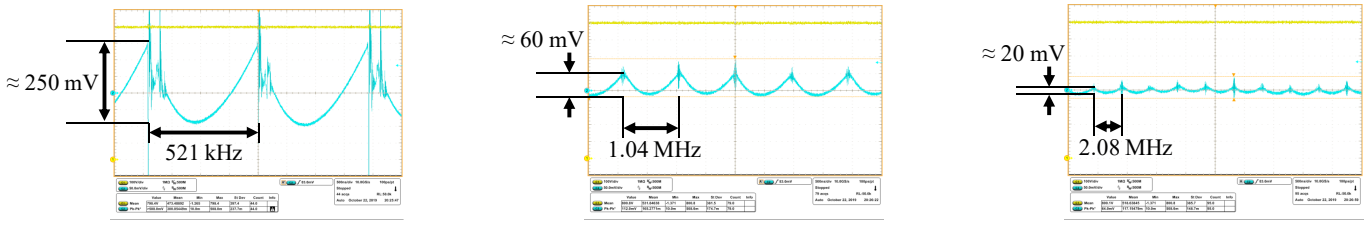
This paper presented a voltage multiplier that is serially segmented and driven in a multiphase mode. By staggering the phase of input signals that drive voltage multiplier segments, the ripple in the output voltage is reduced and consequently the necessary output filter size is also reduced. The ripple reduction is proportional to the number of phases when there is no output filter, and to the number of phases squared when there is a first-order RC filter. Higher-order filters can be used for an even greater benefit. Those advantages are gained at the expense of increased number of isolation transformers and inverters, so one should weight the pros and cons before adopting the proposed topology.

The ripple reduction was demonstrated by an experiment with a 16-stage bipolar voltage multiplier divided into 8 segments and driven in a single-phase, two-phase, and four-phase modes. When the number of phase was increased from 1 to 4, the amplitude of the output voltage ripple was decreased



(a) (b) (c)

Fig. 9. Measured waveforms of the output voltage v_{out} (yellow curve, 100 V/div) and its ripple $v_{out,ac}$ (blue curve, 500 mV/div) *without* an RC filter. The horizontal scale is 500 ns/div. (a) Single-phase mode. (b) Two-phase mode. (c) Four-phase mode.



(a) (b) (c)

Fig. 10. Measured waveforms of the output voltage v_{out} (yellow curve, 100 V/div) and its ripple $v_{out,ac}$ (blue curve, 50 mV/div) *with* an RC filter (cut-off frequency at 70 kHz). The horizontal scale is 500 ns/div. (a) Single-phase mode. (b) Two-phase mode. (c) Four-phase mode.

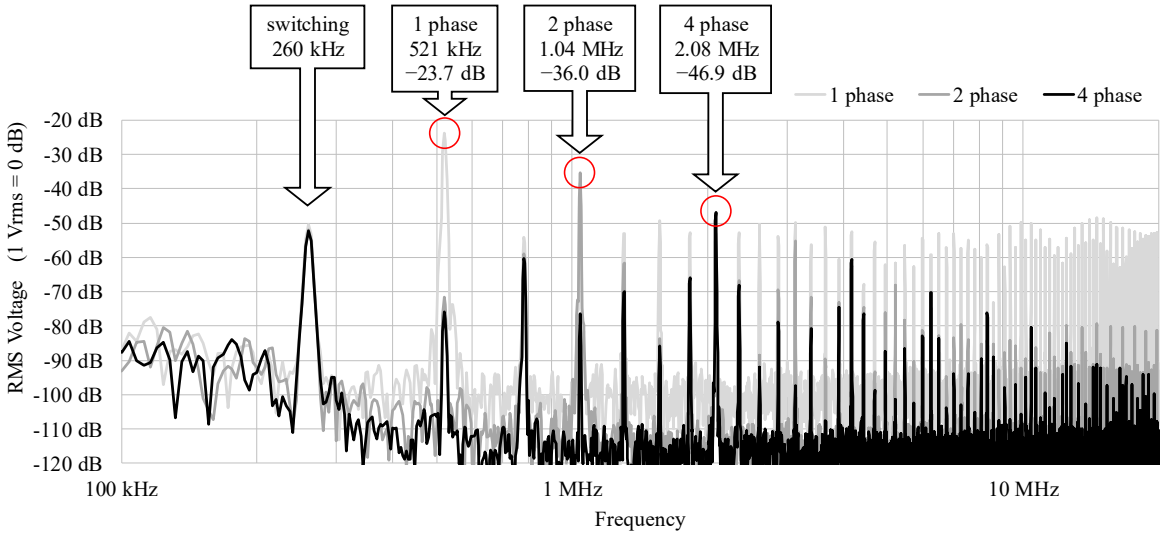


Fig. 11. Frequency spectra of the output voltage ripple in one-, two-, and four-phase mode; Hanning-windowed, 10 GS/s sampling rate, and resolution bandwidth of 7.2 kHz.

by 4 times without an output filter, and 16 times with an RC low-pass filter.

References

[1] J. Beutel, H. L. Kundel, and R. L. Van Metter, *Handbook of medical imaging*. Spie Press, 2000, vol. 1.

[2] S. Humphries, *Principles of charged particle acceleration*. Courier Corporation, 2013.

[3] L. M. Biberman, *Photoelectronic imaging devices. 2. Devices and their evaluation*. Plenum Press, 1971.

[4] R. S. Bever, A. P. Ruitberg, C. W. Kellenbenz, and S. M. Irish, "High voltage power supply design guide for space," NASA Goddard Space Flight Center, Tech. Rep., 2006.

[5] Y. Du, J. Wang, G. Wang, and A. Q. Huang, "Modeling of the high-frequency rectifier with 10-kV SiC JBS diodes in high-voltage series resonant type dc–dc converters," *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 4288–4300, Aug 2014.

[6] A. Lohner, T. Meyer, and A. Nagel, "A new panel-integratable inverter concept for grid-connected photovoltaic systems," in *Proceedings of IEEE International Symposium on Industrial Electronics*, vol. 2, June 1996, pp. 827–831 vol.2.

[7] V. N. Lisin, M. V. Pavlov, J. V. Laschenov, S. I. Gusev, L. V. Kozlov, S. V. Pokrovsky, I. I. Mozhaev *et al.*, "High-voltage transformer-rectifier device," Jul. 6 1982, uS Patent 4,338,657.

[8] H. Xu, Y. He, K. L. Strobel, C. K. Gilmore, S. P. Kelley, C. C. Hennick, T. Sebastian, M. R. Woolston, D. J. Perreault, and S. R. H. Barrett, "Flight of an aeroplane with solid-state propulsion,"

Nature, vol. 563, no. 7732, pp. 532–535, 2018. [Online]. Available: https://doi.org/10.1038/s41586-018-0707-9

[9] S. Park, L. Gu, and J. Rivas-Davila, "A compact 45 V-to-54 kV modular dc-dc converter," in *2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL)*, June 2019, pp. 1–7.

[10] ——, "60 V-to-35 kV input-parallel output-series dc-dc converter using multi-level class-DE rectifiers," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2018, pp. 2235–2241.

[11] R. M. Martinelli and A. F. Ahrens, "Multiphase capacitor-diode voltage multiplier," in *1978 IEEE Power Electronics Specialists Conference*, June 1978, pp. 275–284.

[12] S. Iqbal, "A three-phase symmetrical multistage voltage multiplier," *IEEE Power Electronics Letters*, vol. 3, no. 1, pp. 30–33, March 2005.

[13] R. Gules, L. L. Pfitscher, and L. C. Franco, "An interleaved boost dc-dc converter with large conversion ratio," in *2003 IEEE International Symposium on Industrial Electronics (Cat. No.03TH8692)*, vol. 1, June 2003, pp. 411–416 vol. 1.

[14] H. Baumann, "X-ray diagnostic generator," Feb. 22 1983, uS Patent 4,375,105.

[15] A. Pokryvailo, C. Carp, and C. Scapellati, "A high-power high-voltage power supply for long-pulse applications," *IEEE Transactions on Plasma Science*, vol. 38, no. 10, pp. 2604–2610, Oct 2010.

[16] J. D. Cockcroft and E. T. Walton, "Experiments with high velocity positive ions.—(i) further developments in the method of obtaining high velocity positive ions," *Proceedings of the Royal Society of London. Series A, Containing Papers of a Mathematical and Physical Character*, vol. 136, no. 830, pp. 619–630, 1932.

[17] M. M. Weiner, "Analysis of Cockcroft-Walton voltage multipliers with an arbitrary number of stages," *Review of Scientific Instruments*, vol. 40, no. 2, pp. 330–333, 1969.

[18] J. Kuffel and P. Kuffel, *High voltage engineering fundamentals*. Elsevier, 2000.

[19] M. S. Naidu and V. Kamaraju, *High Voltage Engineering*. McGraw-Hill, 2010.

[20] S. Ray, *Introduction To High Voltage Engineering*. PHI Learning, 2013.

[21] C. Scapellati, "High voltage power supplies for analytical instrumentation," *SPECTROSCOPY-SPRINGFIELD THEN EUGENE THEN DULUTH-*, vol. 19, no. 2; SUPP, pp. 35–36, 2004.

[22] S. Mao, C. Li, T. Song, J. Popovic, and J. A. Ferreira, "High frequency high voltage generation with air-core transformer," in *2017 IEEE International Workshop On Integrated Power Packaging (IWIPP)*, April 2017.