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Tailoring the CdS/CdSe/CdTe multilayer structure for optimization of photovoltaic device performance guided by mapping spectroscopic ellipsometry



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ABSTRACT

Thin film CdTe superstrate solar cells have been fabricated by sputtering starting from CdS/CdSe front layers deposited on transparent conductor coated glass. The performance of such devices is sensitive to the fabrication details including the temperature-time profile, which leads to CdSe/CdTe interdiffusion and formation of a CdTe_{1-x}Se_x bandgap-graded absorber. Mapping spectroscopic ellipsometry (M-SE) has been applied to the CdS and CdSe thin films for process calibration, which involves determining the deposition rate in terms of effective thickness (volume/area) versus spatial position on the sample. The goal is to optimize the performance of the devices by correlating cell parameters with these two effective thicknesses. Intended variations in the thicknesses along with unintended spatial non-uniformities enable coarse and fine-scale optimization, respectively. Using these methods, the highest performance solar cells from the CdS/CdSe/CdTe structure are obtained with 13 nm CdS and 100 nm CdSe. An increase in the CdS thickness above 13 nm leads to a decrease in open-circuit voltage and fill-factor attributed to the formation of a CdSe_{1-z}S_z interdiffusion region with z approaching 0.5, where the alloy electronic properties are likely to suffer. Our results demonstrate that M-SE, exploited in conjunction with deposition non-uniformities, serve as a viable approach for process optimization of complex solar cell structures.

1. Introduction

The CdS/CdTe heterojunction interface region of the CdTe solar cell is affected by the temperature-time profile that the structure undergoes, including the CdTe deposition at an elevated temperature and the CdCl₂ post-deposition heat treatment. As a result, a CdS_{1-y}Te_y alloy region forms by tellurium (Te) diffusion into the CdS layer and a CdTe_{1-x}S_x alloy region forms on the absorber side by sulfur (S) diffusion into CdTe [1–6]. The CdS_{1-y}Te_y alloy region of reduced bandgap is found to be photo-electronically inactive due to the high concentration of defects in the starting CdS. Thus, this alloying is detrimental to the short circuit current density (J_{sc}) of the cell. The CdS layer thickness can be reduced to limit the impact of this alloying on J_{sc} , but partly at the expense of open circuit voltage (V_{oc}) and fill factor (*FF*). On the other hand, the CdTe_{1-x}S_x region on the absorber side is considered photo-electronically active and exhibits a narrower bandgap than the CdTe itself due to bowing of the bandgap [2,7–10]. No significant gains in J_{sc} via absorption in the CdTe_{1-x}S_x region have been identified, however, because of the low solubility of S in CdTe resulting from the large lattice mismatch between CdS and CdTe [7,11,12] as well as the possibility of a very thin interaction region [13].

Thin film CdSe is an alternative n-type layer that can be used in the same role as CdS [14–20]. Considering a fabrication process in which CdTe is deposited on a distinct CdSe layer, graded alloy compounds that can be described as $CdSe_{1-w}Te_w$ and $CdTe_{1-x}Se_x$ are formed by interdiffusion between the CdSe and CdTe layers under the time-temperature profiles of the process. With respect to alloying in the junction region, CdSe holds distinct advantages over CdS. First, in contrast to $CdS_{1-y}Te_y$, the CdSe_{1-w}Te_w region can be photo-electronically active under optimum conditions, leading to a significant increase in J_{sc} due to collection of short wavelength light. Second, Se has higher solubility in the CdTe layer than does S due to the smaller lattice mismatch of CdSe and CdTe

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[15–17]. Because of these effects, a CdTe_{1-x}Se_x alloy with x = 0.5 can form by interdiffusion, and this alloy has a bandgap ~ 0.1 eV lower than that of the CdTe itself [21,22]. Thus, a significantly improved long wavelength response is also possible, i.e. a shift of the external quantum efficiency (EQE) fall-off to increased wavelength, leading to increased $J_{\rm sc}$. Because an unalloyed CdSe layer is not believed to be photo-electronically active [16], interdiffusion must occur such that no residual pure CdSe (or CdSe1-wTew with low w) remains at the front of the device in order to prevent loss of EQE in the short wavelength region. Because CdSe interdiffusion with CdTe is enhanced relative to CdS, a well-defined notch-like bandgap profile can be achieved similar to that in optimized three-stage CuIn1-xGaxSe2 (CIGS) absorber fabrication [23]. In addition, because of II-VI compound compatibility, CdSe can be prepared with the same wide variety of deposition techniques as CdTe absorbers, yielding a similar range and controllability of film properties as has been reported previously for CdTe [24-29].

For CdTe solar cells incorporating CdSe in place of CdS, however, interface formation between the high resistivity transparent (HRT) layer, typically SnO₂, and the CdSe_{1-w}Te_w alloy is considered one of the challenging issues. Advances in the solar cell fabrication process for CdSe/CdTe are needed due to the observed reduction in Voc and FF compared to CdS/CdTe cells [14–16]. A number of studies indicate that inserting a CdS layer between the HRT and CdSe1-wTew layers as a thin inactive window component for the solar cell can improve V_{oc} [14,15, 30-33]. With this approach, CdSe is deposited as an intermediate layer at the CdS/CdTe heterojunction, yielding compositional and bandgap profiles again controlled by the time-temperature profiles of the process. The resulting bandgap profile of the intermixed CdS/CdSe/CdTe components of the solar cell is expected to exhibit a complicated shape ranging from as high as \sim 2.4 eV (for unalloyed CdS) at the front of the cell, dropping to a potential minimum of \sim 1.4 eV (for CdSe_{0.5}Te_{0.5}) near the diffuse junction and gradually increasing to 1.5 eV (CdTe) at the back of the device.

This investigation follows up on previous research by Razooqi et al. [34] who reported a systematic mapping spectroscopic ellipsometry (M-SE) study of CdSe/CdTe solar cell structures without the standard n-type CdS window layer. J_{sc} enhancement by CdSe was optimized by exploiting correlations between the M-SE determined CdSe effective thickness (volume/area) at a given location and the dot solar cell performance parameters at that location. Due to the non-uniformity in the as-deposited CdSe thickness over the area of the substrate, the statistics of the thickness-performance correlations could be increased, enabling a reduction in the number of depositions required for optimization. In the previous research, the optimum J_{sc} was characterized by enhancements in both the short and long wavelength regions of the EQE response, but at the expense of V_{oc} and *FF* [34].

In this new study, solar cell optimization has been expanded to include both CdS and CdSe layer thicknesses, starting from an initially deposited CdS/CdSe bilayer. Both CdS and CdSe deposition processes have been calibrated by M-SE in order to associate a given location on the TECTM15/HRT/CdS/CdSe surface with a pair of effective thicknesses for CdS and CdSe, given the two deposition times. The importance of these results derives from the ability to establish fine scale propertyperformance correlations spatially in a single deposition, relying on the thickness non-uniformity associated with the deposition systems. By performing M-SE calibrations, these spatial non-uniformities can be exploited such that device performance variations within a single deposition can be understood in terms of property variations, and correlations can be established for use in fine scale optimization. The success of this approach is illustrated here through correlations established between the M-SE results for front layer CdS and CdSe effective thicknesses at a given location and the CdTe solar cell performance at that location. Two ranges of CdS effective thickness near ~10 nm and above \sim 100 nm have been found to provide maxima in the V_{oc} \times *FF* product, both ranges with an optimum CdSe effective thickness near 100 nm. These ranges have been proposed as yielding dilute solutions of CdS in

CdSe and dilute solutions of CdSe in CdS, respectively, when the two adjoining layers interact. The overall highest efficiency as a function of CdS effective thickness is controlled by the variation in J_{sc} , which exhibits a maximum for a CdS effective thickness of 13 nm.

2. Experimental details

2.1. Solar cell fabrication

Schematic diagrams of the structure of the solar cells of this study are shown in Fig. S1 of Appendix A, Supplementary data. The CdS layers were deposited first by magnetron sputtering onto 6.5 cm \times 6.5 cm TECTM15 M substrates placed reproducibly at the center of the substrate holder. Next, the CdSe layers were deposited onto the CdS coated substrates in a separate sputtering system. For each of these CdS and CdSe thin films, all sputter deposition parameters were kept the same from run to run, as given in Table S1 of Appendix A, and only the CdS and CdSe deposition times were varied. These times were selected to obtain the desired maximum CdS and CdSe effective thicknesses at the substrate center based on M-SE calibration of the two deposition systems as described in Section 2.2. The CdTe absorber layers used in all devices were deposited by sputtering to a fixed final thickness of ~ 2 um on the TECTM15/HRT/CdS/CdSe structures. The CdCl₂ treatment and the procedures for back contact formation were described previously in Ref. [34]. The sputter deposition parameters for the three semiconductor layers of the cell structures in this study are summarized in Table S1 of Appendix A.

2.2. Solar cell property-performance correlations

Before the deposition of the solar cells as described in Section 2.1, M-SE was performed on CdS and CdSe thin films on soda-lime glass and TECTM15 M substrates, respectively, for location-dependent effective thickness calibrations [34–37]. M-SE measurements were performed using a rotating-compensator multichannel instrument (AccuMap-SE, J. A. Woollam Co., Inc). A total of 81 locations were measured, corresponding to the locations of the subsequently fabricated dot solar cell devices.

Analysis of these data yields maps in the structural and optical property parameters over the \sim 6.5 cm \times 6.5 cm area of each calibration sample. The effective thickness maps are calculated from the structural parameters using material volume fractions determined from the Bruggeman effective medium approximation [38]. Each such volume fraction is multiplied by the thickness of the corresponding layer, and the products are summed for all layers that include the material (CdS or CdSe). This calculation gives the volume of material per unit area, appropriate when calculating the thickness of layers that are deposited on rough surfaces or layers that acquire roughness during growth. From the deposition time and a map of the effective thickness, a map of the deposition rate can be obtained. This calibration can be used to generate effective thickness maps from the deposition time for the subsequent solar cell depositions performed under the same conditions. This is the unique aspect of M-SE compared to other thickness probes, namely the ability to map the volume of film per area of substrate, even on surfaces with roughness modulations larger than the overlying film thickness.

For thickness-performance correlations, current-voltage (J-V) measurements of 81 dot cells per $6.5 \text{ cm} \times 6.5 \text{ cm}$ sample were performed in the dark and under AM 1.5G illumination [39] following the same location pattern as M-SE. EQE spectra for the highest efficiency devices were measured at 0 V bias potential. Both the J-V and EQE measurements were performed using commercial instruments (PV Measurements, Inc.).

2.2.1. CdS effective thickness calibration

Fig. S2a of Appendix A, Supplementary data, shows ellipsometric spectra in (ψ, Δ) measured from the film side of the calibration sample

consisting of thin film CdS on soda-lime glass (SLG/CdS). The pair of spectra is characteristic of one of the 81 locations from the full M-SE data collection for the SLG/CdS sample. The CdS effective thickness intended at the center of the calibration sample was 27 nm, the largest value applied in the second CdS series of Section 3.2. This calibration sample is not optimal for the extraction of the CdS complex dielectric function (ϵ $= \varepsilon_1 + i\varepsilon_2$) spectra, however, because of the thinness of the CdS and the use of a SLG substrate. In fact, the spectra in ε must be determined together with the structural parameters of primary interest for calibration. Previous studies have shown that up to 22 parameters are needed to describe ε for CdS, including 15 parameters associated with the three observed critical points, four associated with a broad background oscillator describing non-parallel band transitions, two with an expression describing the sub-bandgap Urbach tail, and a constant contribution to ε_1 [36]. Details regarding the analysis of the complex dielectric function spectra including the sub-bandgap Urbach tail can be found in Notes 1 and 2 of Appendix A.

Typically, in the analysis of the full M-SE data collection, among the 22 parameters describing $\varepsilon(E)$, a number of these parameters are fixed to values obtained in an analysis of the single crystal material or a polycrystalline material of the largest obtainable grain size. Parameters can also be fixed based on analysis at one or more locations of optimum thickness or different thicknesses, respectively. In the analysis of the CdS calibration sample, this latter approach has been applied such that an analysis is done at the location where the CdS is thickest. Because of the interest in determining the area uniformity of the absorption onset parameters, all dielectric function parameters with the exception of the fundamental bandgap CP values of the amplitude A_0 , resonance energy E_0 , and broadening energy Γ_0 , as well as the Urbach slope E_u , were fixed in generating the final maps. Table S2 of Appendix A presents the 18 fixed and four best-fit variable parameters, the latter with their confidence limits, that characterize the CdS dielectric function used in the analysis of the representative pair of spectra presented in Fig. S2a. The resulting dielectric function is shown in Fig. 1 where the three critical points designated E₀, E₁-A, and E₁-B [40] occur at photon energies of 2.40, 4.96, and 5.52 eV (see Appendix A, Note 1). Additional details regarding the identification of the free and fixed parameters and the structural model are presented in Appendix A, Note 2.

2.2.2. CdSe effective thickness calibration

Fig. S4a of Appendix A, Supplementary data, shows ellipsometric



spectra in (ψ , Δ) corresponding to a single location on the TECTM15/ HRT/CdSe calibration sample. The pair of spectra is characteristic of one of the 81 locations from the full M-SE data collection for this sample. The intended effective thickness of the CdSe at the center of the calibration sample was ~145 nm. Because this layer is thicker than that studied for CdS calibration and thicker than the roughness layer on the HRT, the TECTM15/HRT structure could be used as the substrate for the CdSe calibration sample and still allow accurate structural parameter maps. In this case, variations in the CdSe optical properties can arise over the area of the sample due to the wider range of thicknesses over the area.

The model for $\varepsilon(E)$ of the CdSe and the identification of the fixed parameters used in the M-SE analysis resulted from a multi-thickness analysis applied to a deposition performed under identical conditions but on a native oxide coated Si wafer substrate. For multi-thickness analysis, multiple locations on the 6.5 cm \times 6.5 cm sample were analyzed simultaneously to obtain 21 complex dielectric function parameters along with the bulk and surface roughness layer thicknesses. The complex dielectric function model in this case uses three critical points, the fundamental bandgap CP designated E₀-A, appearing at 1.732 eV in the single crystal (optical electric field E \perp *c*-axis of the wurtzite phase); a broad CP designated E_0 -C, appearing at 2.16 eV in the crystal; and a second broad CP designated E_1 , appearing as a collection of transitions in the single crystal starting with E₁-A at 4.10 eV [41]. In addition to the three CPs, a constant contribution ε_{10} , a background Tauc-Lorentz oscillator, and the Urbach tail are used. In this model, the transition energy E_t of the Urbach tail could be fixed at E_0 , the fundamental bandgap. In the M-SE analysis, 13 of the complex dielectric function parameters from among the 21 parameters determined from the multi-thickness analysis were varied in the analysis of the full maps. These 13 variable parameters include the amplitude A_n , resonance energy E_n , and broadening Γ_n for the three CPs, the amplitude A_{TL} and broadening Γ_{TL} for the Tauc-Lorentz oscillator, ε_{1o} the constant contribution, and the Urbach tail slope E_u .

In addition to the complex dielectric function model, a structural model of the TECTM15/HRT/CdSe sample is required. For the structural model and fixed parameters, the TECTM15/HRT substrate was measured prior to CdSe deposition, performing M-SE at the same locations as the M-SE measurement of the TECTM15/HRT/CdSe structure. Analysis of these results provided maps in the SnO₂, SiO₂, SnO₂:F, and SnO₂ HRT bulk layer thicknesses as well as maps in the SnO2 HRT surface roughness layer thickness and material volume fraction in the roughness layer. The resulting parameters were fixed for the corresponding locations of the TECTM15/HRT/CdSe. In the analysis of the CdSe coated structure, it is assumed that the CdSe fills the voids in the HRT surface roughness measured before CdSe deposition. As a result, the only free parameters in the structural analysis include the CdSe bulk and surface roughness layer thicknesses and the volume fraction of CdSe in the surface roughness. Additional information regarding the model for $\varepsilon(E)$, the parameters used in M-SE analysis of the CdSe, and the structural model for the TECTM15/HRT/CdSe sample can be found in Appendix A, Note 3. The resulting best fit dielectric function from the analysis of Fig. S4a is shown in Fig. 1.

3. Results and discussion

3.1. Mapping spectroscopic ellipsometry

By applying the six free parameter optical and structural model to the pairs of (ψ, Δ) spectra at all 81 locations for the SLG/CdS calibration sample, the four maps of interest depicted in Fig. 2 are generated. Shown in Fig. 2 are the structural parameters of bulk layer thickness d_b , surface roughness layer thickness d_s , and effective thickness $d_{\text{eff}} = d_b + 0.5d_s$. The bulk layer thickness shows a variation from the maximum of ~25.5 nm at the center to ~17 nm, or ~70% of the maximum, in the upper right corner. The surface roughness shows a weak variation between 2.4 and 3.3 nm. Surface roughness development for a thin film starting from



Fig. 2. Maps over an area of 6.5 cm \times 6.5 cm for a CdS calibration film with an intended effective thickness of 27 nm deposited on a SLG substrate. Mapped structural parameters include the (a) bulk layer thickness d_b and (b) surface roughness layer thickness d_s [as in Appendix A, Fig. S2b for the location (3.250, 1.625) (in cm)], (c) effective thickness $d_{\text{eff}} = d_b + 0.5d_s$, and (d) bandgap energy [as in Appendix A, Table S2].

a smooth substrate typically exhibits two regimes, a decay or coalescence of nucleation induced roughness in the early stages of bulk layer growth and an enhancement in the later stages due to atomic scale self-shadowing [42–44]. The effective thickness reflects the bulk layer thickness variation with a maximum of \sim 27 nm at the center and a

minimum of ~ 18 nm at the upper right corner. Also shown is a map of the bandgap in Fig. 2d. Overall, a correlation is observed between the bulk layer thickness and the bandgap as plotted in Fig. S3a of Appendix A such that a wider bandgap is obtained for a thicker film. Similar behavior has been observed for CdSe as will be described in the



Fig. 3. Maps over an area of 6.5 cm \times 6.5 cm for a CdSe calibration film with an intended effective thickness of 145 nm deposited at room temperature on a TECTM15/HRT substrate including the (a) bulk layer thickness d_b and (b) surface roughness layer thickness d_s [as in Appendix A, Fig. S4b for the location (-2.438, 1.625) (in cm)], (c) effective thickness $\Sigma_i d_i f_i$, where the sum is over all layers i = 1,2,3 that incorporate CdSe with f_i being the volume fraction of CdSe in layer i, and (d) bandgap as in Appendix A, **Table S3**. The effective thickness in (c) is a measure of CdSe material volume per unit area of substrate.

discussion of Fig. 3. Such a trend observed for all sputtered II-VI thin films may be due to an increase in the in-plane film stress with thickness [45,46], an effect described in detail for CdTe in previous work [47].

Although the variations in bandgap are of interest for evaluating film stress, the importance of the M-SE analysis lies in the effective thickness or volume of film per substrate area in Fig. 2c, as calculated from the bulk and surface roughness layer thicknesses in Fig. 2a and b. From the deposition time of 3 min, a map of the effective thickness deposition rate can be deduced. Thickness maps can then be obtained for subsequent depositions based simply on the time durations of the depositions. Although such calibrations require precise reproducibility of the depositions, the non-uniformity patterns are generally more reproducible. This implies that correlations between device performance parameters and thickness will be accurate within a single run whereas larger errors may occur in comparing the correlations of one run with another. Such errors may be minimized by performing M-SE calibrations on a regular basis.

The corresponding maps obtained in the analysis of the TECTM15/ HRT/CdSe calibration sample using 13 dielectric function and three structural parameters are depicted in Fig. 3. The structural parameters in Fig. 3 reflect circular patterns of the 7.6 cm CdSe target with the bulk layer thickness ranging from \sim 53 nm in the upper right corner to \sim 101 nm at the center. It is clear that the surface roughness is correlated with the bulk layer thickness, ranging from a minimum of 38 nm at the upper left corner where the CdSe is thin to a maximum of 47 nm at the center where the CdSe is thickest. This suggests that as the CdSe thickness increases, atomic scale self-shadowing leads to a dominant roughening trend starting from the roughness imposed by the underlying HRT. Combining the CdSe components of all layers yields an effective thickness ranging from 91 nm at the upper right corner to 145 nm at the center. Given the deposition time of 14 min, a map of the deposition rate in terms of effective thickness can be generated. This calibration map can be used to estimate the effective thickness maps of subsequent depositions, given the deposition time. From the maps in Fig. 3, a correlation is observed between the bulk layer thickness in Fig. 3a and the bandgap in Fig. 3d. This correlation is plotted in Fig. S3b of Appendix A. For CdSe as for CdS, a wider bandgap is obtained for a thicker film, indicating the buildup of in-plane film stress with increasing thickness.

3.2. Solar cell correlations

In a previous study, the effective thickness of the CdSe front layer was optimized for incorporation into the CdTe1-xSex solar cell fabricated from CdSe/CdTe layers, but without a CdS window layer [34]. A correlation between the cell performance parameters and the starting CdSe effective thickness for the set of devices showed a well-defined J_{sc} and efficiency optimum for a thickness of 150 nm [34]. Because of the loss in Voc for devices fabricated from CdSe/CdTe layers, Poplawsky et al. suggested that addition and optimization of an interface layer between the SnO₂ HRT and CdSe layers were necessary [16]. Overall the presence of CdS or CdS:O between the SnO₂ HRT layer and the front CdSe_{1-w}Te_w in the final device avoids a direct SnO₂/CdSe_{1-w}Te_w interface which is believed to exhibit a larger band offset than the standard SnO₂/CdS interface, thus accounting for the reduction in the device quality and poorer shunt performance [15,16]. Here, CdSe1-wTew designates the material closer to the interface with the HRT derived from the CdSe layer by in-diffusion of Te from the underlying CdTe.

In the present study, several devices fabricated from CdS/CdSe/CdTe structures have been prepared with a range of calibrated effective thicknesses, including depositions of CdS with maximum values of 65 and 100 nm for the first set of runs and 6, 13, 20, and 27 for the second set. These depositions generate a wide range of CdS effective thicknesses from 4 to 100 nm, in order to gain insights into the effect of incorporating a CdS layer within the previously studied windowless device fabricated from CdSe/CdTe layers. Calibrated maximum thicknesses of CdSe of 110 nm and 175 nm were sputter deposited at room temperature

on top of the TECTM15/HRT/CdS structures, generating two ranges of CdSe thickness spanning from 65 to 175 nm. Thus, application of the different thicknesses of CdS and CdSe provides broad ranges of effective thicknesses of these layers due in part to the non-uniformity of the deposition over the sample area. The statistics of the correlations between the device performance parameters and the effective thicknesses of the CdS and CdSe layers are improved through the use of the M-SE based calibrations that provide the effective thickness of each layer as a function of the device coordinates on the sample surface. As a result, the improved statistics made possible by utilizing non-uniformity in the deposition process along with the M-SE calibrations aid in fine-scale optimization of solar cell performance.

Fig. 4 shows the performance parameters of the first set of solar cells fabricated from CdS/CdSe/CdTe structures. These parameters are correlated with the effective thickness of the CdSe layer. This first data set explores a combination of the CdS thickness (~100 nm) that is nearly optimum for the CdS/CdTe solar cell, with the CdSe thickness (~150 nm) that is optimum for the CdTe_{1-x}Se_x solar cell. Two CdS runs were performed on TECTM15/HRT with maximum effective thicknesses of 65 and 100 nm, providing a range from 45 to 100 nm, the latter value approaching that of the optimum for the CdS/CdTe solar cell. Each such structure was then over-deposited with CdSe having a maximum effective thickness of 175 nm. As a result, in the correlations of Fig. 4, a range in the effective thickness of the CdSe from 100 to 175 nm was obtained over the area of the sample structure. This effective thickness range of CdSe encompasses the optimum value of 150 nm identified without incorporation of the CdS window layer within the device [34]. A component of the scatter in the plots of Fig. 4 arises from variations in CdS thickness for a given CdSe thickness. Although the effective thicknesses for CdS in Fig. 2 and CdSe in Fig. 3 exhibit correlations, such scatter is observed due to the different patterns for the deposition systems.

By comparing the best cell parameters for CdS and CdSe respective thicknesses of 100 nm and 150 nm in Fig. 4 (Voc \sim 0.78 V, FF \sim 0.70, J_{sc} $\sim 19 \text{ mA/cm}^2$) with the best cell parameters for a CdSe thickness of 150 nm and no CdS layer in Ref. [34] ($V_{oc} = 0.75$ V, FF = 0.67, $J_{sc} = 26$ mA/cm^2 , reproduced in Table 1), one finds that the dominant effect of adding a standard thickness CdS layer is the loss of current density. This is expected due to absorption by the inactive CdS or CdS_{1-v}Se_v alloy material. Another J_{sc} loss that may occur when the CdS and CdSe layers are both present is associated with the diffusion of Se into the CdS which reduces its bandgap, further enhancing the inactive layer absorption losses. This latter effect may account for the lower J_{sc} for the device fabricated from CdS/CdSe layers (~19 mA/cm²) compared to the CdS/CdTe device without CdSe (\sim 22 mA/cm²; see Table 1). A CdS_{1-y}Se_y alloy region adjacent to the HRT where Se has diffused into CdS may have additional detrimental effects on cell performance, depending on the Se content y. Such effects would be relatively weak as long as y is small. If y approaches 0.5, however, much more significant detrimental effects are likely to result due to the greater fluctuations in potential and shorter carrier mean free time, as described by Nordheim's rule for disordered solid solutions [48]. Partially offsetting the loss of J_{sc} , increases in both $V_{\rm oc}$ and FF occur with the addition of the CdS layer, as would be expected due to an improvement of the contact to the SnO2 HRT provided by a wider bandgap alloy. Compared to the SnO₂/Cd-Se_{1-w}Te_w interface, the advantage of the SnO₂/CdS_{1-y}Se_y interface is a smaller band offset and higher shunt resistance $R_{\rm sh}$, which decreases recombination and increases minority carrier lifetime [16,30,31].

The effect of the addition of the CdS layer is summarized in Table 1 which provides the performance parameters of the highest efficiency CdS/CdTe and CdSe/CdTe devices, as well as those of the first set of CdS/CdSe/CdTe based devices with 65 and 100 nm CdS effective thicknesses. Comparing rows labeled (ii) and 1/(iv), it is observed that with the addition of the CdS layer to the device fabricated from CdSe/CdTe layers, the efficiency trend reflects J_{sc} but opposes V_{oc} , with the *FF* tending to follow V_{oc} . Similar trends are observed by comparing



Best performing solar cells from four groups of CdTe devices: (i) CdS/CdTe with 120 nm CdS (one cell); and in order of increasing CdS thickness: (ii) CdSe/CdTe with 148 nm CdSe (one cell); (iii) CdS/CdSe/CdTe with 6–27 nm CdS and 110 nm CdSe (four cells); and (iv) CdS/CdSe/CdTe with 65 and 100 nm CdS and 175 nm CdSe (two cells). Thicknesses shown are calibrated values for the specific device. The set numbers for groups (iii) and (iv) are from Appendix A, Table S1.

Set #/Group	CdTe device run	Voc (V)	Jsc (mA/cm²)	FF (%)	Efficiency (%)
(i)	(120 nm CdS)/CdTe - Standard	0.832	22.1	72.7	13.4
(ii)	(148 nm CdSe)/CdTe	0.753	26.0	67.0	13.1
2/ (iii)	(6 nm CdS)/(80 nm CdSe)/CdTe	0.713	25.5	64.1	11.6
2/ (iii)	(13 nm CdS)/(100 nm CdSe)/CdTe	0.782	26.4	66.3	13.7
2/ (iii)	(16 nm CdS)/(71 nm CdSe)/CdTe	0.715	24.9	65.3	11.6
2/ (iii)	(21 nm CdS)/(82 nm CdSe)/CdTe	0.711	24.3	53.9	9.31
1/ (iv)	(47 nm CdS)/(109 nm CdSe)/CdTe	0.772	24.0	68.6	12.7
1/ (iv)	(73 nm CdS)/(114 nm CdSe)/CdTe	0.792	22.3	69.2	12.2

averages of the ten best cells for the corresponding rows in Table S4 of Appendix A. Fig. 4 shows that although there is an increase to $V_{oc} \sim 0.78$ V and *FF* ~ 0.70 with the addition of CdS to the optimum device fabricated from CdSe/CdTe, the values do not reach those in Table 1 obtained for the standard CdS/CdTe device without the CdSe interface layer, $V_{oc} \sim 0.83$ V and *FF* ~ 0.73 . This observation supports the suggestion of a relatively weak detrimental effect of the CdS_{1-y}Se_y interaction region for thick ($\sim 50-100$ nm) CdS. Devices of the first set with the highest overall performance are obtained with approximately the minimum CdS thicknesses (~ 50 nm, ~ 70 nm) and minimum CdSe thickness (~ 110 nm) within each of the two runs labeled 1/(iv) in Table 1.

Also of interest in Fig. 4 is the observation that all performance

Fig. 4. Correlations between M-SE calibration of CdSe effective thickness at the precise solar cell location and the solar cell parameters of (a) opencircuit voltage $V_{oc.}$ (b) short-circuit current density J_{sc} , (c) fill-factor *FF*, and (d) efficiency for solar cells fabricated with maximum CdS effective thicknesses of 65 and 100 nm and a maximum CdSe thickness of 175 nm. The low thickness range of the data set for 100 nm CdS overlaps with the maximum thicknesses of the data set for the 65 nm CdS.

parameters improve with the reduction in CdSe effective thickness over the range from 175 nm down to 110 nm. The improvement in the FF follows that observed in cells fabricated from CdSe/CdTe without CdS [34] and may be associated with the reduction of recombination losses within a Se rich CdSe_{1-w}Te_w interaction layer derived from Te diffusion into CdSe [16]. This layer is expected to become thinner or exhibit larger w when the CdSe thickness is reduced. The trend in V_{oc} in Fig. 4 must be associated with the presence of CdS since it is opposite to the behavior observed without CdS in Refs. [34]. This increase in Voc with the reduction in CdSe thickness may be due to an improvement in the material quality in the front region of the device whereby the smaller quantity of Se associated with thinner CdSe results in less Se diffusion into the CdS, leading to a less defective (lower y) $CdS_{1-y}Se_y$ region. Finally, the improvement in J_{sc} as the CdSe thickness decreases over its full range is also opposite to the behavior observed without CdS. This improvement extends from ~ 21 to 24 mA/cm² for the minimum CdS effective thickness of \sim 50 nm, the envelope of maxima in Fig. 4b, and is consistent with the possibility that the smaller quantity of Se from a thinner CdSe layer leads to smaller bandgap reduction for the inactive CdS_{1-y}Se_y and thus lower absorption loss.

The highest overall performance for the devices in Fig. 4 has been obtained with the minimum CdS and CdSe effective layer thickness for each run labeled 1/(iv) in Table 1. Even so, J_{sc} and the efficiency for the lowest CdS thickness appear to be saturating as the CdSe thickness is reduced to its minimum of ~110 nm. Based on the above discussion, a complicated trade-off may lead to such an effect, controlled predominantly by J_{sc} . For the lowest CdSe thicknesses, the notch-like bandgap profile in the absorber established by Se diffusion into CdTe to generate CdTe_{1-x}Se_x may not be strong enough. For CdSe thicknesses above the optimum, both recombination losses in a low w CdSe1-wTew region and absorption losses in the CdS_{1-v}Se_v region are proposed to occur as described above. This interdiffusion problem between CdS and CdSe is proposed to account for losses in both V_{oc} and J_{sc} with increased CdSe thickness in Fig. 4. The problem has also been considered previously from the perspective of S diffusion into the CdSe interface layer as a function of the CdS thickness. This can be evaluated by probing the surface of a CdS/CdSe bilayer after deposition of the CdSe layer [49].

Due to the small lattice mismatch between the CdS and CdSe [10], significant diffusion of S and Se occur into the CdSe and CdS layers,

respectively. Junda et al. [49] show that even for a relatively thin CdS layer, S can be detected on the surface of the subsequently deposited CdSe as a result of the intermixing between the CdS and CdSe layers. They also found that the fraction of S in the top layer of the structure increases with increasing effective thickness of the underlying CdS layer. These observations suggest that for the structures with 100 nm CdS, a photo-inactive CdSe1-zSz layer forms within the CdSe layer by S in-diffusion, and any photons absorbed in this layer would be lost due to the defective material having an undesirably high S content [18,49]. In fact, $CdSe_{1-z}S_z$ alloys with $z \sim 0.5$ can exhibit a particularly high defect density as indicated by a very broad Urbach tail in as-deposited material [49]. It can be concluded that reductions in both the CdS and CdSe effective thicknesses may limit the volume of such defective material derived from the CdSe and also possibly avoid an excessive Se content CdSe_{1-w}Te_w layer adjacent to the CdTe_{1-x}Se_x absorber. Thus, the above trends and suggestions motivate exploration of devices incorporating CdS and CdSe layers that are both thinner than those in Fig. 4. Next, the effect of the CdS thickness on the performance of solar cells fabricated from CdS/CdSe/CdTe structures will be presented and discussed, focusing on thinner layers used for the second set of devices.

Fig. 5 shows the correlation between the M-SE calibrated measurements of CdS effective thickness and the solar cell performance parameters. Results are included for four device structures fabricated from CdS/CdSe/CdTe layers with four different maximum CdS effective thicknesses of 6, 13, 20, and 27 nm, as well as a maximum of 110 nm for the CdSe effective thickness. A component of the scatter in these plots arises from the variation in CdSe thickness for a given CdS thickness. This variation will be addressed in the discussion of Fig. 6. The highest performance device with the thinnest CdS (6 nm maximum) has low $V_{\rm oc}$ and FF (0.71 V, 0.64; see Table 1), and this may be due to nearly complete consumption of the thin CdS layer at the interface through dissolution into the CdSe region. In fact, the performance parameters for this best device are similar, but each slightly lower (\sim 2–3%), in comparison with those of the highest efficiency device fabricated from CdSe with the corresponding 110 nm effective thickness but without a CdS layer (0.72 V, 0.66) [34]. For the devices with thinnest CdS, a $SnO_2/CdSe_{1-z}S_z$

interface is likely to form with a low value of z and a larger band offset leading to associated reductions in cell performance. In fact, because the reductions are larger than expected from a complete loss of the CdS, one can conclude that even a thin $CdSe_{1-z}S_z$ alloy layer of small z in the solar cell has a weakly detrimental effect on V_{oc} and *FF* compared to pure CdSe, as reflected through a broadening of the Urbach tail upon alloying [49]. This alloy broadening effect apparently overcomes any possible improvements through reduction of the bandgap offset at the HRT/CdSe_{1-z}S_z interface. Although Ref. [49] has demonstrated that Urbach tail broadening can be reduced significantly by annealing the CdSe to the high temperatures of overlying CdTe deposition by close-space sublimation (CSS), evidence from studies of other II-VI compound materials suggest that the temperatures associated with the CdCl₂ treatment are not sufficient to generate the same effect as high temperature annealing [50–53].

Thus, it can be concluded that incorporating CdS between the HRT and CdSe in the solar cell fabricated from CdSe/CdTe does not necessarily lead to an improvement in Voc and FF performance by reduction of the band offset at the contact. In fact, a sufficient thickness of CdS is likely to be required in order to compensate for CdS loss by intermixing with the CdSe which also leads to a more defective material. Another limitation of complete dissolution of the thin CdS may be understandable from the calculations of Wie et al. who suggest a weak bowing effect even for the CdSe1-zSz alloys, although this effect has not been observed experimentally, possibly due to Urbach tail broadening [49]. Considering this problem more generally, it can be concluded that adding a very thin CdS layer between the HRT and a thick narrower bandgap material such as CdTe or CdSe may not measurably increase the bandgap of the material adjacent to the HRT due to complete dissolution of S, which in the case of CdTe is expected to decrease the gap due to bowing. This dissolution of CdS is further likely to reduce the quality of the front contact region of the cell through the alloying that occurs [10].

In Fig. 5, the 13 nm CdS device provides the highest J-V performance parameters and highest efficiency, with low series resistance R_s and high R_{sh} . This is likely to represent a trade-off between the reduction of the band offset at the front contact through an increase in the bandgap by



Fig. 5. Correlations between M-SE calibration of CdS effective thickness at the precise solar cell location and the solar cell parameters of (a) open-circuit voltage V_{oc} . (b) short-circuit current density J_{sc} , (c) fill-factor *FF*, and (d) efficiency. These results were obtained for solar cells fabricated with maximum CdS thicknesses of 6, 13, 20, and 27 and a maximum CdSe thickness of 110 nm.



Fig. 6. Correlations between M-SE calibration of CdSe effective thickness at the precise solar cell location and the solar cell parameters of (a) open-circuit voltage V_{oc} , (b) short-circuit current density J_{sc} , (c) fill-factor *FF*, and (d) efficiency. Results are given for the solar cells of Fig. 5 with four different maximum effective thicknesses of CdS.

increased S content there, enhancing the performance, and the generation of a more highly defective CdSe_{1-z}S_z alloy of larger z at the front of the device, reducing the performance [14,15,30–32]. Using more than 13 nm effective thickness for the CdS layer (e.g. 20 and 27 nm in Fig. 5) reduces V_{oc} , J_{sc} , and FF as shown in Fig. 5, and is attributed to a more extensive or larger z $CdSe_{1-z}S_z$ layer at the front that dominates over any improvement in the contact. In fact, the poorest performance is likely to occur over a range of thicknesses where CdSe_{0.5}S_{0.5} forms and dominates the front of the device, as indicated by the most extensive Urbach tail near this composition in accordance with Nordheim's rule [48]. Although the maximum efficiency for the second set of samples with reduced CdS and CdSe thicknesses is higher than that for the first set due to the maximum J_{sc} among all cells, Table 1 and Table S4, the latter for the average of the best ten devices presented in Appendix A, show that both V_{oc} and FF for the best of the second set of samples with (13 nm CdS)/(100 nm CdSe) is lower than those of the first set with (73 nm CdS)/(114 nm CdSe). This may be attributed to the improved HRT/CdS_{1-y}Se_y interface with smaller y for the thicker CdS of the first set of samples that leads to a lower band offset at this interface.

Fig. 6 shows the correlations between M-SE calibration of CdSe effective thickness at the precise solar cell location and the solar cell parameters. These solar cells, fabricated with maximum CdS thicknesses of 6, 13, 20, and 27 and a maximum CdSe effective thickness of 110 nm, represent a replotting of the data from Fig. 5. This figure shows a broader maximum in efficiency than that associated with CdS. The CdS and CdSe effective thickness combination of 13 and 100 nm, respectively, yields the highest efficiency. This result is in good agreement with Paudel et al. [14], who found optimum CdS and CdSe thicknesses of 15 and 100 nm, respectively, in the same CdS/CdSe bilayer configuration. One notable difference in Ref. [14] is the higher CdSe substrate temperature of 250 °C versus room temperature used in the present study. For this second set of samples with thinner CdS and CdSe, the trade-off for CdSe is likely to be similar to that described earlier for the first set, namely an insufficient CdTe1-xSex bandgap profile along with a CdSe_{1-z}S_z alloy with excess z in the window layer region at lower CdSe thickness, and recombination losses in a low w CdSe1-wTew region

adjacent to the alloy absorber at higher thicknesses.

To illustrate the dominant effects described in detail above, J-V measurements for the three highest performance CdTe devices fabricated using different front layers of CdS, CdSe, and CdS/CdSe have been presented in Fig. 7a and b. Optimization of the CdTe devices fabricated using individual CdS and CdSe front layers has been described in previous studies [34,36]. Table 1 shows the parameters for the highest efficiency CdTe solar cells fabricated using the following front layers: (i) standard 120 nm thick CdS [36] and, in order of increasing CdS thickness, (ii) 148 nm thick CdSe from the previous study [34] and (iii, iv) CdS/CdSe from the second and first sets of samples, respectively, including the best cells for each deposition run of a given maximum CdS thickness. When the 120 nm thick CdS layer is applied as the front layer, $V_{\rm oc}$ and FF are maximized (0.83 mV, 0.73) among all the best devices in Table 1; however, due to absorption of high energy photons in the short wavelength region within the inactive CdS layer, J_{sc} is the lowest among the three devices depicted in Fig. 7. For the windowless device fabricated from CdSe/CdTe, the incorporation of \sim 150 nm thick CdSe leads to a significant enhancement in J_{sc} as shown in Table 1. The high value of $J_{\rm sc}$ reflects the interdiffusion of CdSe and CdTe at the CdSe/CdTe interface and the photo-electronic activity of the resulting alloy [14]. Voc is significantly reduced, however, due to the lower bandgap of the CdSe_{1-w}Te_w ternary alloy at the interface to the SnO₂ HRT. As a result, additional recombination is expected in this near-contact region. After adding a very thin CdS layer (13 nm) beneath a 100 nm layer of CdSe, $V_{\rm oc}$ is enhanced over the cell structure without the CdS deposition as indicated in Fig. 7b. Also noted in Fig. 7b is the increase in J_{sc} by 1.5% for the structure with 13 nm CdS layer relative to that without the CdS layer. This may occur because of the widening of the bandgap at the front contact interface and a reduction in recombination losses near this front contact.

To understand the photo-generated current, the EQE spectra for the best CdTe solar cells of Fig. 7a and b fabricated with CdS (120 nm), CdSe (148 nm), and CdS/CdSe (13 nm)/(100 nm) front layers were measured as shown in Fig. 7c and d. Fig. 7c shows a comparison of the EQE spectra of the devices fabricated from CdS/CdTe and CdS/CdSe/CdTe layers.



Fig. 7. (a, b) Light and dark J-V characteristics, and (c, d) external quantum efficiency spectra for the highest efficiency CdTe solar cells fabricated using the CdS and CdSe thicknesses indicated in the legends as calibrated at the cell location. (a) and (c) A comparison of the cell from CdS/CdSe/CdTe incorporating (13 nm)/(100 nm) CdS/CdSe and the cell from CdS/CdSe/CdTe incorporating (13 nm)/(100 nm) CdS/CdSe and the cell from CdS/CdSe/CdTe incorporating (13 nm)/(100 nm) CdS/CdSe and the cell from CdSe/CdTe [34].

For the latter cell, the EQE shows an almost rectangular shape with an average EQE of \sim 80% over the range of 370–830 nm, suggesting very little absorption loss by the front CdS/CdSe bilayer due to the thinness of the CdS. Compared with the CdS/CdTe solar cell, the device with the bilayer has improved response in both the long and short wavelength regions. The long wavelength region enhancement comes from the formation of a CdTe_{1-x}Se_x alloy whose bandgap is lower than CdTe due to bowing whereas the short wavelength region enhancement comes from the very thin CdS and the consumption of the CdSe layer through interdiffusion with CdS and CdTe. As a result, a photo-electronically active alloy material exists near the front of the cell [14,15,30,34]. The resulting two alloy materials including CdS_{1-v}Se_v and CdTe_{1-x}Se_x, however, appear have higher defect densities since the EQE of $\sim 80\%$ over the wide wavelength range is lower than the maximum EQE of \sim 90% at the center of the wavelength range for the standard CdS/CdTe solar cell.

In contrast to the sputtered CdTe cell of Fig. 7c with an EQE of $\sim 80\%$ over the wide wavelength range, a higher EQE of ${\sim}86\%$ over the 370-830 nm range has been obtained for solar cells with CdTe_{1-x}Se_x absorbers in which case the CdTe is prepared by CSS at high temperature (~600 °C) [14,22]. This suggests that the higher temperature of CSS deposition reduces the defect densities of the alloys, compared to cells fabricated by sputtering in which the maximum process temperature is 390 °C during the CdCl₂ treatment. Another possible contribution to the differences in maximum EQE may be optical in nature, namely a higher index of refraction difference at the HRT/CdS_{1-v}Se_v interface compared to the HRT/CdS interface. Such an optical effect would be observed in both sputtered and CSS devices. For the CSS CdTe devices with CdTe_{1-x}Se_x absorbers, however, both experimental EQE and simulations yield similar values of ${\sim}87\%$ for both CdS/CdTe and CdTe_1-xSe_x devices near 650 nm where the CdS/CdTe device exhibits its maximum EQE [14, 22]. As a result, such an optical effect, when considered in detail, is found to be negligible. This is likely due to the rough interface between the HRT and the semiconductor which acts as a graded antireflection layer irrespective of the indices of refraction on each side of the interface.

Fig. 7d highlights the comparison between the devices fabricated

with the CdSe and the CdS/CdSe front layers. Both devices show high collection in the short wavelength region relative to the CdS front layer, but the CdS/CdSe bilaver device shows improved response over the device without CdS. This may be due to a residual Se-rich CdSe_{1-w}Te_w region in the latter device which is detrimental to current collection but serves to improve the contact to the HRT compared to a lower bandgap, higher w CdSe_{1-w}Te_w layer [14,34]. It is notable that over the long wavelength range of 850-900 nm, the CdS/CdSe device response is better than that of the windowless device. This suggests that a deeper minimum in the bandgap profile has been achieved by diffusion of Se into CdTe in the device fabricated from CdS/CdSe/CdTe [14]. Possibly with the 150 nm thick CdSe layer of the windowless device, the front contact is improved with excess Se content by sacrificing an optimum bandgap profile. In fact, the slightly enhanced current collection in the wavelength regions from 650 to 800 nm in the EQE spectra of the CdSe/CdTe device is an indication of an improved compositional profile of the windowless device extending deep into the CdTe absorber. This is possible due to the larger amount of Se [14].

4. Summary

CdTe solar cells starting from CdS/CdSe front layers have been fabricated on transparent conducting oxide coated glass with overlying high resistivity transparent layers. Mapping spectroscopic ellipsometry (M-SE) has been applied to the CdS and CdSe films in order to calibrate the deposition processes and identify accurate effective thicknesses (or volume/area) of these films at the precise locations on the substrate where the solar cells are fabricated.

It has been found that with the addition of CdS to the previously studied CdSe/CdTe structures [34] as the first layer in the fabrication process, two ranges of CdS thickness lead to maxima in the product of V_{oc} and *FF*. These appear to occur when dilute solutions of CdS within CdSe (CdSe_{1-z}S_z) are present at the front of the device for low CdS thicknesses (~10 nm) and dilute solutions of CdSe within CdS (CdS_{1-y}. Se_y) are present at high CdS thicknesses (~100 nm). This is evident from Table 1 for the entries 2/(iii) and 1/(iv) which are ordered in terms of increasing CdS effective thickness. Increases in the CdS thickness in the

low thickness range and increases in the CdSe thickness in the high thickness range lead to rapid decreases in the product of V_{oc} and *FF*. These decreases are proposed to result from the formation of CdSe_{1-z}S_z and CdS_{1-y}Se_y interdiffusion layers, respectively, with z and y each increasing toward 0.5 where the electronic properties of the alloy suffer the most, as expected from Nordheim's rule and observed experimentally in the slope of the Urbach tail of the alloy material [49]. V_{oc} decreases are also proposed for low bandgap alloyed materials adjacent to the HRT due to the expected larger band offsets. In spite of the lower bandgap at the HRT interface and the detrimental effects of CdSe_{1-z}S_z alloying at the front of the device, the thin CdS layer optimum gives higher overall device performance. The reason is the significant gain in current possible in both short and long wavelength ranges that overcomes the decrease in the $V_{oc} \times FF$ product.

At both the low and high CdS thickness optima in the $V_{oc} \times FF$ product, the optimum CdSe thickness is ~100 nm. For the thin CdS layer optimum, this CdSe thickness optimum is proposed to result from an insufficient CdTe_{1-x}Se_x bandgap profile along with a CdSe_{1-z}S_z alloy with excess z in the window layer region at lower CdSe thickness, and from recombination losses in a low w CdSe_{1-w}Te_w region adjacent to the alloy absorber at higher thicknesses. These considerations are proposed to account for the highest performance CdS/CdSe/CdTe solar cell which incorporates 13 nm and 100 nm effective thicknesses of CdS and CdSe, respectively.

The results obtained here suggest further applications of M-SE for analysis of the graded layers resulting from CdS/CdSe/CdTe interactions due to the device fabrication and processing at elevated temperatures. With a database of dielectric functions [21,22], M-SE can be used to characterize the structure and the bandgap profiles of the absorbers of CdSe/CdTe and CdS/CdSe/CdTe solar cells, as has been done for CuIn_{1-x}Ga_xSe₂ absorbers [54,55].

CRediT authorship contribution statement

Mohammed A. Razooqi Alaani: Conceptualization, Methodology, Formal analysis, Writing - original draft. Prakash Koirala: Methodology, Formal analysis. Puja Pradhan: Formal analysis. Adam B. Phillips: Resources. Nikolas J. Podraza: Writing - review & editing. Michael J. Heben: Resources. Robert W. Collins: Conceptualization, Validation, Writing - review & editing, Supervision.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Appendix A. Supplementary data

Supplementary data to this article can be found online at https://doi.org/10.1016/j.solmat.2020.110907.

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M.A. Razooqi Alaani et al.

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- Solar Energy Materials and Solar Cells 221 (2021) 110907
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